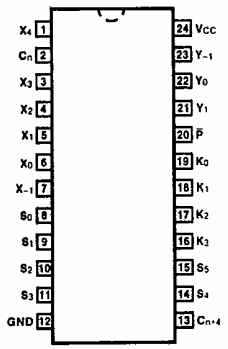
# 93S43

## 4-BIT BY 2-BIT TWOS COMPLEMENT MULTIPLIER

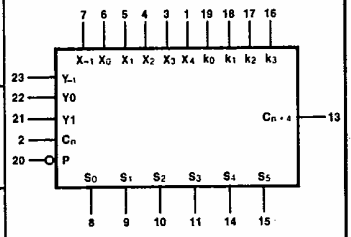
**DESCRIPTION** — The '43 is a high speed twos complement multiplier. The device is a 4-bit by 2-bit building block that can be connected in an iterative array to perform multiplication of two binary numbers of variable lengths. The device can generate the twos complement product, without correction, of two binary numbers presented in twos complement notation.

- **VERY HIGH SPEED MULTIPLICATION — TWO 12-BIT NUMBERS IN 125 ns (TYP)**
- **PROVIDES TWOS COMPLEMENT PRODUCT WITHOUT CORRECTION**
- **EXPANDS TO ANY SIZE ARRAY WITHOUT ADDITIONAL COMPONENTS**
- **ACCEPTS ACTIVE HIGH OR ACTIVE LOW OPERANDS**
- **EASILY CORRECTABLE FOR UNSIGNED, SIGN-MAGNITUDE OR ONES COMPLEMENT MULTIPLICATION**

**CONNECTION DIAGRAM**
PINOUT A




**LOGIC SYMBOL**




VCC = Pin 24
GND = Pin 12

**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE<br>VCC = +5.0 V ±5%,<br>TA = 0°C to +70°C | MILITARY GRADE<br>VCC = +5.0 V ±10%,<br>TA = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 93S43PC | | 9N |
| Ceramic DIP (D) | A | 93S43DC | 93S43DM | 6N |
| Flatpak (F) | A | 93S43FC | 93S43FM | 4M |

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

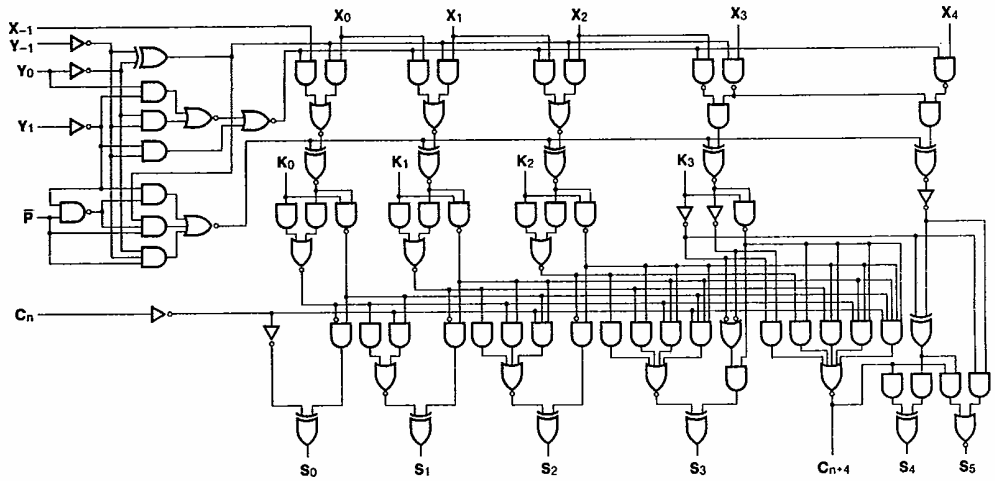
| PIN NAMES | DESCRIPTION | 93S (U.L.) HIGH/LOW |
|---|---|---|
| $X_{-1}$, $X_3$, $X_4$ | Multiplicand Inputs | 1.0/1.0 |
| $X_0$, $X_1$, $X_2$ | Multiplicand Inputs | 2.0/2.0 |
| $Y_0$ | Multiplier Input | 2.0/2.0 |
| $y_{-1}$, $y_1$ | Multiplier Inputs | 1.0/1.0 |
| $k_0$ — $k_3$ | Constant Inputs | 2.0/2.0 |
| $C_n$ | Carry Input | 1.0/1.0 |
| $\overline{P}$ | Polarity Control Input (Active LOW for HIGH Operands) | 3.0/3.0 |
| $S_0$ — $S_5$ | Product Outputs | 25/12.5 |
| $C_{n+4}$ | Carry Output | 25/12.5 |

**FUNCTIONAL DESCRIPTION** — The '43 is a super fast hardware multiplier employing Schottky technology and twos complement arithmetic. It multiplies a multiplicand of four bits by a multiplier of two bits and forms a basic iterative logic cell. It can also multiply in active HIGH (positive logic) or active LOW (negative logic) representations by reinterpreting the active levels of the inputs, outputs and the Polarity Control ($\overline{P}$). The binary number with 1 as the most significant bit is treated as a negative number represented in twos complement form. These '43 iterative logic cells can be connected to implement multiplication of an X-bit number by a Y-bit number. This application requires X • Y ÷ 4 • 2 packages and the resulting product has X + Y bits. At the beginning of the array, a constant can be presented at the K inputs that will be added to the least significant part of the product. The packages can be connected in parallel, triangular or split-array scheme depending on the speed requirement. The '41 ALU can be used with these multipliers in the split-array scheme to obtain high speed multiplication.

**TABLE I SWITCHING TEST CONDITIONS**

| INPUT | OUTPUTS | INPUTS AT 0 V (Remaining Inputs at 4.5 V) |
|---|---|---|
| $C_n$ | $C_{n+4}$, $S_0$ — $S_3$, $S_4$, $S_5$ | $\overline{P}$, $y_{-1}$, $y_1$, All x |
| $k_0$ | $C_{n+4}$, $S_0$ — $S_3$, $S_4$, $S_5$ | $\overline{P}$, $y_{-1}$, $y_1$, All x |
| $k_1$ | $C_{n+4}$, $S_1$ — $S_3$, $S_4$, $S_5$ | $\overline{P}$, $y_{-1}$, $y_1$, All x |
| $k_2$ | $C_{n+4}$, $S_2$, $S_3$, $S_4$, $S_5$ | $\overline{P}$, $y_{-1}$, $y_1$, All x |
| $k_3$ | $S_3$ | $\overline{P}$, $y_{-1}$, $y_1$, All x |
| $k_3$ | $S_4$, $S_5$ | $\overline{P}$, $y_{-1}$, $y_1$, All x, $C_n$ |
| $x_{-1}$ | $C_{n+4}$, $S_0$ — $S_3$, $S_4$, $S_5$ | $\overline{P}$, $y_1$, All k |
| $x_0$ | $C_{n+4}$, $S_0$ — $S_3$, $S_4$, $S_5$ | $\overline{P}$, $y_{-1}$, $y_1$, All k |
| $x_1$ | $C_{n+4}$, $S_1$ — $S_3$, $S_4$, $S_5$ | $\overline{P}$, $y_{-1}$, $y_1$, All k |
| $x_2$ | $C_{n+4}$, $S_2$, $S_3$, $S_4$, $S_5$ | $\overline{P}$, $y_{-1}$, $y_1$, All k |
| $x_3$, $x_4$ | $S_3$ | $\overline{P}$, $y_{-1}$, $y_1$, All k |
| $x_3$, $x_4$ | $S_4$, $S_5$ | $\overline{P}$, $y_{-1}$, $y_1$, All k, $C_n$ |
| $x_3$, $x_4$ | $S_4$, $S_5$ | $\overline{P}$, $y_{-1}$, All k, $C_n$ |
| $y_{-1}$ | $C_{n+4}$, $S_0$ — $S_3$, $S_4$, $S_5$ | $\overline{P}$, $x_1$, $x_2$, $x_3$, $x_4$, All k |
| $y_0$ | $C_{n+4}$, $S_0$ — $S_3$, $S_4$, $S_5$ | $\overline{P}$, $x_1$, $x_2$, $x_3$, $x_4$, All k |
| $y_1$ | $C_{n+4}$, $S_0$ — $S_3$, $S_4$, $S_5$ | $x_0$, $x_1$, $x_2$, $x_3$, $x_4$, All k |

**LOGIC DIAGRAM**



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL | PARAMETER | 93S | | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $I_{CC}$ | Power Supply Current | | 149 | mA | $V_{CC}$ = Max |

**AC CHARACTERISTICS:** $V_{CC}$ = +5.0 V, $T_A$ = +25° C (See Section 3 for waveforms and load configurations)

| SYMBOL | PARAMETER | 93S $C_L$ = 15 pF | | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$C_n$ to $C_{n+4}$ | | 9.0<br>9.0 | ns | Figs. 3-1, 3-5 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$C_n$ to $S_0 - S_3$ | | 13<br>11 | ns | Figs. 3-1, 3-4 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$C_n$ to $S_4$, $S_5$ | | 16<br>15 | ns | Figs. 3-1, 3'4 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$k_n$ to $C_{n+4}$ | | 12<br>13 | ns | Figs. 3-1, 3-5 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$k_n$ to $S_0 - S_3$ | | 14<br>12 | ns | Figs. 3-1, 3-5 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$k_n$ to $S_4$, $S_5$ | | 19<br>17 | ns | Figs. 3-1, 3-4 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$x_n$ to $C_{n+4}$ | | 15<br>24 | ns | Figs. 3-1, 3-5 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$x_n$ to $S_0 - S_3$ | | 25<br>25 | ns | Figs. 3-1, 3-4 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$x_n$ to $S_4$, $S_5$ | | 30<br>21 | ns | Figs. 3-1, 3-4 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$y_n$ to $C_{n+4}$ | | 25<br>27 | ns | Figs. 3-1, 3-5 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$y_n$ to $S_0 - S_3$ | | 28<br>27 | ns | Figs. 3-1, 3-4 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$y_n$ to $S_4$, $S_5$ | | 32<br>30 | ns | Figs. 3-1, 3-4 |