

1. General Description

This ROM-Based 8-bit micro-controller uses a fully static CMOS design technology combines higher speed and smaller size with the low power and high noise immunity of CMOS.

On chip memory system includes 2.0 K bytes of ROM, and 80 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software :

- ◆ Fully CMOS static design
- ◆ 8-bit data bus
- ◆ On chip ROM size : 2.0 K words
- ◆ Internal RAM size : 80 bytes (73 general purpose registers, 7 special registers)
- ◆ 34 single word instructions
- ◆ 12-bit instructions
- ◆ 2-level stacks
- ◆ Operating voltage : 2.3 V ~ 6.3 V
- ◆ Operating frequency : 0 ~ 20 MHz
- ◆ The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- ◆ Addressing modes include direct, indirect and relative addressing modes
- ◆ Power-on Reset
- ◆ Power edge-detector Reset
- ◆ Sleep Mode for power saving
- ◆ 4 oscillator start-up time :
150 μ s, 20 ms, 40 ms, 80 ms
- ◆ 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- ◆ 4 types of oscillator can be selected by code options :
 - RC—Low cost RC oscillator
 - LFXT—Low frequency crystal oscillator
 - XTAL—Standard crystal oscillator
 - HFXT—High frequency crystal oscillator
- ◆ On-chip RC oscillator based Watchdog Timer(WDT) can be operated freely
- ◆ Pull up resistors for the following pins :
PA0~PA3, PB0~PB7, /MCLR, RTCC
- ◆ Pull down resistors for the following pins :
PA0~PA3, PB0~PB7, RTCC
- ◆ 12 I/O pins with their own independent direction control

3. Applications

The application areas of this MDT1030 range from appliance motor control and high speed automotive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral ... etc.

4. Pin Assignment

PA2	1	18	PA1
PA3	2	17	PA0
RTCC	3	16	OSC1
/MCLR	4	15	OSC2
V _{ss}	5	14	V _{dd}
PB0	6	13	PB7
PB1	7	12	PB6
PB2	8	11	PB5
PB3	9	10	PB4

5. Pin Function Description

Pin Name	I/O	Function Description
PA0~PA3	I/O	Port A, TTL input level
PB0~PB7	I/O	Port B, TTL input level
RTCC	I	Real Time Clock/Counter, Schmitt Trigger input levels
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
V _{dd}		Power supply
V _{ss}		Ground

6. Memory Map

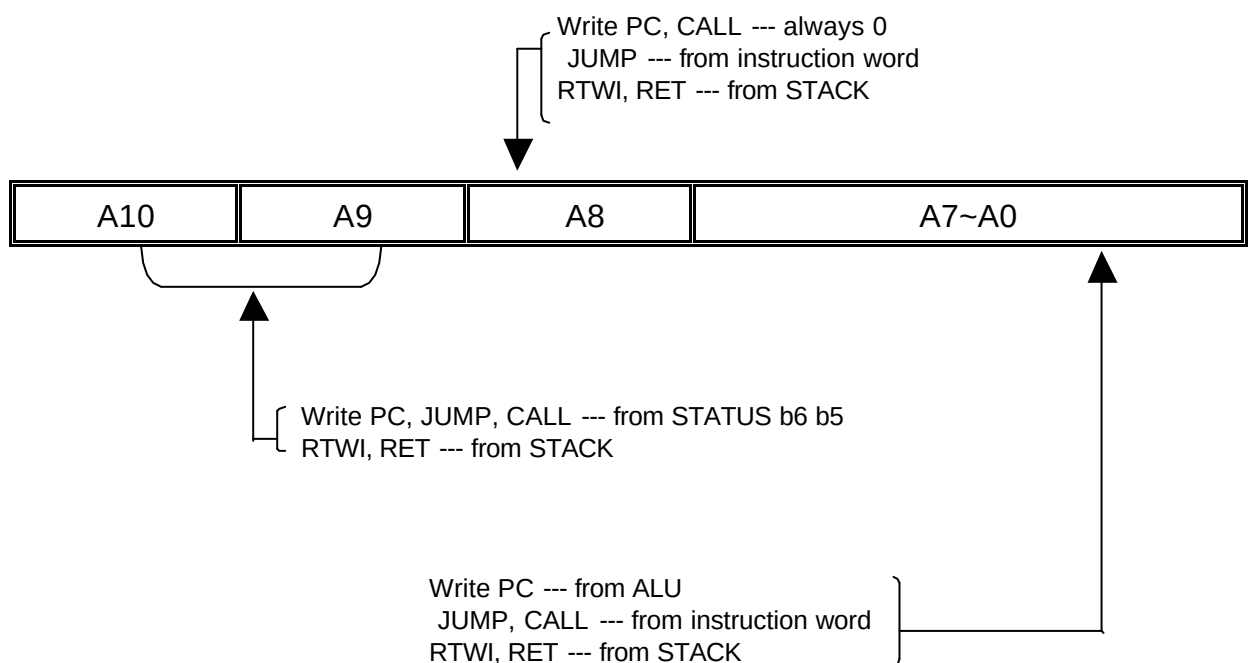
(A) Register Map

Address	Description
00	Indirect Addressing Register
01	RTCC
02	PC
03	STATUS
04	MSR
05	Port A
06	Port B
07~0F	Internal RAM, General Purpose Register
10~1F	Internal Memory Select Register
30~3F	Internal Memory Select Register
50~5F	Internal Memory Select Register
70~7F	Internal Memory Select Register

(1) IAR (Indirect Address Register) : R0

(2) RTCC (Real Time Counter/Counter Register) : R1

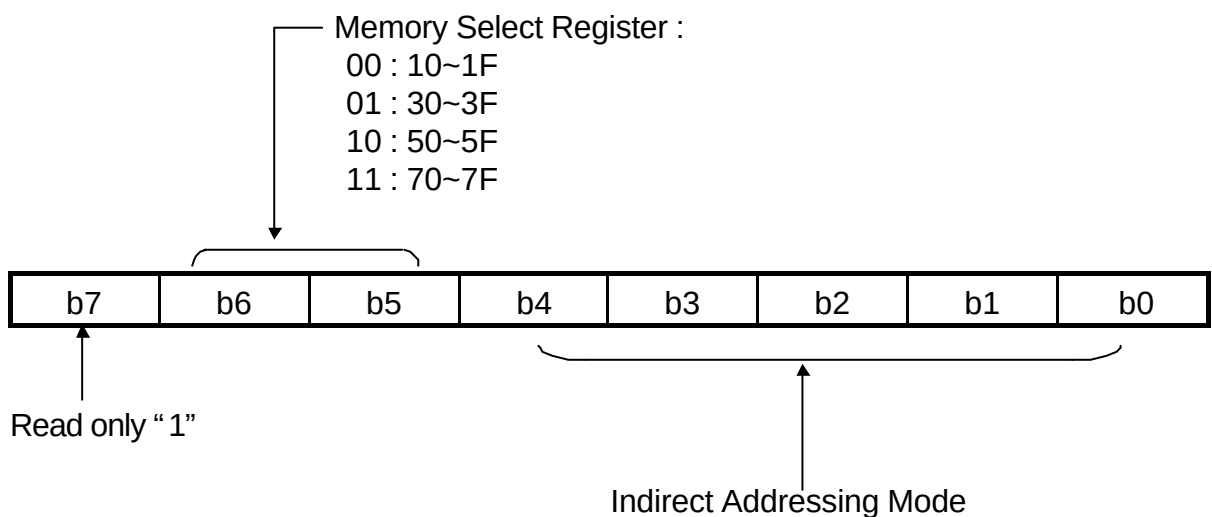
(3) PC (Program Counter) : R2



(4) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power loss Flag bit
4	TF	Time overflow Flag bit
6—5	page	Page select bit : 00 : 000H --- 1FFH 01 : 200H --- 3FFH 10 : 400H --- 5FFH 11 : 600H --- 7FFH
7	—	General purpose bit

(5) MSR (Memory Select Register) : R4



(6) PORT A : R5

PA3~PA0, I/O Register

(7) PORT B : R6

PB7~PB0, I/O Register

(8) TMR (Time Mode Register)

Bit	Symbol	Function		
2—0	PS2—0	Prescaler Value	RTCC rate	WDT rate
		0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin		

(9) CPIO A, CPIO B (Control Port I/O Mode Register)

The CPIO register is "write-only"

= "0", I/O pin in output mode;

= "1", I/O pin in input mode.

(10) Configuration ROM :

Bit 1	Bit 0	Oscillator Type
0	0	RC Oscillator
0	1	LFXT Oscillator
1	0	XTAL Oscillator
1	1	HFXT Oscillator

Bit 3	Bit 2	Oscillator Start-up Time
0	0	150 μ s
0	1	20 ms
1	0	40 ms
1	1	80 ms

Bit 4	Watchdog Timer control
0	Watchdog timer disable all the time
1	Watchdog timer enable all the time

(B) Program Memory

Address	Description
000-7FF	Program memory
7FF	The starting address of the power on, external reset or WDT

7. Reset Condition for all Registers

Register	Address	Power-On Reset	/MCLR or WDT Reset
CPIO A	--	1111 1111	1111 1111
CPIO B	--	1111 1111	1111 1111
TMR	--	--11 1111	--11 1111
IAR	00h	—	—
RTCC	01h	xxxx xxxx	uuuu uuuu
PC	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000# #uuu
MSR	04h	111x xxxx	111u uuuu
PORT A	05h	---- xxxx	---- uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu

Note : u=unchanged, x=unknown, - =unimplemented, read as "0"
 # =value depends on the condition of the following table

Condition	Status: bit 4	Status: bit 3
/MCLR reset (not during SLEEP)	u	u
/MCLR reset during SLEEP	1	0
WDT reset (not during SLEEP)	0	1
WDT reset during SLEEP	0	0

8. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 000000	NOP	No operation	None	
010000 000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 000100	RET	Return	Stack→PC	None
010000 000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrr	STWR R	Store W to register	W→R	None
011000 trrrrr	LDR R, t	Load register	R→t	Z
1110ii iiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔ R(4~7)]→t	None
011001 trrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrr	SUBWR R, t	Subtract W from register	R - W→t (R+W+1→t)	C, HC, Z
011101 trrrrr	DECR R, t	Decrement register	R - 1→t	Z
011110 trrrrr	DECRSZ R, t	Decrement register, skip if zero	R - 1→t	None
010010 trrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
1101ii iiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
1111 iiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
1011 iiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrr	RRR R, t	Rotate right register	R(n)→R(n-1), C→R(7), R(0)→C	C
010101 trrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrr	CLRR R	Clear register	0→R	Z

This specification are subject to be changed without notice. Any latest information please preview

Instruction Code	Mnemonic Operands	Function	Operating	Status
0000bb brrrrr	BCR R, b	Bit clear	$0 \rightarrow R(b)$	None
0010bb brrrrr	BSR R, b	Bit set	$1 \rightarrow R(b)$	None
0001bb brrrrr	BTSC R, b	Bit Test, skip if clear	Skip if $R(b)=0$	None
0011bb brrrrr	BTSS R, b	Bit Test, skip if set	Skip if $R(b)=1$	None
1100 nnnnnnnn	CALL n	Call subroutine	$n \rightarrow PC$, $PC+1 \rightarrow \text{Stack}$	None
1010ii iiiiii	RTWI i	Return, place immediate to W	$\text{Stack} \rightarrow PC$, $i \rightarrow W$	None
100n nnnnnnnn	JUMP n	JUMP to address	$n \rightarrow PC$	None

Note :

W	: Working register	b	: Bit position
WT	: Watchdog timer	t	: Target
TMODE	: TMODE mode register	0	: Working register
CPIO	: Control I/O port register	1	: General register
TF	: Timer overflow flag	R	: General register address
PF	: Power loss flag	C	: Carry flag
PC	: Program Counter	HC	: Half carry
OSC	: Oscillator	Z	: Zero flag
Inclu.	: Inclusive 'U'	/	: Complement
Exclu.	: Exclusive '⊕'	x	: Don't care
AND	: Logic AND '∩'	i	: Immediate data (8 bits)
		n	: Immediate address

9. Electrical Characteristics

(A) Operating Voltage & Frequency

V_{dd} : 2.3 V ~ 6.3 V

Frequency : 0 Hz ~ 20 MHz

(B) Input Voltage :

@ $V_{dd}=5.0$ V, Temperature = 25 °C

	Port	Min.	Max.
V_{il}	PA, PB	V_{ss}	1.0 V
	RTCC, /MCLR	V_{ss}	0.8 V
V_{ih}	PA, PB	2.0 V	V_{dd}
	RTCC, /MCLR	3.4 V	V_{dd}

***Threshold Voltage :**

This specification are subject to be changed without notice. Any latest information please preview

Port A, Port B $V_{th} = 1.56 \text{ V}$

RTCC, /MCLR $V_{il} = 1.4 \text{ V}$, $V_{ih} = 2.9 \text{ V}$ (Schmitt Trigger)

(C) Output Voltage :

@ $V_{dd} = 5.0 \text{ V}$, Temperature = 25°C , the typical value as followings :

PA, PB Port	
$I_{oh} = -20.0 \text{ mA}$	$V_{oh} = 3.50 \text{ V}$
$I_{ol} = 20.0 \text{ mA}$	$V_{ol} = 0.44 \text{ V}$
$I_{oh} = -5.0 \text{ mA}$	$V_{oh} = 4.70 \text{ V}$
$I_{ol} = 5.0 \text{ mA}$	$V_{ol} = 0.20 \text{ V}$

(D) Leakage Current

@ $V_{dd} = 5.0 \text{ V}$, Temperature = 25°C , the typical value as followings :

I_{il}	$- 1.0 \mu\text{A (Max.)}$
I_{ih}	$+ 1.0 \mu\text{A (Max.)}$

(E) Sleep Current

@WDT—Disable, Temperature = 25°C

$V_{dd} = 2.3 \sim 6.3 \text{ V}$, $I_{dd} < 1.0 \mu\text{A}$

@WDT—Enable, Temperature = 25°C , the typical value as followings :

$V_{dd} = 2.3 \text{ V}$	$I_{dd} < 1.0 \mu\text{A}$
$V_{dd} = 3.0 \text{ V}$	$I_{dd} = 2.0 \mu\text{A}$
$V_{dd} = 4.0 \text{ V}$	$I_{dd} = 5.0 \mu\text{A}$
$V_{dd} = 5.0 \text{ V}$	$I_{dd} = 12.0 \mu\text{A}$
$V_{dd} = 6.3 \text{ V}$	$I_{dd} = 20.0 \mu\text{A}$

(F) Operating Current / Voltage

Temperature = 25°C , the typical value as followings :

(i) OSC Type=RC ; WDT—Enable; @ $V_{dd}=5.0\text{ V}$

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
3P	4.7 K	12.4 M	1.9 m
	10.0 K	7.0 M	1.1 m
	47.0 K	1.7 M	310.0 μ
	100.0 K	842.0 K	180.0 μ
	300.0 K	282.5 K	90.0 μ
	470.0 K	180.0 K	75.0 μ
20P	4.7 K	5.40 M	900.0 μ
	10.0 K	2.80 M	500.0 μ
	47.0 K	666.6 K	150.0 μ
	100.0 K	318.2 K	100.0 μ
	300.0 K	106.5 K	70.0 μ
	470.0 K	68.8 K	60.0 μ
100P	4.7 K	1.66 M	320.0 μ
	10.0 K	851.0 K	180.0 μ
	47.0 K	193.5 K	80.0 μ
	100.0 K	92.6 K	65.0 μ
	300.0 K	29.8 K	60.0 μ
	470.0 K	18.7 K	55.0 μ
300P	4.7 K	695.0 K	160.0 μ
	10.0 K	350.0 K	105.0 μ
	47.0 K	79.1 K	65.0 μ
	100.0 K	35.5 K	60.0 μ
	300.0 K	11.9 K	55.0 μ
	470.0 K	7.5 K	53.0 μ

(ii) OSC Type=LF (C=20 p); WDT—Enable

Voltage/Frequency	32 K	455 K	1 M	Sleep
2.3 V	4.0 μ A	X	X	<1.0 μ A
3.0 V	8.0 μ A	50.0 μ A	85.0 μ A	2.0 μ A
4.0 V	17.0 μ A	70.0 μ A	140.0 μ A	4.0 μ A
5.0 V	30.0 μ A	110.0 μ A	200.0 μ A	12.0 μ A
6.3 V	58.0 μ A	160.0 μ A	290.0 μ A	20.0 μ A

(iii) OSC Type=XT (C=10 p); WDT—Enable

Voltage/Frequency	1 M	4 M	10 M	Sleep
2.1 V	65.0 μ A	220.0 μ A	490.00 μ A	<1.0 μ A
3.0 V	120.0 μ A	365.0 μ A	800.00 μ A	2.0 μ A
4.0 V	210.0 μ A	550.0 μ A	1.20 mA	4.0 μ A
5.0 V	330.0 μ A	750.0 μ A	1.70 mA	12.0 μ A
6.3 V	530.0 μ A	1.2 mA	2.40 mA	20.0 μ A

(iv) OSC Type=HF (C=10 p); WDT—Enable

Voltage/Frequency	4 M	10 M	20 M	Sleep
2.1 V	220.0 μ A	560.00 μ A	950.00 μ A	<1.0 μ A
3.0 V	400.0 μ A	900.00 μ A	1.50 mA	2.0 μ A
4.0 V	640.0 μ A	1.60 mA	2.60 mA	4.0 μ A
5.0 V	900.0 μ A	2.40 mA	3.70 mA	12.0 μ A
6.3 V	1.4 mA	3.60 mA	5.50 mA	20.0 μ A

(G) Pull Resistance

@ Input Mode : $V_{dd}=3.0$ V

PORT	Pull-High Resistance	$R_{hi}=330.0$ KOhm
	Pull-Low Resistance	$R_{lo}=330.0$ KOhm
RTCC	Pull-High Resistance	$R_{hi}=300.0$ KOhm
	Pull-Low Resistance	$R_{lo}=300.0$ KOhm
/MCLR	Pull-High Resistance	$R_{hi}=300.0$ KOhm

@ Input Mode : $V_{dd} = 5.0 \text{ V}$

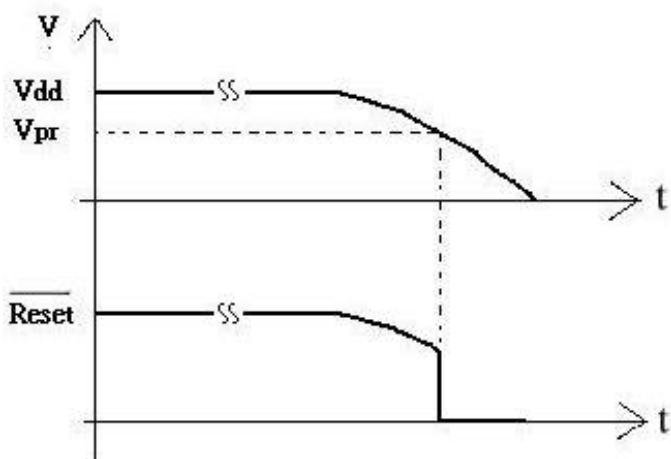
PORT	Pull-High	Resistance	$R_{hi} = 160.0 \text{ KOhm}$
	Pull-Low	Resistance	$R_{lo} = 160.0 \text{ KOhm}$
RTCC	Pull-High	Resistance	$R_{hi} = 150.0 \text{ KOhm}$
	Pull-Low	Resistance	$R_{lo} = 150.0 \text{ KOhm}$
/MCLR	Pull-High	Resistance	$R_{hi} = 150.0 \text{ KOhm}$

p.s. : It is only a reference value for the Pull High/Low Resistance, and the accurate value of the Resistance depends on the various parameter of the Process. But the variation of the value will be not more than 20%.

(H) Power Edge-detector Reset Voltage, @ $V_{dd} = 5.0 \text{ V}$

$$V_{pr} \leq 1.1 \sim 1.3 \text{ V}$$

V_{pr} : V_{dd} (Power Supply)



The Power Edge-detector function can be chosen as either “Enable” or “Disable” :

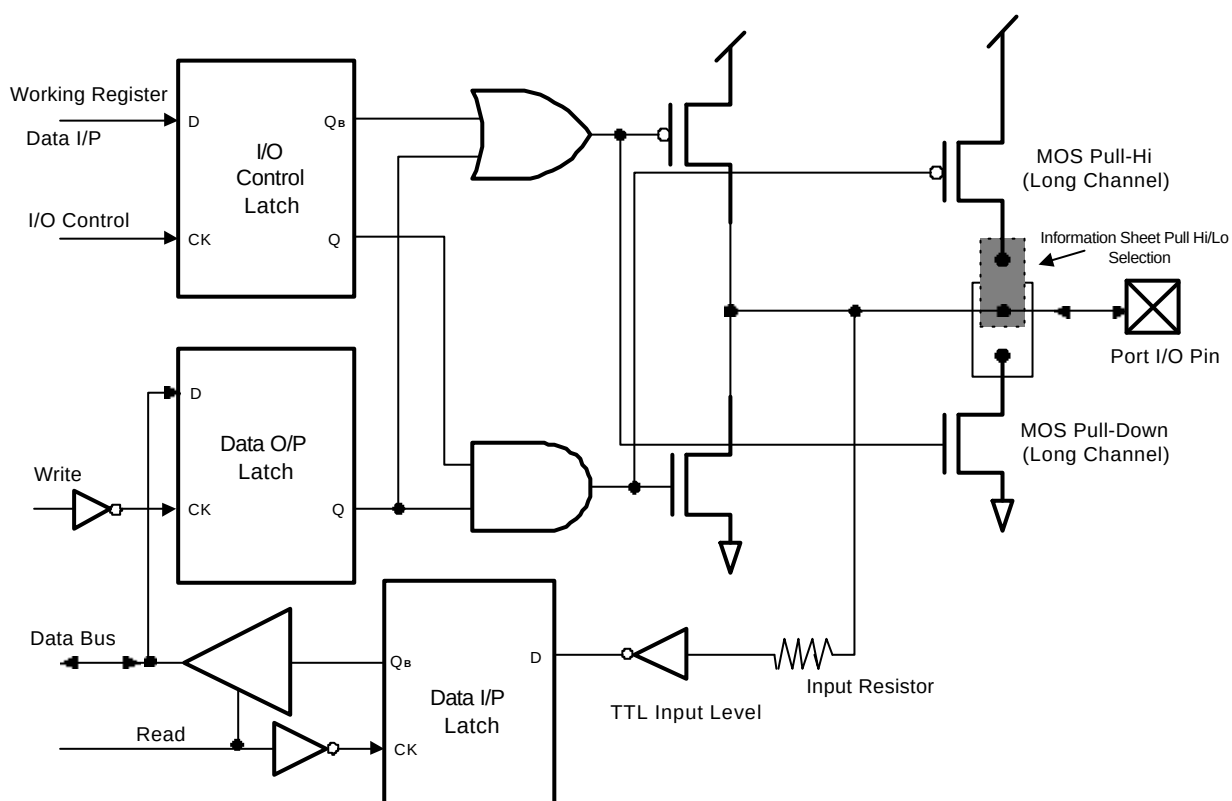
- (i) “Disable” condition : No Power EDT function.
- (ii) “Enable” condition : Under operation condition(Not in Sleep Mode), if the operating voltage(V_{pr}) was not dropped down smoothly, then, $1.1 \text{ V} \leq V_{pr} \leq 2.0 \text{ V}$, the IC will be reset.

(I) The basic WDT time-out cycle time

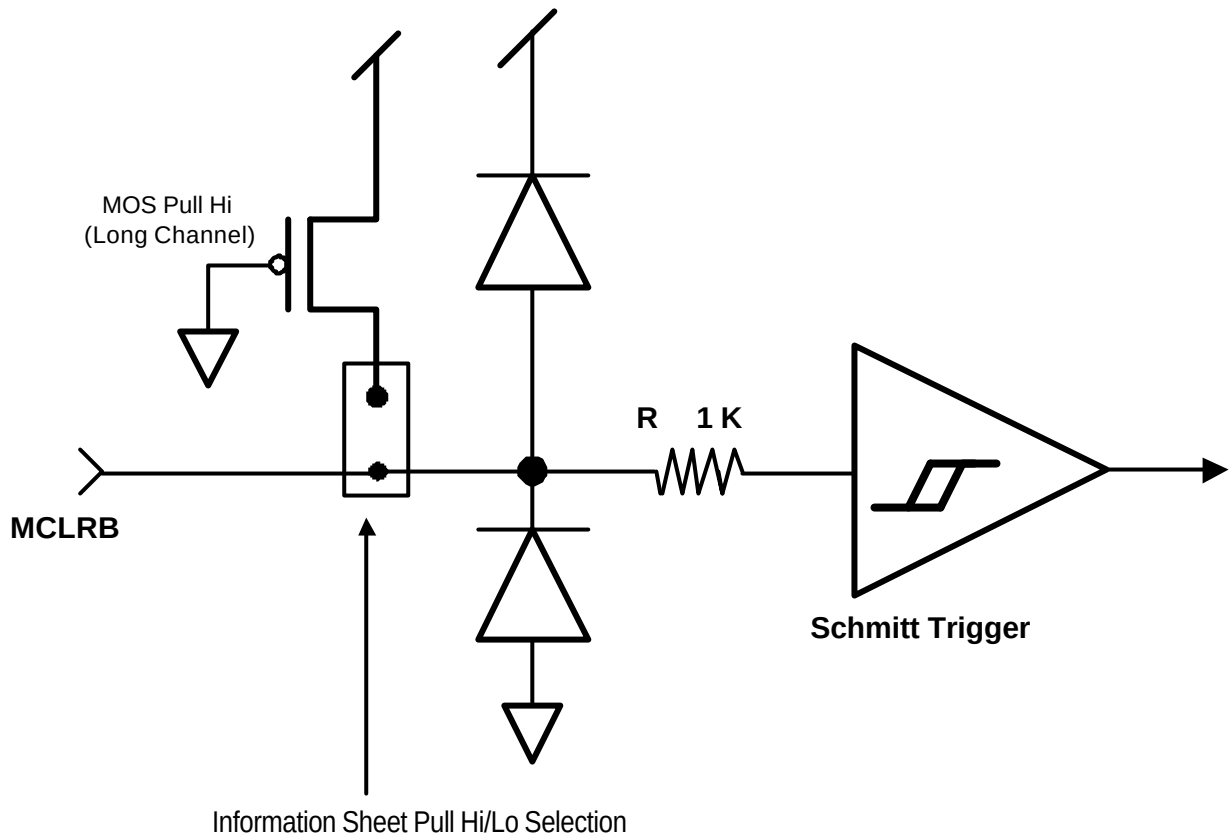
Temperature = 25 °C, the typical value as followings :

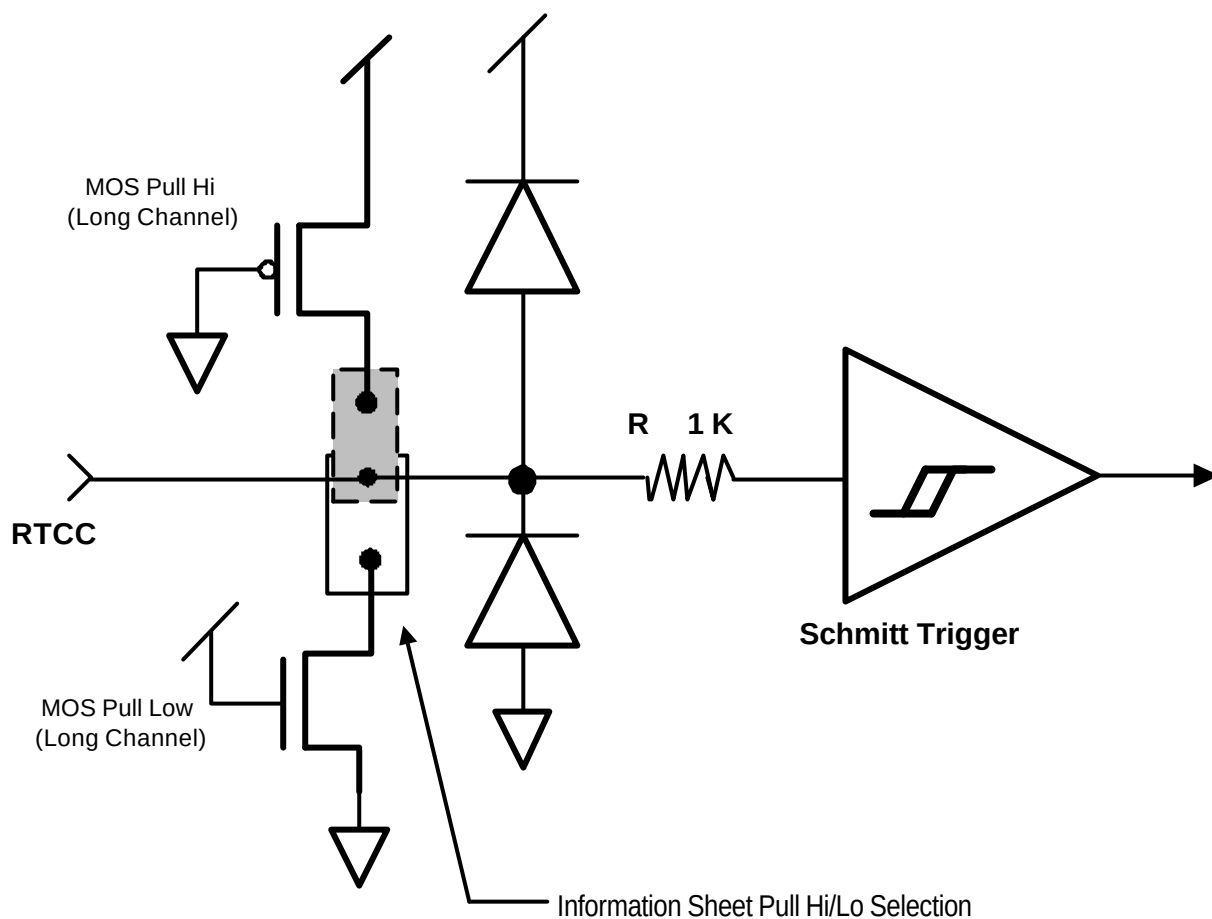
Voltage (V)	Basic WDT time-out cycle time (ms)
2.3	28.90
3.0	25.60
4.0	22.30
5.0	20.00
6.3	18.10

10. Port A and Port B Equivalent Circuit

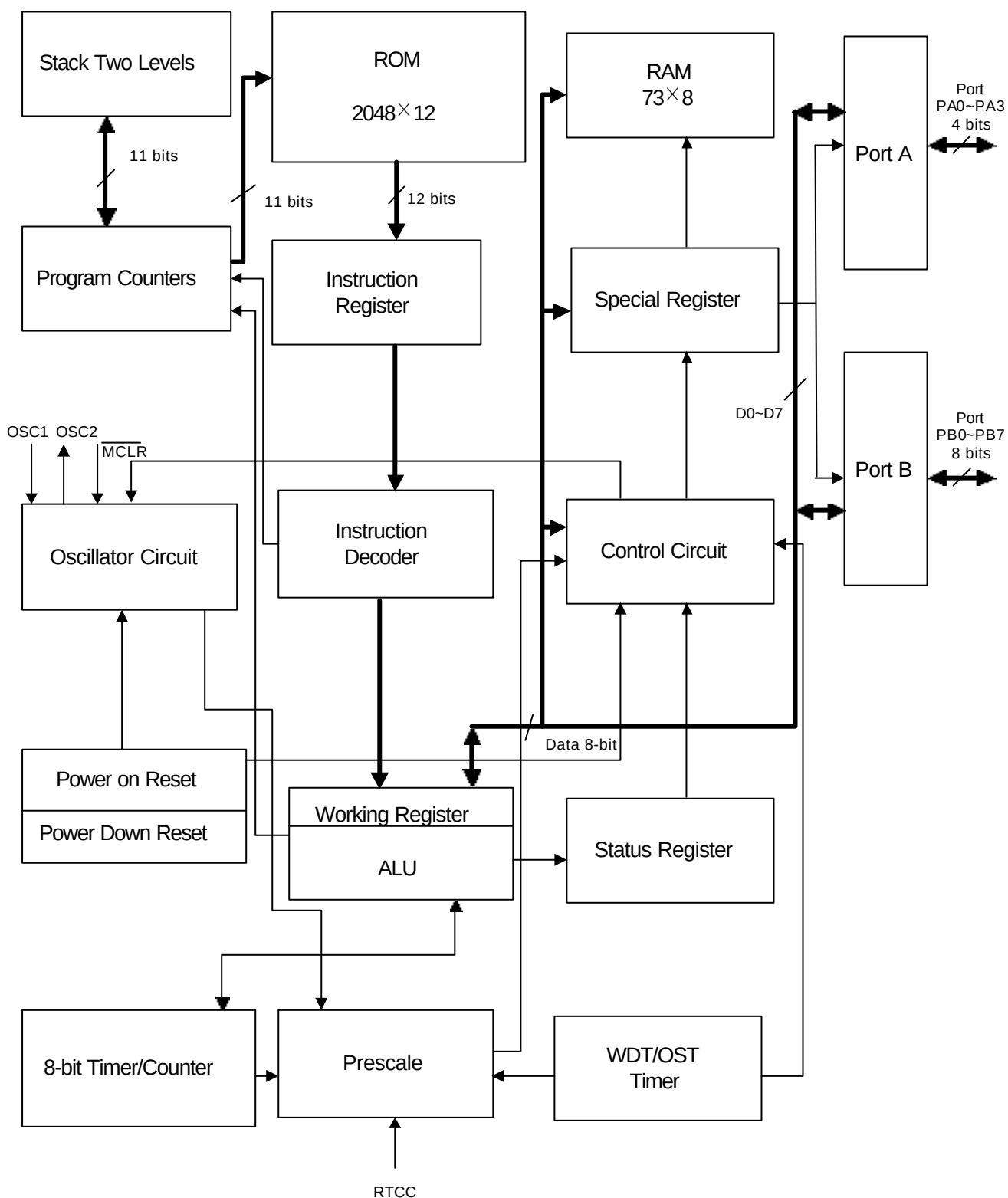


11. MCLRB and RTCC Input Equivalent Circuit





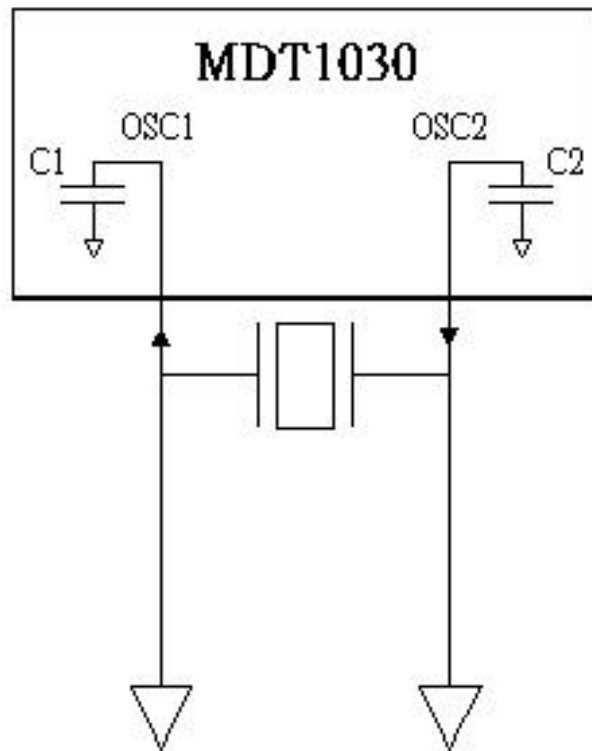
12. Block Diagram



13. Capacitor Selection For Crystal Oscillator

(a) With built-in Oscillation Capacitors (Default for HF,XT,LF)

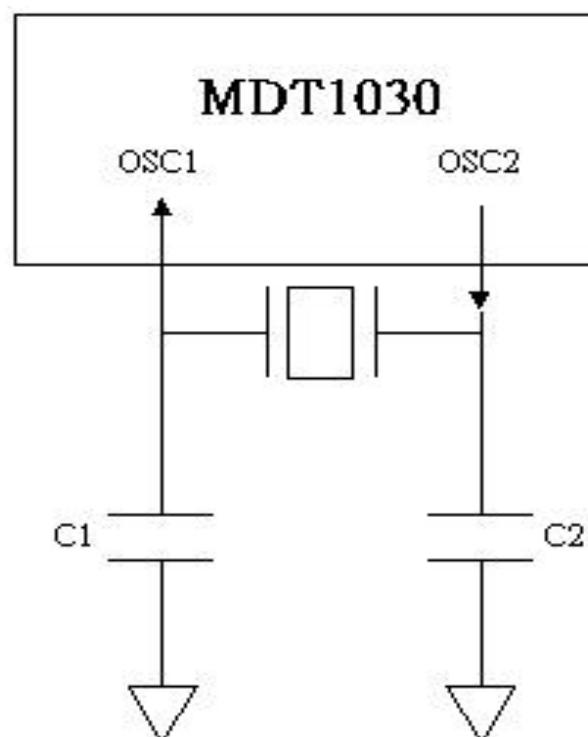
@ $V_{dd} = 2.3V \sim 5.5V$, $C1 = C2 = 10P \sim 15P$



(b) Without built-in Oscillation Capacitors

@ $V_{dd} = 3.0\text{ V} \sim 5.0\text{ V}$

Osc. Type	Resonator Freq.	C1	C2
HF	20 MHz	5 pF ~10 pF	10 pF~30 pF
	10 MHz	10 pF ~50 pF	20 pF ~100 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
XT	10 MHz	10 pF ~30 pF	10 pF ~50 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
	1 MHz	10 pF ~30 pF	20 pF ~50 pF
LF	1 MHz	3 pF ~5 pF	3 pF ~5 pF
	455 K	10 pF ~30 pF	20 pF ~50 pF
	32 K	10 pF ~20 pF	15 pF ~30 pF



To increase the stability of oscillator and the ability of anti-noise, the above values of the external capacitor range are recommended, but the higher capacitance will increase the start-up time.

There do not have built-in Oscillation Capacitors for RC type.

