

RF LDMOS Wideband Integrated Power Amplifiers

The MDE6IC9120N/GN wideband integrated circuit is designed with on-chip matching that makes it usable from 920 to 960 MHz. This multi-stage structure is rated for 26 to 32 Volt operation and covers all typical cellular base station modulation formats.

- Typical Doherty Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQ1A} = I_{DQ1B} = 90$ mA, $I_{DQ2A} = 550$ mA, $V_{G2B} = 1.6$ Vdc, $P_{out} = 25$ Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)
920 MHz	32.5	38.4	6.6	-39.0
940 MHz	32.0	38.0	6.7	-40.4
960 MHz	31.3	37.7	7.0	-39.6

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 940 MHz, 146 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out}), Designed for Enhanced Ruggedness
- Stable into a 5:1 VSWR. All Spurs Below -60 dBc @ 100 mW to 120 Watts CW P_{out}
- Typical P_{out} @ 1 dB Compression Point $\approx$ 120 Watts CW

Features

- Production Tested in a Symmetrical Doherty Configuration
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel

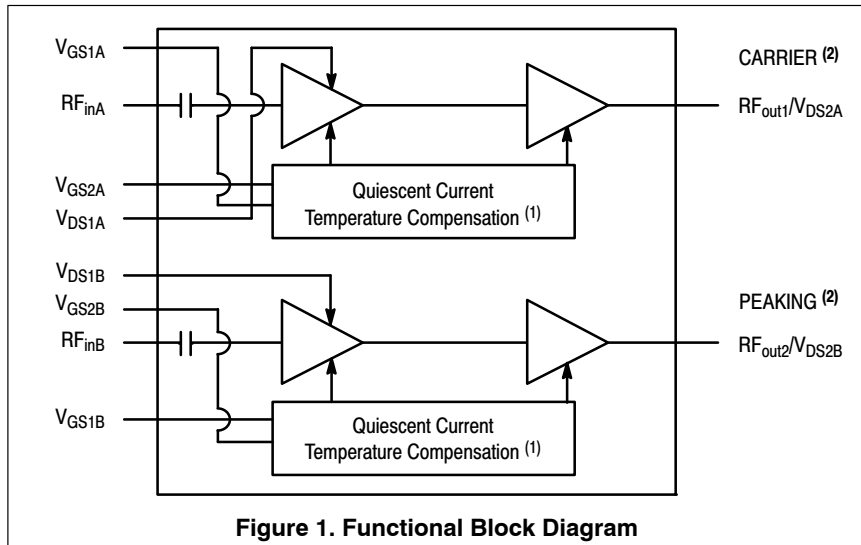


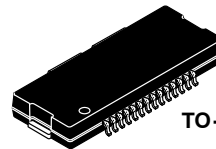
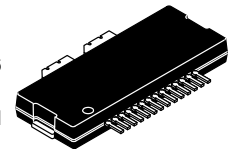
Figure 1. Functional Block Diagram

- Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.
- Peaking and Carrier orientation is determined by the test fixture design.

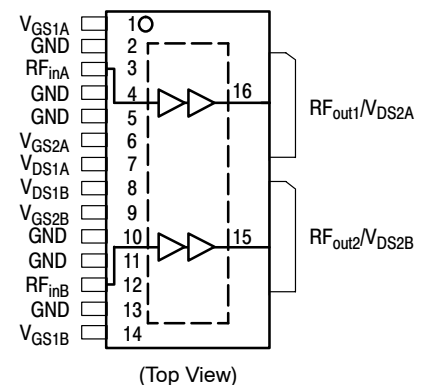
MDE6IC9120NR1 MDE6IC9120GNR1

**920-960 MHz, 25 W AVG., 28 V
SINGLE W-CDMA
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS**

**CASE 1866-02
TO-270 WBL-16
PLASTIC
MDE6IC9120NR1**



**CASE 1867-02
TO-270 WBL-16 GULL
PLASTIC
MDE6IC9120GNR1**



Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +66	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
Input Power	P_{in}	30	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
----------------	--------	-------------	------

Final Doherty Application

Thermal Resistance, Junction to Case Case Temperature 80°C, $P_{out} = 30$ W CW Stage 1A, 27 Vdc, $I_{DQ1A} = 90$ mA Stage 1B, 27 Vdc, $I_{DQ1B} = 90$ mA Stage 2A, 27 Vdc, $I_{DQ2A} = 550$ mA Stage 2B, 27 Vdc, $V_{G2B} = 2.5$ Vdc	$R_{\theta JC}$	6.0 4.9 1.3 0.95	°C/W
--	-----------------	---------------------------	------

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 — Off Characteristics ⁽¹⁾					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 66\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 1.5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
Stage 1 — On Characteristics ⁽¹⁾					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 20\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	1	1.7	3	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_{DQ1A} = I_{DQ1B} = 90\text{ mA}$)	$V_{GS(Q)}$	—	2.5	—	Vdc
Fixture Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_{DQ1A} = I_{DQ1B} = 90\text{ mA}$, Measured in Functional Test)	$V_{GG(Q)}$	7.4	8.1	8.8	Vdc
Stage 2 — Off Characteristics ⁽¹⁾					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 66\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 1.5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
Stage 2 — On Characteristics ⁽¹⁾					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 160\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	1	1.7	3	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_{DQ2A} = 550\text{ mA}$)	$V_{GS(Q)}$	—	2.1	—	Vdc
Fixture Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_{DQ2A} = 550\text{ mA}$, Measured in Functional Test)	$V_{GG(Q)}$	5.8	6.5	7.2	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 407\text{ mA}$)	$V_{DS(on)}$	0.15	0.3	0.8	Vdc
Functional Tests ^(2,3,4) (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ1A} = I_{DQ1B} = 90\text{ mA}$, $I_{DQ2A} = 550\text{ mA}$, $V_{G2B} = 1.6\text{ Vdc}$, $P_{out} = 25\text{ W Avg.}$, $f = 940\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	G_{ps}	30.0	32.0	36.0	dB
Power Added Efficiency	PAE	36.0	38.0	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.8	6.7	—	dB
Adjacent Channel Power Ratio	ACPR	—	-40.4	-36.0	dBc
Typical Broadband Performance ⁽³⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ1A} = I_{DQ1B} = 90\text{ mA}$, $I_{DQ2A} = 550\text{ mA}$, $V_{G2B} = 1.6\text{ Vdc}$, $P_{out} = 25\text{ W Avg.}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset					
Frequency	G_{ps} (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)	
920 MHz	32.5	38.4	6.6	-39.0	
940 MHz	32.0	38.0	6.7	-40.4	
960 MHz	31.3	37.7	7.0	-39.6	

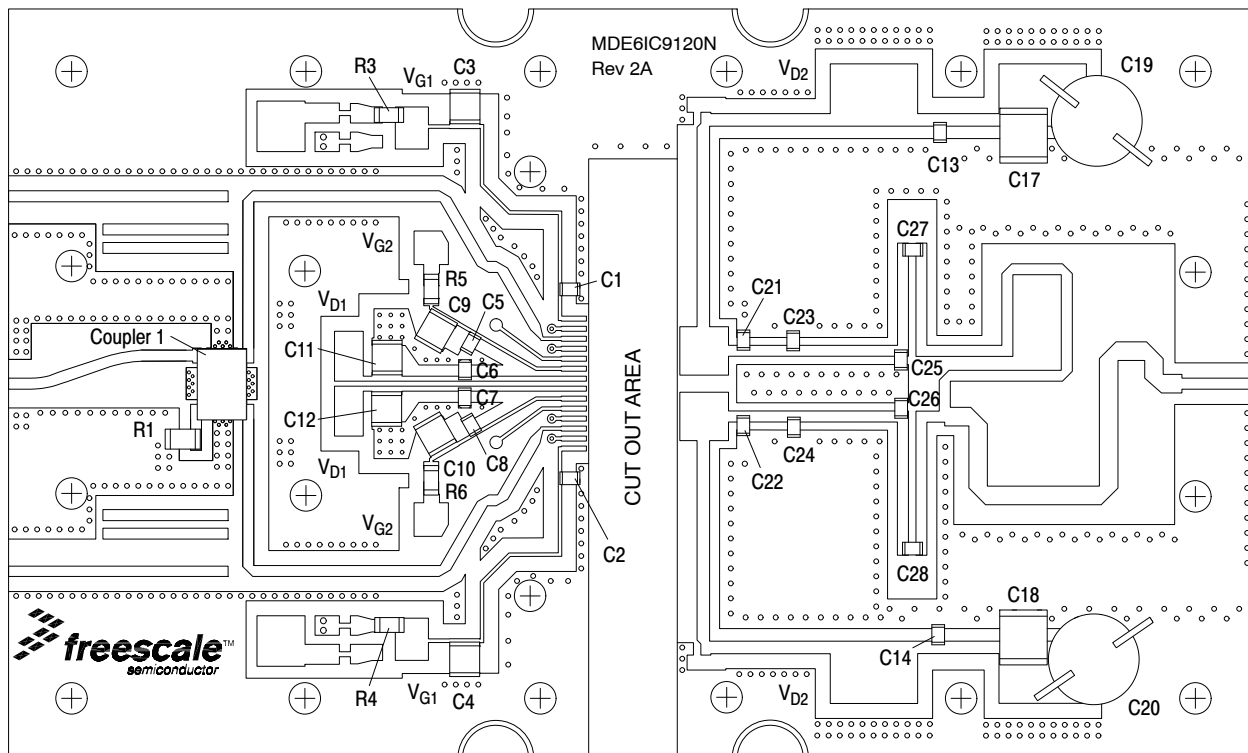
- Each side of device measured separately.
- Part internally matched both on input and output.
- Measurement made with device in a Symmetrical Doherty configuration.
- Measurement made with device in straight lead configuration before any lead forming operation is applied.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances ⁽¹⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ1A} = I_{DQ1B} = 90\text{ mA}$, $I_{DQ2A} = 550\text{ mA}$, $V_{G2B} = 1.6\text{ Vdc}$, 920-960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	120	—	W
IMD Symmetry @ 90 W PEP, P_{out} where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD _{sym}	—	8	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW _{res}	—	50	—	MHz
Quiescent Current Accuracy over Temperature ⁽²⁾ with 4.3 k Ω Gate Feed Resistors (-30 to 85°C)	ΔI_{QT}	—	0.02 0.03	—	%
Gain Flatness in 40 MHz Bandwidth @ $P_{out} = 25\text{ W Avg.}$	G_F	—	1.2	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.04	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1dB$	—	0.02	—	dBm/°C

1. Measurement made with device in a Symmetrical Doherty configuration.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.



Note: Component numbers C15, C16 and R2 are not used.

Figure 3. MDE6IC9120NR1(GNR1) Test Circuit Component Layout

Table 6. MDE6IC9120NR1(GNR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C5, C6, C7, C8	0.01 μ F, 50 V Chip Capacitors	GCM2195C1H103JA16D	Murata
C3, C4, C9, C10, C11, C12	1.0 μ F, 35 V Chip Capacitors	GRM32RR71H105KA01K	Murata
C13, C14, C27, C28	39.0 pF Chip Capacitors	ATC600F390JT250XT	ATC
C17, C18	10.0 μ F, 35 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C19, C20	220 μ F, 50 V Electrolytic Capacitors	EMVY500ADA221MJA0G	Nippon Chemi-Con
C21, C22	15.0 pF Chip Capacitors	ATC600F150GT250XT	ATC
C23, C24	1.6 pF Chip Capacitors	ATC600F1R6JT250XT	ATC
C25, C26	2.7 pF Chip Capacitors	ATC600F2R7JT250XT	ATC
Coupler 1	50 Ω , 3 dB Hybrid Coupler	GSC362-HYB0900	Soshin
R1	50 Ω , 10 W Termination	RFP-060120A15Z50-2	Anaren
R3, R4, R5, R6	4.3 K Ω , 1/4 W Chip Resistors	CRCW12064K30FKEA	Vishay
PCB	0.020", $\epsilon_r = 3.50$	RO4350B	Rogers

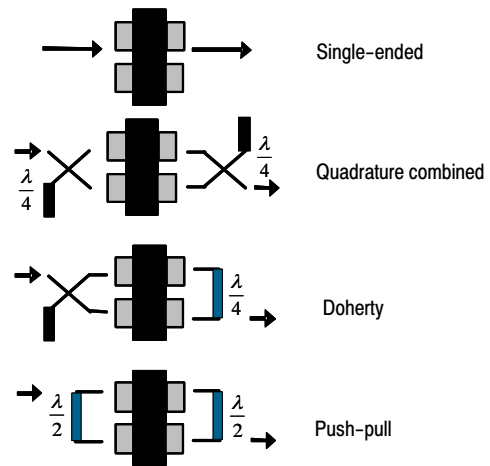


Figure 4. Possible Circuit Topologies

TYPICAL CHARACTERISTICS

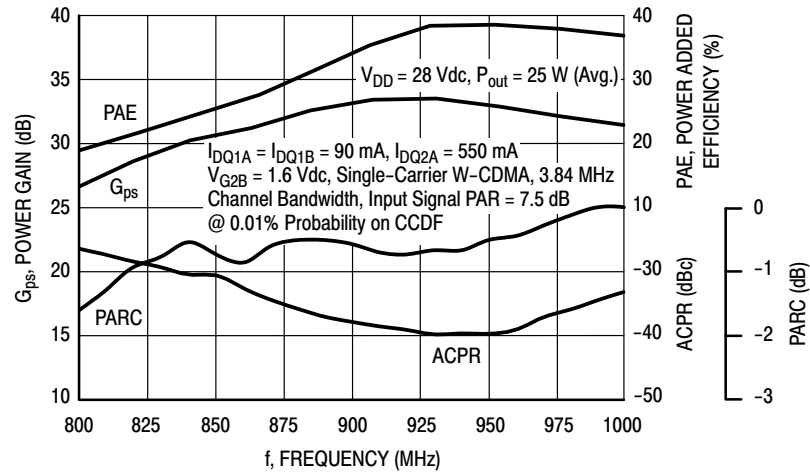


Figure 5. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 25$ Watts Avg.

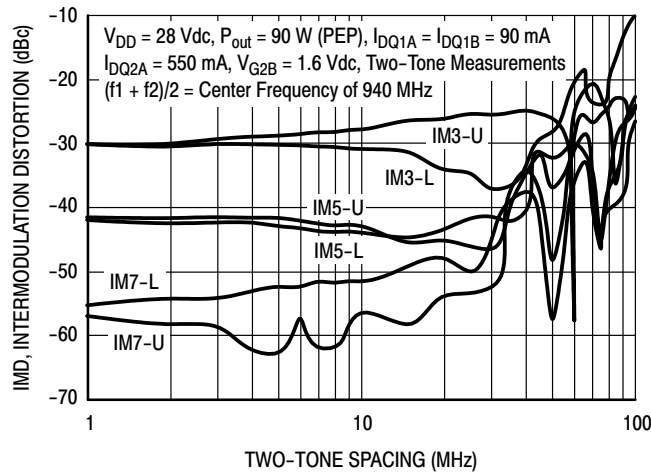


Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing

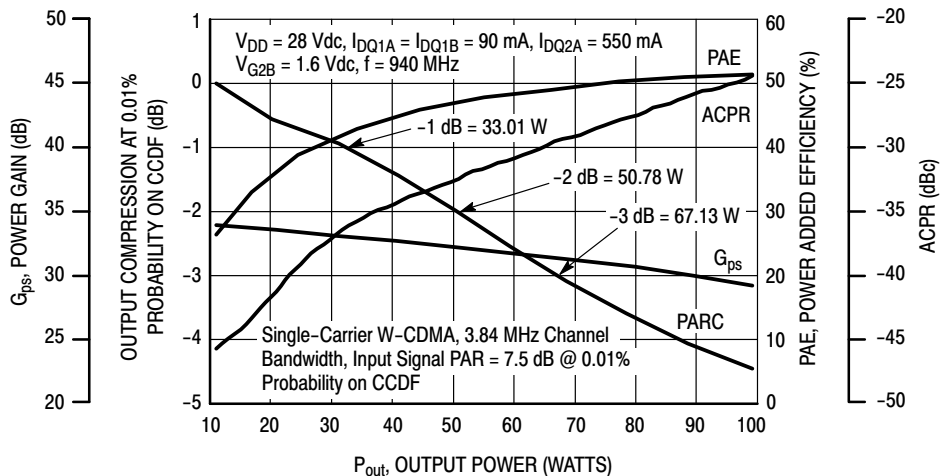


Figure 7. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

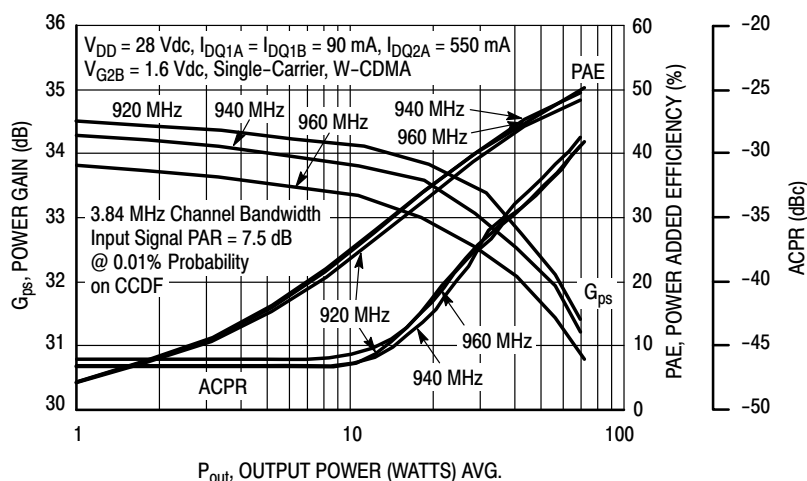


Figure 8. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

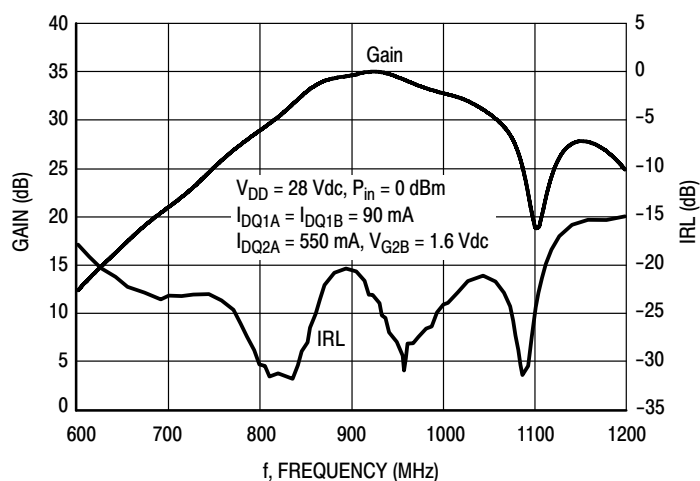


Figure 9. Broadband Frequency Response

W-CDMA TEST SIGNAL

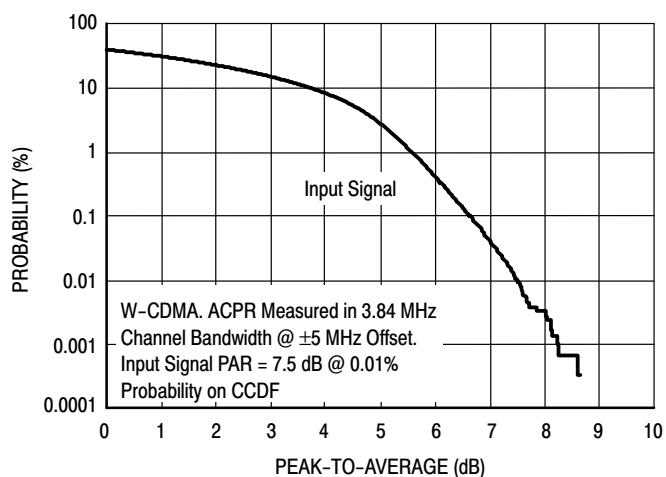


Figure 10. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

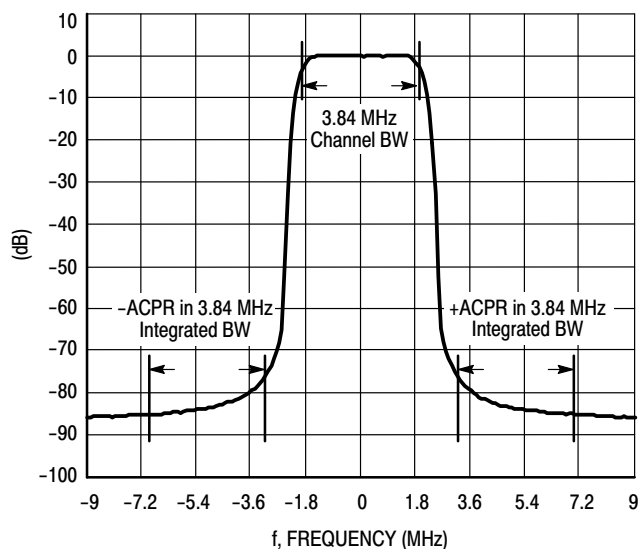


Figure 11. Single-Carrier W-CDMA Spectrum

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ1A} = I_{DQB} = 90 \text{ mA}$, $I_{DQ2A} = 550 \text{ mA}$, $V_{G2B} = 1.6 \text{ Vdc}$, $P_{out} = 25 \text{ W Avg.}$

f MHz	Z_{in} Ω	Z_{load} Ω
820	56.02 - j0.10	3.61 + j1.78
840	57.03 - j2.95	3.11 + j1.50
860	57.27 - j6.01	2.65 + j1.56
880	57.45 - j8.80	2.28 + j1.81
900	57.56 - j12.21	2.07 + j2.11
920	56.66 - j15.98	1.87 + j2.40
940	55.81 - j19.90	1.77 + j2.64
960	53.45 - j23.91	1.75 + j2.89
980	51.34 - j27.40	1.58 + j3.12

Note: Measured with Peaking side open.

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

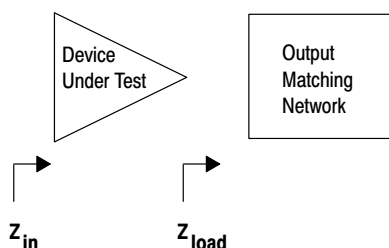


Figure 12. Series Equivalent Input and Load Impedance — Carrier Side

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ1A} = I_{DQB} = 90 \text{ mA}$, $I_{DQ2A} = 550 \text{ mA}$, $V_{G2B} = 1.6 \text{ Vdc}$, $P_{out} = 25 \text{ W Avg.}$

f MHz	Z_{in} Ω	Z_{load} Ω
820	56.02 - j0.10	2.56 - j3.47
840	57.03 - j2.95	2.36 - j2.95
860	57.27 - j6.01	2.15 - j2.39
880	57.45 - j8.80	2.02 - j1.85
900	57.56 - j12.21	1.90 - j1.32
920	56.66 - j15.98	1.72 - j0.85
940	55.81 - j19.90	1.60 - j0.39
960	53.45 - j23.91	1.47 + j0.12
980	51.34 - j27.40	1.30 + j0.66

Note: Measured with Carrier side open.

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

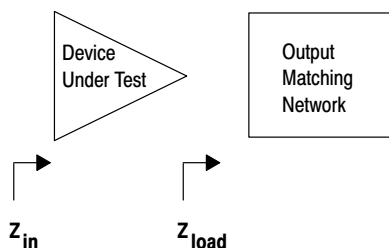
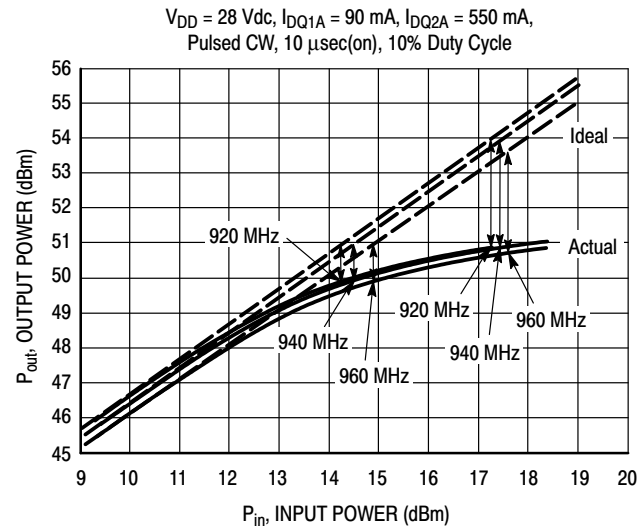


Figure 13. Series Equivalent Input and Load Impedance — Peaking Side

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
920	98.4	49.9	123	50.9
940	98.9	50.0	123	50.9
960	95.5	49.8	118	50.7

Test Impedances per Compression Level

f (MHz)		Z_{source} Ω	Z_{load} Ω
920	P1dB	49.53 - j0.96	1.59 - j0.84
940	P1dB	48.85 - j0.63	1.75 - j0.53
960	P1dB	51.26 - j0.82	1.72 - j0.33

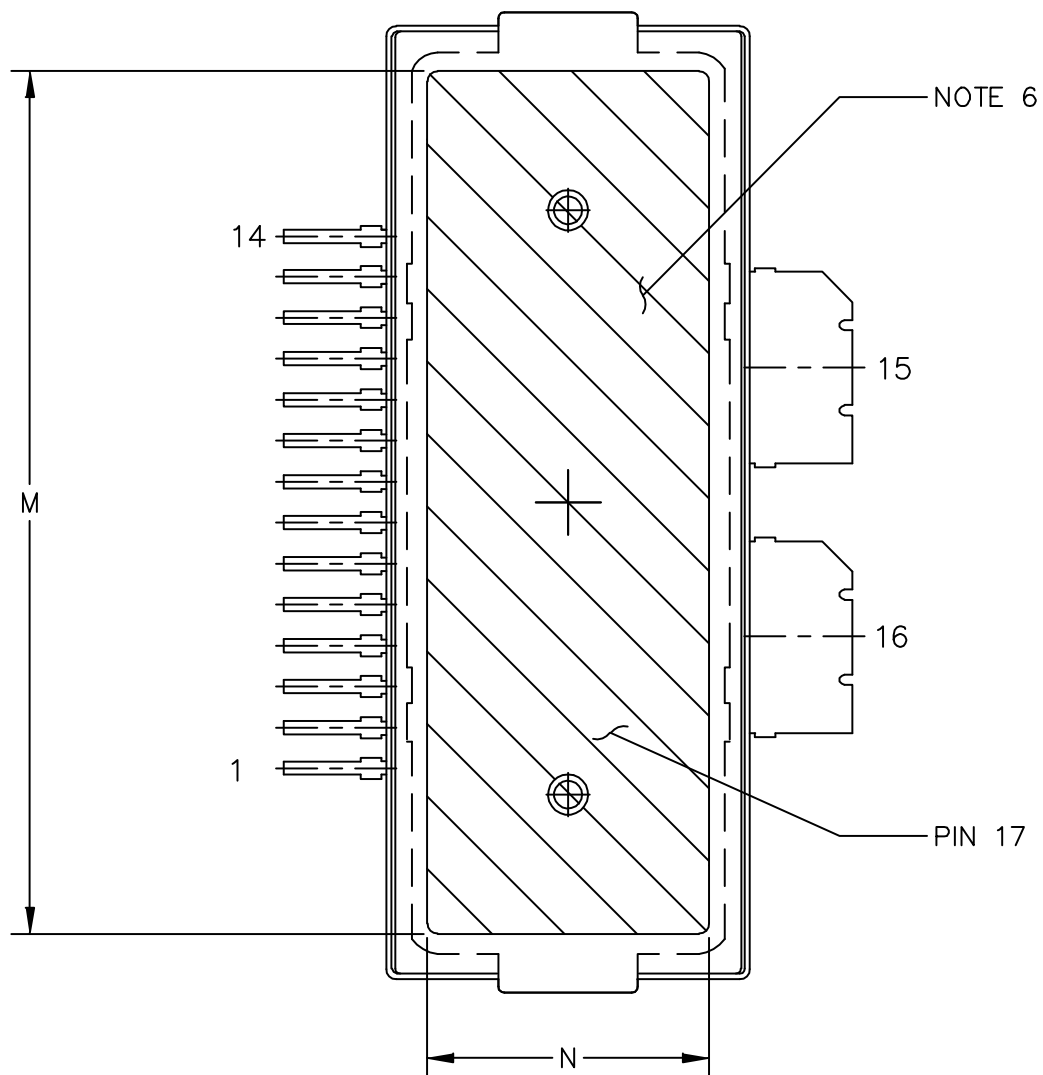
Figure 14. Pulsed CW Output Power
versus Input Power @ 28 V

NOTE: Measurement made on the Class AB, carrier side of the device.

The drawing illustrates a 14-pin connector with the following features and dimensions:

- Top View:**
 - Dimensions:** Overall width E , overall height $D1$, pin pitch $E1$, and pin width $E3$.
 - Pin Array:** 14 pins arranged in a single row. Pin 1 is at the top left. Pin 14 is at the bottom left.
 - Pin Dimensions:** Pin height $13X$ (e1), pin width $14X$ (b1), and pin spacing $2X$ (e3).
 - Feature Callouts:**
 - PIN ONE INDEX:** A circle with a crosshair indicating the location of pin 1.
 - Feature 16:** A rectangular feature on the right side.
 - Feature 15:** A rectangular feature on the right side.
 - Feature 14:** A rectangular feature on the right side.
 - Feature 13:** A rectangular feature on the right side.
 - Feature 12:** A rectangular feature on the right side.
 - Feature 11:** A rectangular feature on the right side.
 - Feature 10:** A rectangular feature on the right side.
 - Feature 9:** A rectangular feature on the right side.
 - Feature 8:** A rectangular feature on the right side.
 - Feature 7:** A rectangular feature on the right side.
 - Feature 6:** A rectangular feature on the right side.
 - Feature 5:** A rectangular feature on the right side.
 - Feature 4:** A rectangular feature on the right side.
 - Feature 3:** A rectangular feature on the right side.
 - Feature 2:** A rectangular feature on the right side.
 - Feature 1:** A rectangular feature on the right side.
- Side View:**
 - Dimensions:** Overall height A , pin height $A1$, and pin width $A2$.
 - Feature Callouts:**
 - DATUM PLANE:** A horizontal line indicating the datum plane.
 - SEATING PLANE:** A horizontal line indicating the seating plane.
 - Feature H:** A rectangular feature on the top surface.
 - Feature C:** A rectangular feature on the bottom surface.
 - Feature Y:** A rectangular feature on the bottom surface.
 - Feature F:** A rectangular feature on the bottom surface.
 - Feature ZONE "J":** A rectangular feature on the bottom surface.
 - Feature 7:** A rectangular feature on the bottom surface.

MDE6IC9120NR1 MDE6IC9120GNR1



VIEW Y-Y

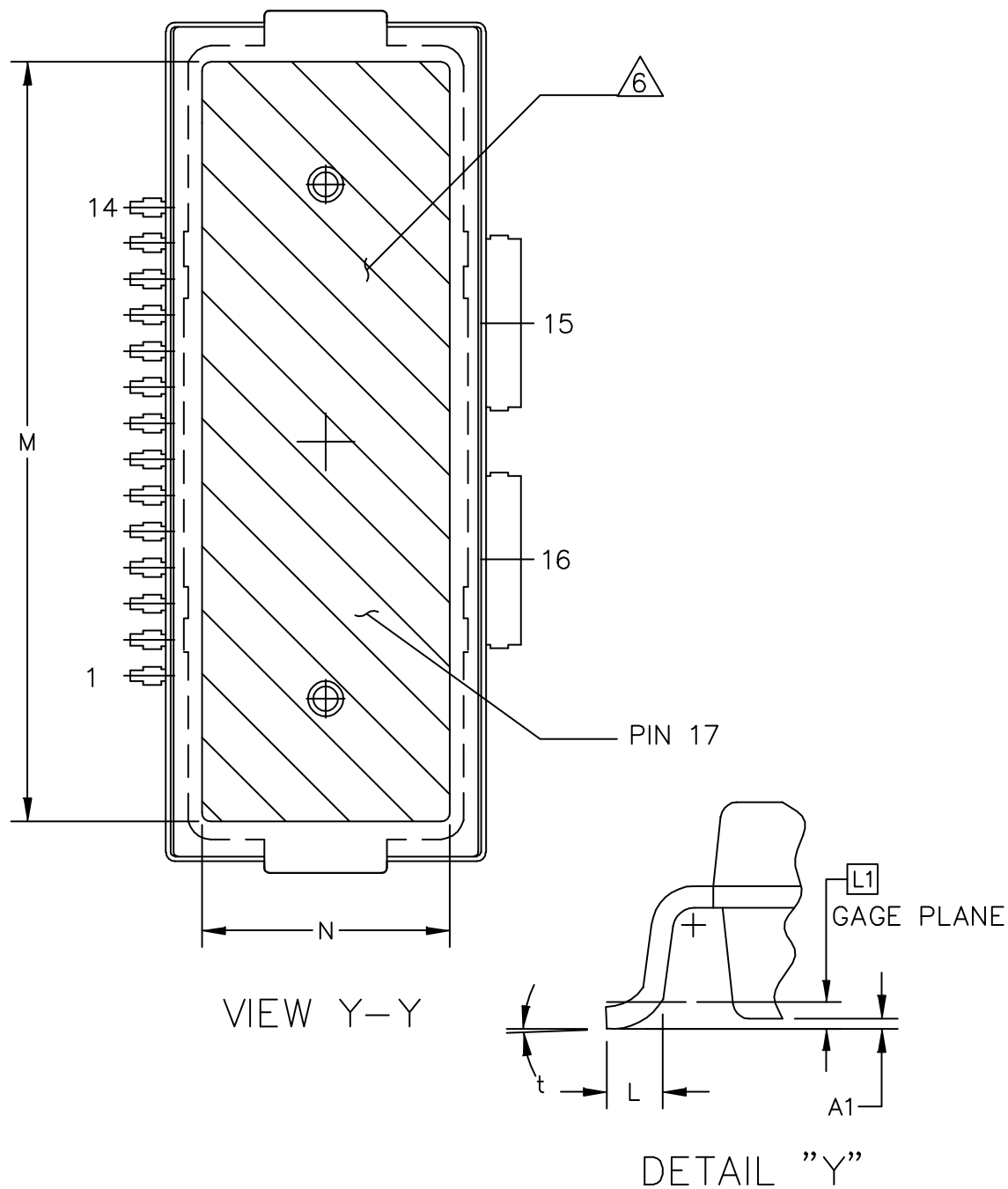
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 WIDE BODY LONG, 16 LEAD, PLASTIC		DOCUMENT NO: 98ASA10739D	REV: A
		CASE NUMBER: 1866-02	02 AUG 2007
		STANDARD: NON-JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

INCH			MILLIMETER		DIM	INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.122	.128	3.10	3.25	M	.800	----	20.32	----
A1	.039	.043	0.96	1.12	N	.270	----	6.86	----
A2	.040	.042	1.02	1.07	b	.184	.190	4.67	4.83
D	.928	.932	23.57	23.67	b1	.010	.016	0.25	0.41
D1	.954	.958	24.23	24.33	c1	.007	.011	0.18	0.28
E	.551	.559	14.00	14.20	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e3	.131 BSC		3.33 BSC	
E3	.132	.140	3.35	3.56					
F	.025 BSC		0.64 BSC		aaa	.004		0.10	

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE		
TITLE: TO-270 WIDE BODY LONG, 16 LEAD, PLASTIC				DOCUMENT NO: 98ASA10739D		REV: A
				CASE NUMBER: 1866-02		02 AUG 2007
				STANDARD: NON-JEDEC		



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: TO-270 WIDE BODY LONG, 16 LEAD, GULL WING PLASTIC		DOCUMENT NO: 98ASA10740D		REV: A	
		CASE NUMBER: 1867-02		02 AUG 2007	
		STANDARD: NON-JEDEC			

MDE6IC9120NR1 MDE6IC9120GNR1

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

INCH		MILLIMETER		INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX
A	.122	.128	3.10	3.25	b	.184	.190
A1	.001	.004	0.02	0.10	b1	.010	.016
A2	.125	.131	3.18	3.33	c1	.007	.011
D	.928	.932	23.57	23.67	e	.020 BSC	0.51 BSC
D1	.954	.958	24.23	24.33	e1	.040 BSC	1.02 BSC
E	.429	.437	10.9	11.1	e2	.131 BSC	3.33 BSC
E1	.353	.357	8.97	9.07	t	2°	8°
E2	.346	.350	8.79	8.89	aaa	.004	0.10
E3	.132	.140	3.35	3.56			
L	.018	.024	0.46	0.61			
L1	.01 BSC		0.25 BSC				
M	.800	----	20.32	----			
N	.270	----	6.86	----			
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE	
TITLE: TO-270 WIDE BODY LONG, 16 LEAD, GULL WING PLASTIC					DOCUMENT NO: 98ASA10740D		REV: A
					CASE NUMBER: 1867-02		02 AUG 2007
					STANDARD: NON-JEDEC		

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Nov. 2009	• Initial Release of Data Sheet

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2009. All rights reserved.

