

Description

The ACS8515 is a highly integrated, single-chip solution for 'hit-less' protection switching of SEC clocks from Master and Slave SETS clockcards in a SONET or SDH Network Element. The ACS8515 has fast activity monitors on the inputs and will implement automatic system protection switching against master clock failure.

A further input is provided for an optional standby SEC clock. The ACS8515 is fully compliant with the required specifications and standards.

The ACS8515 can perform frequency translation from a SEC input clock distributed along a back plane to a different local line card clock, e.g. 8 kHz distributed on the back plane and 19.44 MHz generated on the line cards.

An SPI⁽¹⁾ compatible serial port is incorporated, providing access to the configuration and status registers for device setup.

The ACS8515 can utilise either a low cost XO oscillator module, or a TCXO with full temperature calibration - as required by the application.

Rev2.1 adds choice of edge alignment for 8kHz input, as well as a low jitter n x E1/DS1 output mode. Other minor changes are made, with all described in Appendix A.

Features

- Suitable for Stratum 3, 4E and 4 SONET or SDH Equipment Clock (SEC) applications
- Meets AT&T, ITU-T, ETSI and Telcordia specifications
- Three SEC input clocks, from 2 kHz to 155.52 MHz
- Generates two SEC output clocks, up to 311.04 MHz
- Frequency translation of SEC input clock to a different local line card clock
- Robust input clock source frequency and activity monitoring on all inputs
- Supports Free-run, Locked and Holdover modes of operation
- Automatic 'hit-less' source switchover on loss of input
- External force fast switch between SEC inputs
- Phase build out for output clock phase continuity during input switchover
- SPI⁽¹⁾ compatible serial microprocessor interface
- Programmable wander and jitter tracking attenuation 0.1 Hz to 20 Hz
- Single +3.3 V operation. +5 V I/O compatible
- Operating temperature (ambient) -40°C to +85°C
- Available in 64 pin LQFP package
- Lead (pb)-free version available (ACS8515 Rev2.1T) RoHS and WEEE compliant.

(1) SPI is a trademark of Motorola Corporation

Block Diagram

Figure 1. Simple Block Diagram

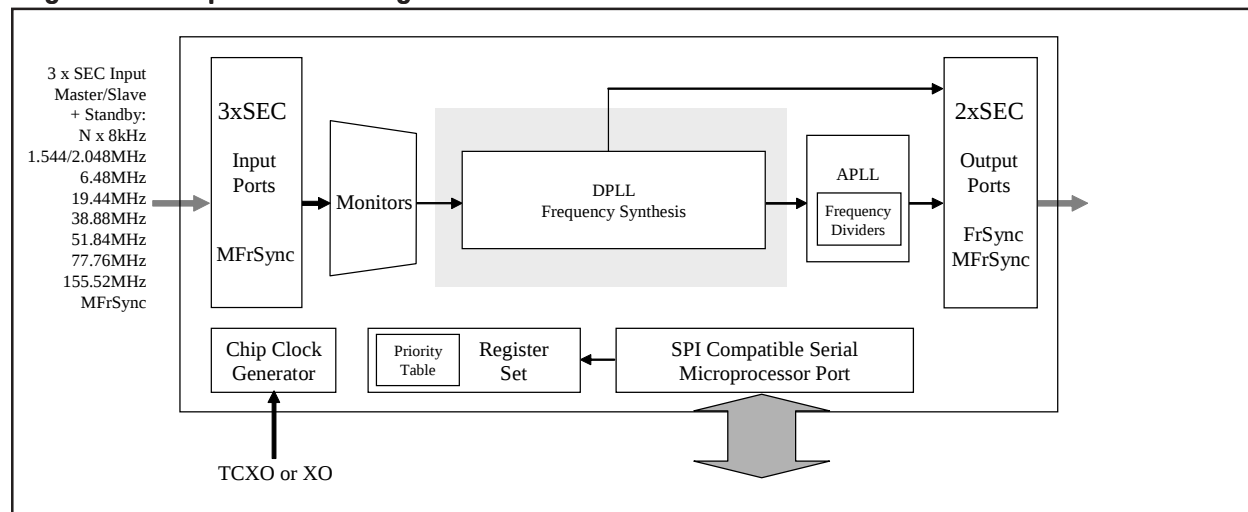


Table of Contents**List of Sections**

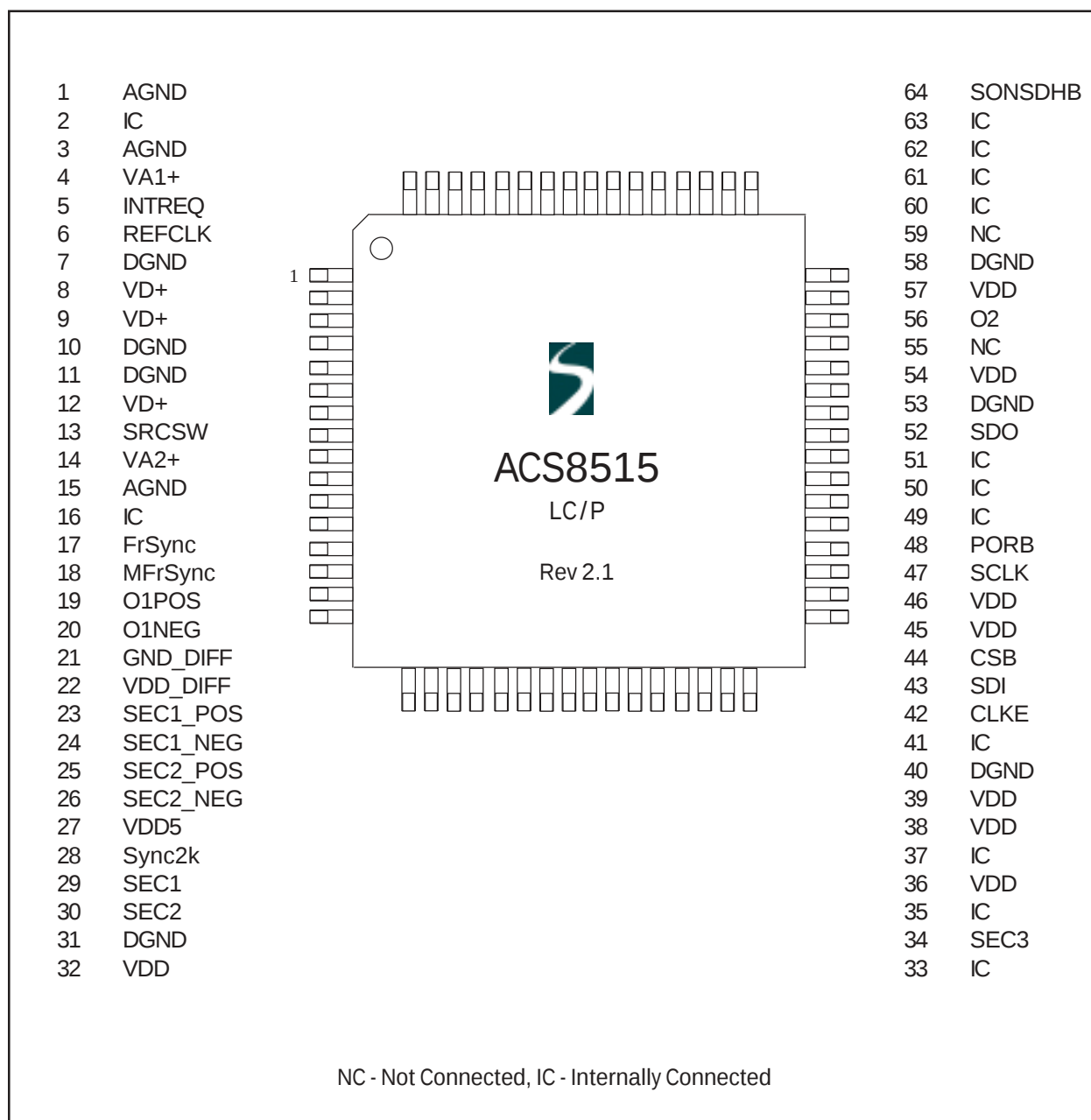
Description	1
Block Diagram	1
Features	1
Table of Contents	2
Pin Diagram	4
Pin Descriptions	5
Functional Description	7
Local Oscillator Clock	7
Crystal Frequency Calibration	7
Input Reference Clock Ports	8
Input Wander and Jitter Tolerance	10
Output Clock Ports	11
Low Speed Output Clock	11
High Speed Output Clock	12
Frame Sync and Multi-Frame Sync Clocks	12
Low Jitter Multiple E1/DS1 Outputs	12
Output Wander and Jitter	13
Phase Variation	14
Phase Build Out	16
Microprocessor Interface	16
Register Set	16
Configuration Registers	16
Status Registers	16
Register Access	17
Interrupt Enable and Clear	17
Register Map	18
Register Map Description	21
Selection of Input Reference Clock Source	29
Automatic Control Selection	29
Ultra Fast Switching	30
External Protection Switching	30
Activity Monitoring	30
Modes of Operation	32
Free-run Mode	32
Pre-Locked Mode	32
Locked Mode	32
Lost-Phase Mode	33
Holdover Mode	33
Pre-Locked(2) Mode	33
Power On Reset - PORB	33
Electrical Specification	35
Serial Microprocessor Interface Timing	44
Package Information	46
Thermal Conditions	47
Application Information	48
Appendix A Rev2.1 Changes Described	49
Revision History	49
Ordering Information	50
Disclaimers	50

List of Figures

Figure 1. Simple Block Diagram	1
Figure 2. ACS8515 Pin Diagram	4
Figure 3. Minimum Input Jitter Tolerance (OC-3/STM-1)	11
Figure 4. Minimum Input Jitter Tolerance (DS1/E1)	12
Figure 5. Wander and Jitter Transfer Measured Characteristics	14
Figure 6. Maximum Time Interval Error of TOUT0 Output Port	15
Figure 7. Time Deviation of TOUT0 Output Port	15
Figure 8. Phase Error Accumulation of TOUT0 Output Port in Holdover Mode	15
Figure 9. Inactivity and Irregularity Monitoring	30
Figure 10. Automatic Mode Control State Diagram	34
Figure 11. Recommended Line Termination for PECL Input/Output Ports	38
Figure 12. Recommended Line Termination for LVDS Input/Output Ports	39
Figure 13. Input/Output Timing	43
Figure 14. Serial Interface Read Access Timing	44
Figure 15. Serial Interface Write Access Timing	45
Figure 16. LQFP Package	46
Figure 17. Typical 64 Pin LQFP Footprint	47
Figure 18. Simplified Application Schematic	48

List of Tables

Table 1. Power Pins	5
Table 2. No Connections	5
Table 3. Other Pins	6
Table 4. Input Reference Source Selection and Group Allocation	9
Table 5. Input Reference Source Jitter Tolerance	10
Table 6. Amplitude and Frequency values for Jitter Tolerance	11
Table 7. Amplitude and Frequency values for Jitter Tolerance	12
Table 8. Output Reference Source Selection Table	13
Table 9. Multiple E1/DS1 Output in Relation to Normal Outputs	13
Table 10. Register Map	18
Table 11. Register Map Description	21
Table 12. Absolute Maximum Ratings	35
Table 13. Operating Conditions	35
Table 14. DC Characteristics: TTL Input Pad	35
Table 15. DC Characteristics: TTL Input Pad with Internal Pull-up	36
Table 16. DC Characteristics: TTL Input Pad with Internal Pull-down	36
Table 17. DC Characteristics: TTL Output Pad	36
Table 18. DC Characteristics: PECL Input/Output Pad	37
Table 19. DC Characteristics: LVDS Input/Output Pad	38
Table 20. DC Characteristics: Output Jitter Generation (Test definition G.813)	39
Table 21. DC Characteristics: Output Jitter Generation (Test definition G.812)	40
Table 22. DC Characteristics: Output Jitter Generation (Test definition ETS-300-462-3)	40
Table 23. DC Characteristics: Output Jitter Generation (Test definition GR-253-CORE)	41
Table 24. DC Characteristics: Output Jitter Generation (Test definition AT&T 62411)	41
Table 25. DC Characteristics: Output Jitter Generation (Test definition G.742)	42
Table 26. DC Characteristics: Output Jitter Generation (Test definition TR-NWT-000499)	42
Table 27. DC Characteristics: Output Jitter Generation (Test definition GR-1244-CORE)	42
Table 28. Serial Interface Read Access Timing	45
Table 29. Serial Interface Write Access Timing	45
Table 30. 64 Pin LQFP Package Dimension Data (for use with Figure 16)	47
Table 31. Revision History	49

Pin Diagram
Figure 2. ACS8515 Pin Diagram


Pin Descriptions
Table 1. Power Pins

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
8, 9, 12	VD+	P	-	Supply voltage: Digital supply to gates in analog section, +3.3 Volts. +/- 10%
22	VDD_DIFF	P	-	Supply voltage: Digital supply for differential output pins 19 & 20, +3.3 Volts. +/- 10%
27	VDD5	P	-	VDD5: Digital supply for +5 Volts tolerance to input pins. Connect to +5 volts (+/- 10%) for clamping to +5 v. Connect to VDD for clamping to +3.3 v. Leave floating for no clamping, input pins tolerant up to +5.5 v.
32, 36, 38, 39, 45, 46, 54, 57	VDD	P	-	Supply voltage: Digital supply to logic, +3.3 Volts. +/- 10%
4	VA1+	P	-	Supply voltage: Analog supply to clock multiplying APLL, +3.3 Volts. +/- 10%
14	VA2+	P	-	Supply voltage: Analog supply to output APLL, +3.3 Volts. +/- 10%
7, 10, 11, 31, 40, 53, 58	DGND	P	-	Supply Ground: Digital ground for logic
21	GND_DIFF	P	-	Supply Ground: Digital ground for differential output pins 19 & 20
1, 3, 15	AGND	P	-	Supply Ground: Analog ground

Table 2. No Connections

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
55, 59	NC	-	-	Not Connected: Leave to Float
2, 16, 33, 35, 60, 61, 62, 63	IC	-	-	Internally Connected: Leave to Float
37	IC	-	-	Internally connected: Leave to Float. Reserved for JTAG control reset input on next revision
41	IC	-	-	Internally connected: Leave to Float. Reserved for JTAG test mode select input on next revision
49	IC	-	-	Internally connected: Leave to Float. Reserved for JTAG boundary scan clock input on next revision
50	IC	-	-	Internally connected: Leave to Float. Reserved for JTAG serial test data output on next revision
51	IC	-	-	Internally connected: Leave to Float. Reserved for JTAG serial test data input on next revision

Table 3. Other Pins

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
5	INTREQ	O	-	Interrupt request: Software Interrupt enable
6	REFCLK	I	TTL	Reference clock: 12.8 MHz (refer to section headed Local Oscillator Clock)
13	SRCSW	I	TTL _D	Source switching: Force fast source switching on SEC1 and SEC2
17	FrSync	O	TTL	Output reference: 8 kHz Frame Sync, 50:50 mark/space ratio output
18	MFrSync	O	TTL	Output reference: 2 kHz Multi-Frame Sync, 50:50 mark/space ratio output
19 20	O1POS O1NEG	O	LVDS/ PECL	Output reference: Programmable, default 38.88 MHz LVDS
23 24	SEC1_POS SEC1_NEG	I	LVDS/ PECL	Input reference: Programmable, default 19.44 MHz LVDS
25 26	SEC2_POS SEC2_NEG	I	PECL/ LVDS	Input reference: Programmable, default 19.44 MHz PECL
28	Sync2k	I	TTL _D	Multi-Frame Sync 2 kHz: Multi-Frame Sync input
29	SEC1	I	TTL _D	Input reference: Programmable, default 8 kHz
30	SEC2	I	TTL _D	Input reference: Programmable, default 8 kHz
34	SEC3	I	TTL _D	Input reference: External standby reference clock source, programmable, default 19.44 MHz
42	CLKE	I	TTL _D	SCLK edge select: SCLK active edge select, CLKE=1 selects falling edge of SCLK to be active, CLKE = 0 for rising edge
43	SDI	I	TTL _D	Microprocessor interface address: Serial data input
44	CSB	I	TTL ^U	Chip select (active low): This pin is asserted Low by the microprocessor to enable the microprocessor interface
47	SCLK	I	TTL _D	Address Latch Enable: default Serial data clock. When this pin transitions from low to high, the address bus inputs are latched into the internal registers
48	PORB	I	TTL ^U	Power on reset: Master reset. If PORB is forced Low, all internal states are reset back to default values

Note: I = input, O = output, P = power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor

Table 3 (continued).

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
52	SDO	O	TTL _D	Microprocessor interface address: Serial data output
56	O2	O	TTL	Output reference: 19.44 MHz fixed
64	SONSDHB	I	TTL _D	SONETSDHB: SONET or SDH frequency select: sets the initial power-up state (or state after a PORB) of the SONET/SDH frequency selection registers, addr 34h, bit 2 and addr 38, bits 5 and 6. When low SDH rates are selected (2.048 MHz etc) and when set high SONET rates are selected (1.544 MHz etc). The register states can be changed after power up by software.

Functional Description

The ACS8515 is a highly integrated, single-chip solution for 'hit-less' protection switching of SEC clocks from Master and Slave SETS clock cards in a SONET or SDH Network Element. The ACS8515 has fast activity monitors on the inputs and will implement automatic system protection switching for Master/Slave SEC clock failure. The standby SEC clock will be selected if both the Master and Slave input clocks fail. The selection of the Master/Slave input can also be forced by a Force Fast Switch pin.

The ACS8515 can perform frequency translation from a SEC input clock distributed along a back plane to a different local line card - e.g. 8 kHz distributed on the back plane and 19.44 MHz generated on the line cards.

The ACS8515 has three SEC clock inputs (Master, Slave and Standby) and a single Multi-Frame Sync input, for synchronising the frame and multi-frame sync outputs.

The ACS8515 generates two SEC clock outputs via PECL/LVDS and TTL ports, with spot frequencies from 1.544/2.048 MHz up to 311.04 MHz. The ACS8515 also provides an 8 kHz Frame Sync and 2 kHz Multi-Frame Sync output clock.

The ACS8515 has a high tolerance to input jitter and wander. The jitter/wander transfer is programmable (0.1 Hz up to 20 Hz cut-off points).

The ACS8515 includes an SPI compatible serial microprocessor port, providing access to the configuration and status registers for device setup.

Local Oscillator Clock

The Master system clock on the ACS8515 requires an external clock oscillator of frequency 12.80 MHz. The exact clock specification is dependent on the quality of Holdover performance required in the application.

In most Line Card protection switching applications where there is a high chance that at least one SEC reference input will be available, the long term stability requirement for Holdover is not appropriate and an inexpensive crystal local oscillator can be used. In other applications where there may be a requirement for longer term Holdover stability to meet the ITU standards for Stratum 3, a higher quality oscillator can be used.

Please contact Semtech for information on crystal oscillator suppliers.

Crystal Frequency Calibration

The absolute crystal frequency accuracy is less important than the stability since any frequency offset can be compensated by adjustment of register values in the IC. This allows for calibration and compensation of any crystal frequency variation away from its nominal value.

+/- 50 ppm adjustment would be sufficient to cope with most crystals, in fact the range is an order of magnitude larger due to the use of two 8 bit register locations. The setting of the *conf_nominal_frequency* register allows for this adjustment. An increase in the register value increases the output frequencies by 0.02 ppm for each LSB step. The default value (in decimal) is 39321. The minimum being 0 and the maximum 65535, giving a -700 ppm to +500 ppm adjustment range of the output frequencies.

For example, if the crystal was oscillating at 12.8 MHz + 5 ppm, then the calibration value in the register to give a - 5 ppm adjustment in output frequencies to compensate for the crystal inaccuracy, would be :

$$39321 - (5 / 0.02) = 39071 \text{ (decimal)}$$

The ACS8515 supports up to three individual input reference clock sources via TTL/CMOS and PECL/LVDS technologies. These interface technologies support +3.3 V and +5 V operation.

Input Reference Clock Ports

The input reference clock ports are arranged in groups. Group one comprises a TTL port (SEC1) and a PECL/LVDS port (SEC1POS and SEC1NEG). Group two comprises a TTL port (SEC2) and a PECL/LVDS port (SEC2POS and SEC2NEG). Group three comprises a TTL port (SEC3). For group one and group two, only one of the two input ports types must be active at any time, the other must not be driven by a reference input. Unused PECL/LVDS differential inputs should be fixed with one input high (VDD) and the other low (GND), or set in LVDS mode and left floating (in which case one input is internally pulled high and the other low).

SDH and SONET networks use different default frequencies; the network type is selectable using the *config_mode* register 34 Hex, bit 2. For SONET, *config_mode* register 34 Hex, bit 2 = 1, for SDH *config_mode* register 34 Hex, bit

2 = 0. On power-up or by reset, the default will be set by the state of the SONSDHB pin (pin 64). Specific frequencies and priorities are set by configuration.

The TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. Clock speeds above 100 MHz should not be applied to the TTL ports. The PECL/LVDS ports support the full range of clock speeds, up to 155.52 MHz.

The actual spot frequencies supported are:

- 2 kHz
- 4 kHz
- 8 kHz (and N x 8 kHz),
- 1.544 MHz (SONET)/2.048 MHz (SDH),
- 6.48 MHz,
- 19.44 MHz,
- 25.92 MHz,
- 38.88 MHz,
- 51.84 MHz,
- 77.76 MHz,
- 155.52 MHz.

The frequency selection is programmed via the *cnfg_ref_source_frequency* register. The internal DPLL will normally lock to the selected input at the frequency of the input, eg. 19.44 MHz will lock the DPLL phase comparisons at 19.44 MHz. It is, however, possible to utilise an internal pre-divider to the DPLL to divide the input frequency before it is used for phase comparisons in the DPLL. This pre-divider can be used in one of 2 ways;

1. Any of the supported spot frequencies can be divided to 8 kHz by setting the 'lock8K' bit (bit 6) in the appropriate *cnfg_ref_source_frequency* register location. For good jitter tolerance for all frequencies and for operation at 19.44 MHz and above, use lock8K. It is possible to choose which edge of the 8kHz input to lock to, by setting the appropriate bit of the *cnfg_control1* register.

Table 4. Input Reference Source Selection and Group Allocation

Port Name	Input Port Technology	Frequencies Supported	SEC Source Group	Default Priority (Note 3)
SEC1	TTL/CMOS	Up to 100MHz (Note 1) Default (SONET/SDH): 8kHz	1	1 (4)
SEC2	TTL/CMOS	Up to 100MHz (Note 1) Default (SONET/SDH): 8kHz	2	3 (5)
SEC1	LVDS/PECL LVDS default	Up to 155.52MHz (Note 2) Default (SONET/SDH): 19.44MHz	1	2 (6)
SEC2	PECL/LVDS PECL default	Up to 155.52MHz (Note 2) Default (SONET/SDH): 19.44MHz	2	4 (7)
SEC3	TTL/CMOS	Up to 100MHz (Note 1) Default (SONET/SDH): 19.44MHz	3	5 (10)
SYNC1	TTL/CMOS	2kHz Multi Frame Sync	-	-

Notes for Table 4.

Note 1. TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies are 2 kHz, 4 kHz, 8 kHz, N x 8 kHz, 1.544/2.048 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz and 77.76 MHz.

Note 2. PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz. There are different output clock frequencies available for SONET and SDH applications.

Note 3. The default priority values in brackets are the default numbers reported in the register map, which match up with the ACS8510.

On power up, or by reset, the default will be set by the SONSDHB pin. Specific frequencies and priorities are set by configuration. For SONET, *config_mode* register 34 Hex, bit 2 = 1. For SDH *config_mode* register 34 Hex, bit 2 = 0.

2. Any multiple of any supported frequency can be supported by using the "DivN" feature (bit 7 of the *cnfg_ref_source_frequency* register). Any reference input can be set to lock at 8 kHz independently of the frequencies and configurations of the other inputs.

Any reference input with the 'DivN' bit set in the *cnfg_ref_source_frequency* register will employ the internal pre-divider prior to the DPLL locking. The *cnfg_freq_divn* register contains the divider ratio N where the reference input will get divided by (N+1) where $0 < N < 2^{14} - 1$. The *cnfg_ref_source_frequency* register must be set to the closest supported spot frequency to the input frequency, but must be lower than the

input frequency. When using the 'DivN' feature the post-divider frequency must be 8 kHz, which is indicated by setting the 'lock8k' bit high (bit 6 in *cnfg_ref_source_frequency* register). Any input set to DivN must have the frequency monitors disabled (if the frequency monitors are disabled, they are disabled for all inputs regardless of the input configurations, in this case only activity monitoring will take place). Whilst any number of inputs can be set to use the 'DivN' feature, only one N can be programmed, hence all inputs using the 'DivN' feature must require the same division to get to 8 kHz.

PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz. The choice of PECL or LVDS compatibility is programmed via the *cnfg_differential_inputs* register.

Unused PECL/LVDS differential inputs should be fixed with one input high (VDD) and the other input low (GND), or set in LVDS mode and left floating, in which case one input is internally pulled high and the other low.

Input Wander and Jitter Tolerance

The ACS8515 is compliant to the requirements of all relevant standards, principally ITU Recommendation G.825, ANSI DS1.101-1994 and ETS 300 462-5 (1997).

All reference clock inputs have a tight frequency tolerance but a generous jitter tolerance. Pull-in, hold-in and pull-out ranges are specified for each input port in Table 5. Minimum jitter tolerance masks are specified in Figures 3 and 4, and Tables 6 and 7, respectively. The ACS8515 will tolerate wander and jitter components greater than those shown in Figure

3 and Figure 4, up to a limit determined by a combination of the apparent long-term frequency offset caused by wander and the eye-closure caused by jitter (the input source will be rejected if the offset pushes the frequency outside the hold-in range for long enough to be detected, whilst the signal will also be rejected if the eye closes sufficiently to affect the signal purity). The '8klocking' mode should be engaged for high jitter tolerance according to these masks.

All reference clock ports are monitored for quality, including frequency offset and general activity. Single short-term interruptions in selected reference clocks may not cause rearrangements, whilst longer interruptions, or multiple, short-term interruptions, will cause rearrangements, as will frequency offsets which are sufficiently large or sufficiently long to cause loss-of-lock in the phase-locked loop. The failed reference source will be removed from the priority table and declared as unserviceable, until its perceived quality has been restored to an acceptable level.

Table 5. Input Reference Source Jitter Tolerance

Jitter Tolerance	Frequency Monitor Acceptance Range	Frequency Acceptance Range (Pull-in)	Frequency Acceptance Range (Hold-in)	Frequency Acceptance Range (Pull-out)
G.703	+/- 16.6 ppm	+/- 4.6 ppm (see Note 1)	+/- 4.6 ppm (see Note 1)	+/- 4.6 ppm (see Note 1)
G.783				
G.823		+/- 9.2 ppm (see Note 2)	+/- 9.2 ppm (see Note 2)	+/- 9.2 ppm (see Note 2)
GR-1244-CORE				

Notes for Table 5.

Note 1. The frequency acceptance and generation range will be +/-4.6 ppm around the required frequency when the external crystal frequency accuracy is within a tolerance of +/- 4.6 ppm.

Note 2. The default acceptance range and generation range is +/- 9.2 ppm with an exact external crystal frequency of 12.8 MHz. This range is also programmable from 0 to 80 ppm in 0.08 ppm steps.

The registers *sts_curr_inc_offset* (address 0C, 0D, 07) report the frequency of the DPLL with respect to the external TCXO frequency. This is a 19 bit signed number with one LSB representing 0.0003 ppm (range of +/- 80 ppm). Reading this regularly can show how the currently locked source is varying in value e.g. due to wander on its input.

The ACS8515 performs automatic frequency monitoring with an acceptable input frequency offset range of +/- 16.6 ppm. The ACS8515 DPLL has a programmable frequency limit of +/- 80 ppm. If the range is programmed to be > 16.6 ppm, the frequency monitors should be disabled so the input reference source is not automatically rejected as out of frequency range.

Output Clock Ports

The ACS8515 supports two SEC output clocks, on TTL and PECL/LVDS ports, and a pair of secondary output clocks, 'Frame-Sync' and 'Multi-Frame-Sync'. The two output clocks are individually controllable. The 'Frame-Sync' and 'Multi-Frame-Sync' are derived from the main SEC clock. The frequencies of the output clock are selectable from a range of pre-defined spot frequencies, with a variety of output technologies supported, as defined in Table 8.

Low Speed Output Clock

The O2 SEC clock is supplied on a TTL port with a fixed frequency of 19.44 MHz.

Figure 3. Minimum Input Jitter Tolerance (OC-3/STM-1)

(for inputs supporting G.783 compliant sources)

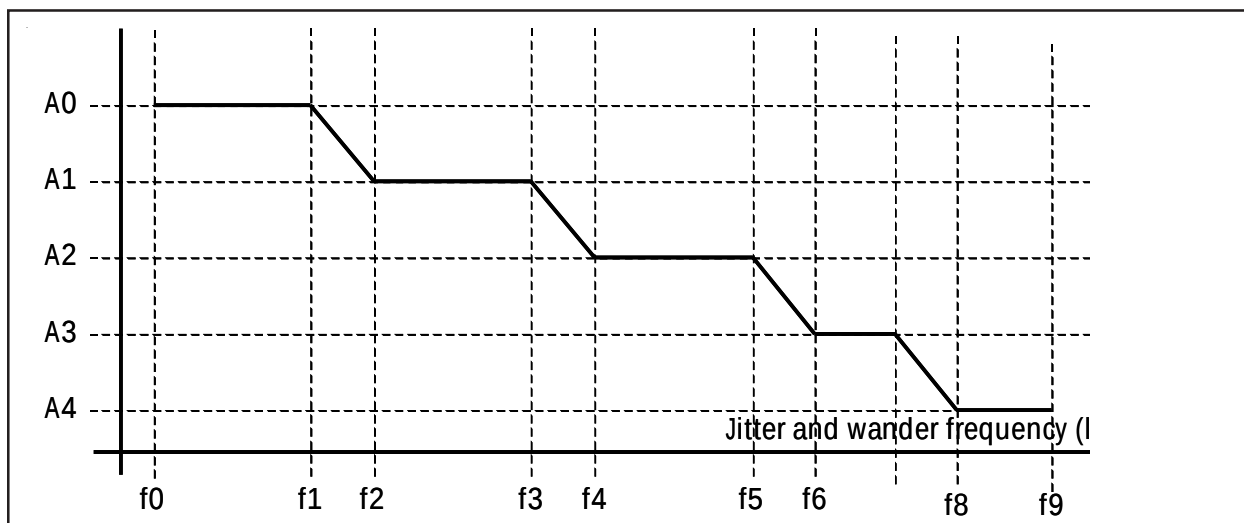


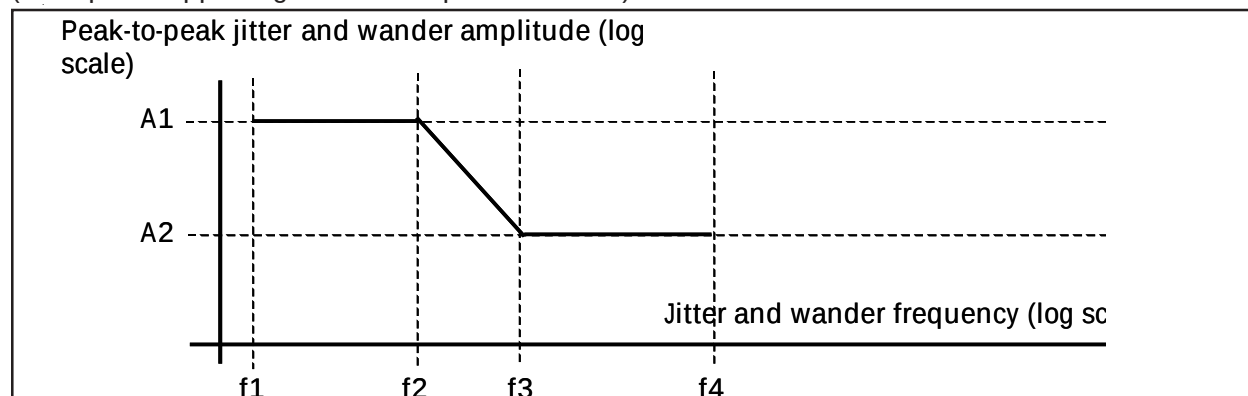
Table 6. Amplitude and Frequency values for Jitter Tolerance

(for inputs supporting G.783 compliant sources)

STM level	Peak to peak amplitude (unit Interval)					Frequency (Hz)									
	A0	A1	A2	A3	A4	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9
STM-1	2800	311	39	1.5	0.15	12u	178u	1.6m	15.6m	0.125	19.3	500	6.5k	65k	1.3m

Figure 4. Minimum Input Jitter Tolerance (DS1/E1)

(for inputs supporting G.783 compliant sources)


Table 7. Amplitude and Frequency values for Jitter Tolerance

(for inputs supporting G.783 compliant sources)

Type	Spec.	Amplitude (UI pk-pk)		Frequency (Hz)			
		A1	A2	F1	F2	F3	F4
DS1	GR-1244-CORE	5	0.1	10	500	8k	40k
E1	ITU G.823	1.5	0.2	20	2.4k	18k	100k

High Speed Output Clock

The O1 SEC clock is supplied on a PECL/LVDS port with spot frequencies of;

- 19.44 MHz,
- 38.88 MHz,
- 155.52 MHz,
- 311.04 MHz,
- Dig 1.

(where Dig 1 is 1.544 MHz (SONET)/2.048 MHz (SDH), and multiples of 2, 4 and 8 depending on SONET/SDH mode setting).

The actual frequency is selectable via the *cnfg_differential_outputs* register. The O1 port can also support 311.04 MHz, which is enabled via the *cnfg_T0_output_enable* register. The O1 port can be made LVDS or PECL compatible via the *cnfg_differential_outputs* register.

Frame Sync and Multi-Frame Sync Clocks

Frame Sync (8 kHz) and Multi-Frame Sync (2 kHz) clocks will be provided on outputs FrSync and MFrSync. The FrSync and MFrSync clocks have a 50:50 mark/space ratio.

Low Jitter Multiple E1/DS1 Outputs

This feature added to Rev2.1 is activated using the *cnfg_control1* register. This sends a frequency of twice the Dig2 rate (see reg addr 39h, bits 7:6) to the APLL instead of the normal 77.76MHz. For this feature to be used, the Dig2 rate must only be set to 12352kHz/16384kHz using the *cnfg_T0_output_frequencies* register. The normal OC3 rate outputs are then replaced with E1/DS1 multiple rates. The E1(SONET)/DS1(SDH) selection is made in the same way as for Dig2 using the *cnfg_T0_output_enable* register. Table 9 shows the relationship between primary output frequencies and the corresponding output in E1/DS1 mode, and which output they are available from.

Output Wander and Jitter

Wander and jitter present on the output clocks are dependent on:

1. The magnitude of wander and jitter on the selected input reference clock (in locked mode);
2. The internal wander and jitter transfer characteristic (in Locked mode);
3. The jitter on the local oscillator clock;
4. The wander on the local oscillator clock (in Holdover mode).

Wander and jitter are treated in different ways to reflect their differing impacts on network design. Jitter is always strongly attenuated, whilst wander attenuation can be varied to suit

the application and operating state. Wander and jitter attenuation is performed by using a digital phase-locked loop (DPLL) with a programmable bandwidth. This gives a transfer characteristic of a low pass filter, with a programmable pole. It is sometimes necessary to change the filter dynamics to suit particular circumstances - one example being when locking to a new source, the filter can be opened up to reduce locking time and can then be gradually tightened again to remove wander. Since wander represents a relatively long-term deviation from the nominal operating frequency, it affects the rate of supply of data to the network element. Strong wander attenuation limits the rate of consumption of data to within a smaller range, so a larger buffer store is required to prevent data loss. But, since

Table 8. Output Reference Source Selection Table

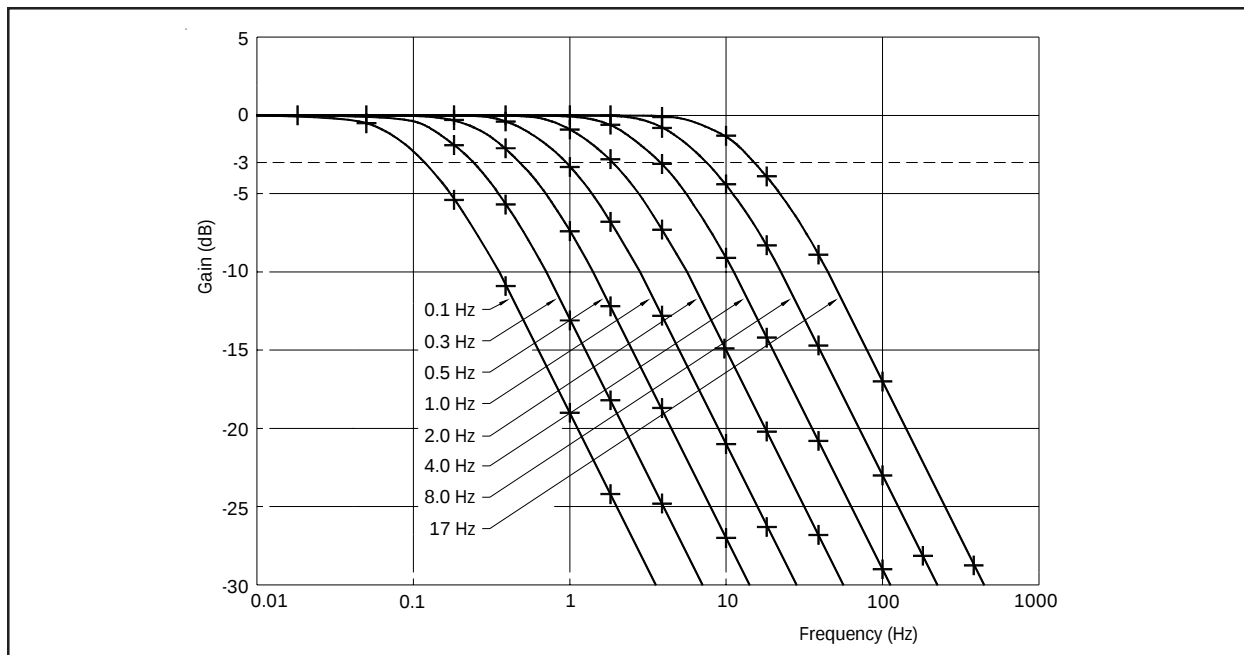
Port Name	Output Port Technology	Frequencies Supported
O1	LVDS/PECL LVDS default	19.44 MHz, 38.88 MHz (default), 155.52 MHz, 311.04 MHz, Dig1 Dig1 is 1.544 MHz/2.048 MHz and multiples of 2, 4 and 8
O2	TTL/CMOS	19.44 MHz fixed
FrSync	TTL/CMOS	FrSync, 8 kHz. 50:50 mark/space ratio
MFrSync	TTL/CMOS	MFrSync, 2 kHz. 50:50 mark/space ratio

Notes for Table 8.

Dig 1 is shown as either 1.544 MHz or 2.048 MHz, where 1.544 MHz is SONET and 2.048 MHz is SDH. Pin SONSDHB controls the default frequency output. When SONSDHB pin is High SONET is default, and when SONSDHB pin is Low SDH is default.

Table 9. Multiple E1/DS1 Outputs in relation to Standard Outputs

Mode	Freq to APLL	APLL Multiplier	APLL Freq	clk_filt	clk_filt/2	clk_filt/4	clk_filt/6	clk_filt/8	clk_filt/12	clk_filt/16	clk_filt/48	DPLL Freq
Default	77.76	4	311.04	311.04	155.52	77.76	51.84	38.88	25.92	19.44	6.48	77.76
n value						16		8		4		
n x E1	32.768	4	131.072	131.072	65.536	32.768	21.84533	16.384	10.92267	8.192	2.730667	77.76
n x T1	24.704	4	98.816	98.816	49.408	24.704	16.46933	12.352	8.234667	6.176	2.058667	77.76
Frequencies Available by Output												
				O1				O1			O1	
											O2	

Figure 5. Wander and Jitter Transfer Measured Characteristics


any buffer store potentially increases latency, wander may often only need to be removed at specific points within a network where buffer stores are acceptable, such as at digital cross connects. Otherwise, wander is sometimes not required to be attenuated and can be passed through transparently. The ACS8515 has programmable wander transfer characteristics in a range from 0.1 Hz to 20 Hz. The wander and jitter transfer characteristic is shown in Figure 5.

Wander on the local oscillator clock will not have significant effect on the output clock whilst in locked mode, so long as the DPLL bandwidth is set high enough so that the DPLL can compensate quickly enough for any frequency changes in the crystal. In Free-run or Holdover mode wander on the crystal is more significant. Variation in crystal temperature or supply voltage both cause drifts in operating frequency, as does ageing. These effects must be limited by careful selection of a suitable component for the local oscillator, as specified in the section 'Local Oscillator Clock'.

Phase Variation

There will be a phase shift across the ACS8515 between the selected input reference source and the output clock. This phase shift may vary over time but will be constrained to lie within specified limits. The phase shift is characterized using two parameters, MTIE (Maximum Time Interval Error), and TDEV (Time Deviation), which, although being specified in all relevant specifications, differ in acceptable limits in each one. Typical measurements for the ACS8515 are shown in Figures 6 and 7, for locked mode operation. Figure 8 shows a typical measurement of Phase Error accumulation in Holdover mode operation.

The required performance for phase variation during Holdover is specified in several ways depending upon the particular circumstances pertaining:

1. ETSI 300 462-5, Section 9.1, requires that the short-term phase error during switchover (i.e., Locked to Holdover to Locked) be limited to an accumulation rate no greater than 0.05 ppm during a 15 second interval.

Figure 6. Maximum Time Interval Error of T_{OUT0} Output Port

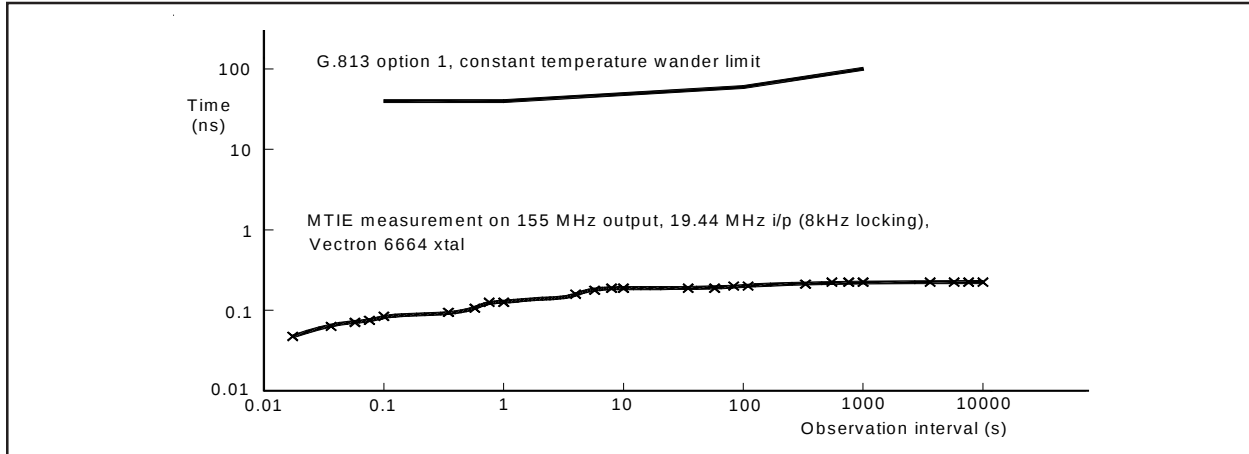


Figure 7. Time Deviation of T_{OUT0} Output Port

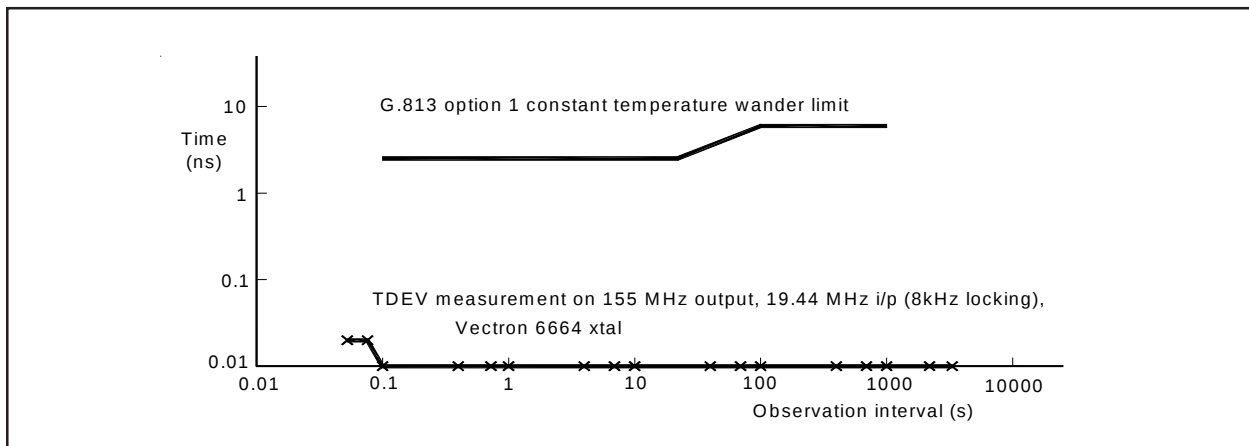
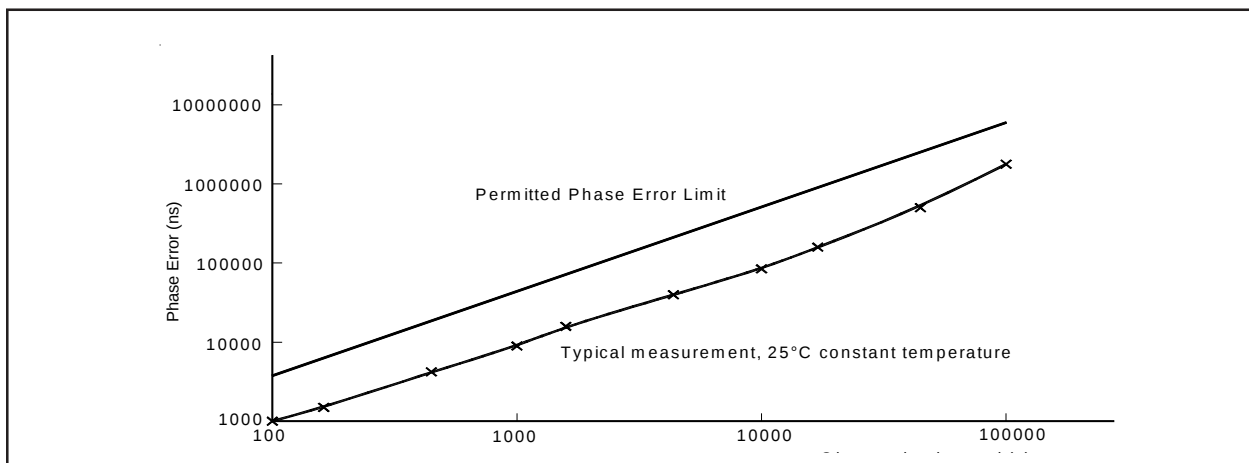


Figure 8. Phase Error Accumulation of T_{OUT0} Output Port in Holdover Mode



2. ETSI 300 462-5, Section 9.2, requires that the long-term phase error in the Holdover mode should not exceed

$$\{(a1+a2)S+0.5bS^2+c\}$$

where

a1 = 50 ns/s (allowance for initial frequency offset)

a2 = 2000 ns/s (allowance for temperature variation)

b = 1.16×10^{-4} ns/s² (allowance for ageing)

c = 120 ns (allowance for entry into Holdover mode).

3. ANSI T1.101-1994, Section 8.2.2, requires that the phase variation be limited so that no more than 255 slips (of 125 µs each) occur during the first day of Holdover. This requires a frequency accuracy better than:

$$((24 \times 60 \times 60) + (255 \times 125 \mu s)) / (24 \times 60 \times 60) = 0.37 \text{ ppm}$$

Temperature variation is not restricted, except to within the normal bounds of 0 to 50 Celsius.

4. Bellcore GR.1244.CORE, Section 5.2., Table 4, shows that an initial frequency offset of 50 ppb is permitted on entering Holdover, whilst a drift over temperature of 280 ppb is allowed; an allowance of 40 ppb is permitted for all other effects.

5. ITU G.822, Section 2.6, requires that the slip rate during category(b) operation (interpreted as being applicable to Holdover mode operation) be limited to less than 30 slips (of 125 µs each) per hour

$$(((60 \times 60) / 30) + 125 \mu s) / (60 \times 60) = 1.042 \text{ ppm}$$

Phase Build Out

Phase Build Out (PBO) is the function to minimise phase transients on the output SEC clock during input reference switching or mode switching. If the currently selected input reference clock source is lost (due to a short interruption, out of frequency detection, or complete loss of reference), the second, next highest priority reference source will be selected. During this transition, the Lost_Phase mode is entered.

The typical phase disturbance on clock reference source switching will be less than 10 ns on the ACS8515. For clock reference switching caused by the main input failing or being disconnected, then the phase disturbance

on the output will still be less than the 120 ns allowed for in the G.813 spec. The actual value is dependant on the frequency being locked to.

The PBO requirement, as specified in Telcordia GR1244-CORE, Section 5.7, in that a phase transient of greater than 3.5 µs occurring in less than 0.1 seconds should be absorbed, will be implemented on a future version. ITU-T G.813 states that the max allowable short term phase transient response, resulting from a switch from one clock source to another, with Holdover mode entered in between, should be a maximum of 1 µs over a 15 second interval. The maximum phase transient or jump should be less than 120 ns at a rate of change of less than 7.5 ppm and the Holdover performance should be better than 0.05 ppm.

On the ACS8515, PBO can be enabled, disabled or frozen using the µP interface. By default, it is enabled. When PBO is enabled, it can also be frozen, which will disable the PBO operation on the next input reference switch, but will remain with the current offset. If PBO is disabled while the device is in the Locked mode, there will be a phase jump on the output SEC clocks as the DPLL locks back to 0 degree phase error.

Microprocessor Interface

The ACS8515 incorporates a serial microprocessor interface that is compatible with the Serial Peripheral Interface (SPI) for device setup.

Register Set

All registers are 8-bits wide, organised with the most-significant bit positioned in the left-most bit, with bit-significance decreasing towards the right-most bit. Some registers carry several individual data fields of various sizes, from single-bit values (e.g., flags) upwards. Several data fields are spread across multiple registers; their organisation is shown in the register map.

Configuration Registers

Each configuration register reverts to a default value on power-up or following a reset. Most default values are fixed, but some will be pin-settable. All configuration registers can be read out over the microprocessor port.

Status Registers

The Status Registers contain readable registers. They may all be read from outside the chip but are not writable from outside the chip (except for a clearing operation). All status registers are read via shadow registers to avoid data hits due to dynamic operation. Each individual status register has a unique location.

Register Access

Most registers are of one of two types, configuration registers or status registers, the exceptions being the *chip_revision* register. Configuration registers may be written to or read from at any time (the complete 8-bit register must be written, even if only one bit is being modified). All status registers may be read at any time and, in some status registers (such as the *sts_interrupts* register), any individual data field may be cleared by writing a '1' into each bit of the field (writing a '0' value into a bit will not affect the value of the bit). Details of each register are given in the Register Map and Register Map Description sections.

Interrupt Enable and Clear

Interrupt requests are flagged on pin INTREQ (active High).

Bits in the interrupt status register are set (high) by the following conditions;

1. Any reference source becoming valid or going invalid
2. A change in the operating state (eg. Locked, Holdover etc.)
3. A brief loss of the currently selected reference source

All interrupt sources are maskable via the mask register *cnfg_interrupt_mask*, each one being enabled by writing a '1' to the appropriate bit.

Any unmasked bit set in the interrupt status register will cause the interrupt request pin to be asserted (high).

All interrupts are cleared by writing a '1' to the bit(s) to be cleared in the status register.

When all pending unmasked interrupts are cleared the interrupt pin will go inactive (low).

The loss of the currently selected reference source will eventually cause the input to be considered invalid, triggering an interrupt. The time taken to raise this interrupt is dependent on the leaky bucket configuration of the activity monitors. The very fastest leaky bucket setting will still take up to 128 ms to trigger the interrupt. The interrupt caused by the brief loss of the currently selected reference source is provided to facilitate very fast source failure detection if desired. It is triggered after missing just a couple of cycles of the reference source.

Register Map

Shaded areas in the map are 'don't care' and writing either 0 or 1 will not affect any function of the device.

Bits labelled 'Set to 0' or 'Set to 1' must be set as stated during initialisation of the device, either following power up, or after a power on reset (PORB). Failure to correctly set these bits may result in the device operating in an unexpected way.

Some registers do not appear in this list, for example 07 and 08. These are either not used, or have test functionality. Do not write to any undefined registers as this may cause the device to operate in a test mode. If an undefined register has been inadvertently addressed, the device should be reset to ensure the undefined registers are at default values.

Table 10. Register Map

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
02	chip_revision (read only)	Chip revision number (7:0)							
03	cnfg_control1 (read/write)			Set to '0'	Analog div sync	Set to '0'	8k Edge Polarity	Set to '0'	Set to '0'
04	cnfg_control2 (read/write)			Phase loss flag limit			Set to '0'	Set to '1'	Set to '0'
05	sts_interrupts (read/write)			SEC2DIFF	SEC1DIFF	SEC2	SEC1		
06		Operating mode	Main ref failed						SEC3
09	sts_operating_mode (read only)						Operating mode (2:0)		
0A	sts_priority_table (read only)	Highest priority valid source				Currently selected reference source			
0B		3 rd highest priority valid source				2 nd highest priority valid source			
0C	sts_curr_inc_offset (read only)	Current increment offset (7:0)							
0D		Current increment offset (15:8)							
07							Current increment offset (18:16)		
0E	sts_sources_valid (read only)			SEC2DIFF	SEC1DIFF	SEC2	SEC1		
0F									SEC3
11	sts_reference_sources (read/write)	status <SEC2>				status <SEC1>			
12		status <SEC2DIFF>				status <SEC1 DIFF>			
14						status <SEC3>			
18	cnfg_ref_selection_priority (read/write)	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'
19		programmed _priority <SEC2>				programmed _priority <SEC1>			
1A		programmed _priority <SEC2DIFF>				programmed _priority <SEC1DIFF>			

Table 10. Register Map (continued).

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
1B	cnfg_ref_selection_priority (read/write) (continued)	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'
1C		Set to '0'	Set to '0'	Set to '0'	Set to '0'	programmed _priority <SEC3>			
1D		Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'
1E		Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'
22	cnfg_ref_source_frequency (read/write)	divn	lock8k	bucket_id <SEC1> (1:0)		reference_source_frequency <SEC1> (3:0)			
23		divn	lock8k	bucket_id <SEC2> (1:0)		reference_source_frequency <SEC2> (3:0)			
24		divn	lock8k	bucket_id <SEC1DIFF> (1:0)		reference_source_frequency <SEC1DIFF> (3:0)			
25		divn	lock8k	bucket_id <SEC2DIFF> (1:0)		reference_source_frequency <SEC2DIFF> (3:0)			
28		divn	lock8k	bucket_id <SEC3> (1:0)		reference_source_frequency <SEC3> (3:0)			
32	cnfg_operating_mode (read/write)						Forced operating mode		
33	cnfg_ref_selection (read/write)					force_select_reference_source			
34	cnfg_mode (read/write)	Auto external 2k enable	Phase alarm timeout enable	Clock edge	Set to '0'	External 2k Sync enable	SONET/ SDH I/P		Revertive mode
35	cnfg_control3 (read/write)			Set to '1'	Set to '0'				
36	cnfg_differential_inputs (read/write)							SEC2DIFF PECL	SEC1DIFF PECL
38	cnfg_output_enable (read/write)	311.04 MHz on O1		1=SONET 0=SDH for Dig1	Set to '0'	Set to '0'	O2 enable	Set to '0'	Set to '0'
39	cnfg_O1_output_frequencies (read/write)			Digital 1					
3A	cnfg_differential_output (read/write)			O1 frequency selection		Set to '0'	Set to '0'	O1 LVDS enable	O1 PECL enable
3B	cnfg_bandwidth (read/write)	Auto b/w switch acq/lock	Acquisition bandwidth			Set to '0'	Normal/locked bandwidth		
3C	cnfg_nominal_frequency (read/write)	Nominal frequency (7:0)							
3D		Nominal frequency (15:8)							
40	cnfg_holdover_offset (read/write)	Set to '0'							
41	cnfg_freq_limit (read/write)	DPLL Frequency offset limit (7:0)							
42								DPLL Frequency offset limit (9:8)	

Table 10. Register Map (continued).

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
43	cnfg_interrupt_mask (read/write)	Set to '0'	Set to '0'	status SEC2DIFF	status SEC1DIFF	status SEC2	status SEC1	Set to '0'	Set to '0'
44		Oper. mode	Main ref	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	status SEC3
45					Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'
46	cnfg_freq_divn (read/write)	Divide-input-by-n ratio (7:0)							
47				Divide-input-by-n ratio (13:8)					
48	cnfg_monitors (read/write)			Ultra-fast switching	External source switch enable	Freeze phase buildout	Phase buildout enable	Frequency monitors configuration (1:0)	
50	cnfg_activ_upper_threshold 0 (read/write)	Configuration 0: Activity alarm set threshold (7:0)							
51	cnfg_activ_lower_threshold 0 (read/write)	Configuration 0: Activity alarm reset threshold (7:0)							
52	cnfg_bucket_size 0 (read/write)	Configuration 0: Activity alarm bucket size (7:0)							
53	cnfg_decay_rate 0 (read/write)								Configuration 0: decay_rate (1:0)
54	cnfg_activ_upper_threshold 1 (read/write)	Configuration 1: Activity alarm set threshold (7:0)							
55	cnfg_activ_lower_threshold 1 (read/write)	Configuration 1: Activity alarm reset threshold (7:0)							
56	cnfg_bucket_size 1 (read/write)	Configuration 1: Activity alarm bucket size (7:0)							
57	cnfg_decay_rate 1 (read/write)								Configuration 1: decay_rate (1:0)
58	cnfg_activ_upper_threshold 2 (read/write)	Configuration 2: Activity alarm set threshold (7:0)							
59	cnfg_activ_lower_threshold 2 (read/write)	Configuration 2: Activity alarm reset threshold (7:0)							
5A	cnfg_bucket_size 2 (read/write)	Configuration 2: Activity alarm bucket size (7:0)							
5B	cnfg_decay_rate 2 (read/write)								Configuration 2: decay_rate (1:0)
5C	cnfg_activ_upper_threshold 3 (read/write)	Configuration 3: Activity alarm set threshold (7:0)							
5D	cnfg_activ_lower_threshold 3 (read/write)	Configuration 3: Activity alarm reset threshold (7:0)							
5E	cnfg_bucket_size 3 (read/write)	Configuration 3: Activity alarm bucket size (7:0)							
5F	cnfg_decay_rate 3 (read/write)								Configuration 3: decay_rate (1:0)

Register Map Description

Table 11. Register Map Description

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
02	chip_revision	This read-only register contains the chip revision number This revision = 1 Last revision (engineering samples) = 0	00000001
03	cnfg_control1	Bits (7:6) Unused Bit 5 =1 32/24MHz to APLL: Feeds 2x Dig2 frequency to the APLL instead of the normal 77.76MHz. Thus the normal OC3/STM1 outputs are replaced with multiple E1/T1 rates. Note: Dig2 set bits (Reg. 39h Bits (7:6)) must be set to 11 for this mode. =0 77.76MHz to APLL Bit 4 =1 Synchronizes the dividers in the output APLL section to the dividers in the DPLL section such that their phases align. This is necessary in order to have phase alignment between inputs and output clocks at OC3 derived rates (6.48 MHz to 77.76 MHz). Keeping this bit high may be necessary to avoid the dividers getting out of synchronization when quick changes in frequency occur such as a force into Free-Run. =0 The dividers may get out of phase following step changes in frequency, but in this mode the correct number of high frequency edges is guaranteed within any synchronization period. The output will frequency lock (default). The device will always remain in synchronization 2 seconds from a reset, before the default setting applies. Bits 3 Test control - leave unchanged, or set to '0' Bit 2 =1 When in 8k locking mode the system will lock to the rising input clock edge. =0 When in 8k locking mode the system will lock to the falling input clock edge. Bits (1:0) Test controls - leave unchanged, or set to '00'	XX000000
04	cnfg_control2	Bits (7:6) Unused. Bits (5:3) define the phase loss flag limit. By default set to 4 (100) which corresponds to approximately 140°. A lower value sets a corresponding lower phase limit. The flag limit determines the value at which the DPLL indicates phase lost as a result of input jitter, a phase jump, or a frequency jump on the input. Bits (2:0) Test controls - leave unchanged or set to '010'.	XX100010
	sts_interrupts	This register contains one bit for each bit of sts_sources_valid, one for loss of reference the device was locked to, and another for the operating mode. All bits are active high. All bits except the 'main ref failed' bit (bit 14) are set on a 'change' in the state of the relevant status bit, i.e. if a source becomes valid, or goes invalid it will trigger an interrupt. If the Operating Mode (register 9) changes state the interrupt will be generated. Bit 14 (main ref failed) of the interrupt status register is used to flag inactivity on the reference that the device is locked to much more quickly than the activity monitors can support. If bit 6 of the cnfg_monitors register (register 48) (flag ref loss on TDO) is set, then the state of this bit is driven onto the TDO pin of the device. All bits are maskable by the bits in the cnfg_interrupt_mask register. Each bit may be cleared individually by writing a '1' to that bit, thus resetting the interrupt. Any number of bits can be cleared with a single write operation. Writing '0's will have no effect.	

Table 11. Register Map Description (continued).

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
05	sts_interrupts (continued)	Bits (7:6) Unused	XX0000XX
		Bit 5 SEC2DIFF (sts_interrupts bit 5)	
		Bit 4 SEC1DIFF (sts_interrupts bit 4)	
		Bit 3 SEC2 (sts_interrupts bit 3)	
		Bit 2 SEC1 (sts_interrupts bit 2)	
		Bits (1:0) Unused	
06		Bits 7 Operating mode (sts_interrupts bit 15)	00XXXXX0
		Bit 6 Main ref failed (sts_interrupts bit 14)	
		Bits (5:1) Unused	
		Bit 0 SEC 3 (sts_interrupts bit 8)	
09	sts_operating_mode	This read-only register holds the current operating state of the main state machine. Figure 10 show how the values of the 'operating state' variable match with the individual states. Bits (7:3) Unused Bits (2:0) State 001 Freerun (default) 010 Holdover 100 Locked 110 Pre-locked 101 Pre-locked2 111 Phase lost	XXXXX001
	sts_priority_table	This is a 16-bit read-only register. Bits (15:12) Third-highest priority valid source: this is the channel number of the input reference source which is valid and has the next-highest priority to the second-highest-priority valid source. Bits (11:8) Second-highest priority valid source: this is the channel number of the input reference source which is valid and has the next-highest priority to the highest-priority valid source. Bits (7:4) Highest-priority valid source: this is the channel number of the input reference source which is valid and has the highest priority; it may not be the same as the currently-selected reference source (due to failure history or changes in programmed priority). Bits (3:0) Currently-selected reference source: this is the channel number of the input reference source which is currently input to the DPLL. Note that these registers are updated by the state machine in response to the contents of the cnfg_ref_selection_priority register and the ongoing status of individual channels; channel number '0000', appearing in any of these registers, indicates that no channel is available for that priority.	
0A		Bits (7:4) Highest-priority valid source (sts_priority_table bits (7:4)) Bits (3:0) Currently selected reference source (sts_priority_table bits (3:0))	00000000
0B		Bits (7:4) 3rd-highest-priority valid source (sts_priority_table bits (15:12)) Bits (3:0) 2nd-highest-priority valid source (sts_priority_table bits (11:8))	00000000
	sts_curr_inc_offset	This read-only register contains a signed-integer value representing the 19 significant bits of the current increment offset of the digital PLL. The register may be read periodically to build up a historical database for later use during holdover periods (this would only be necessary if an external oscillator which did not meet the stability criteria described in Local Oscillator Clock section is used). The register will read 00000000 immediately after reset.	
0C		Bits (7:0) sts_curr_inc_offset bits (7:0)	00000000
0D		Bits (7:0) sts_curr_inc_offset bits (15:8)	00000000
07		Bits (7:3) Unused Bits (2:0) sts_curr_inc_offset bits (18:16)	XXXXX000

Table 11. Register Map Description (continued).

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
	sts_sources_valid	This register contains a bit to show validity for every reference source. =1 Valid source =0 Invalid source (default)	
0E		Bits (7:6) Unused Bit 5 SEC2DIFF Bit 4 SEC1DIFF Bit 3 SEC2 Bit 2 SEC1 Bits (1:0) Unused	XX0000XX
0F		Bits (7:1) Unused Bit 0 SEC3	XXXXXX0
	sts_reference_sources	This register holds the status of each of the input reference sources. The status of each reference source is shown in a 4-bit field. Each bit is active high. To aid status checking, a copy of each status bit 3 is provided in the sts_sources_valid register. The status is reported as follows: (Each bit may be cleared individually) Status bit 3 = Source valid (no alarms) (bit 3 is combination of bits 0-2) (default 0) Status bit 2 = Out-of-band alarm (default 1) Status bit 1 = No activity alarm (default 1) Status bit 0 = Phase lock alarm (default 0)	
11		Bits (7:4) Status of input reference source SEC2 Bits (3:0) Status of input reference source SEC1	01100110
12		Bits (7:4) Status of input reference source SEC2DIFF Bits (3:0) Status of input reference source SEC1DIFF	01100110
14		Bits (7:4) Unused Bits (3:0) Status of input reference source SEC3	XXXX0110
	cnfg_ref_selection_priority	This register holds the priority of each of the input reference sources. The priority values are all relative to each other, with lower-valued numbers taking higher priorities. Only the values 1 to 15 (dec) are valid - '0' disables the reference source. Each reference source must be given a unique priority, however two sources given the same priority number will be assigned on a first in first out basis. It is recommended to reserve the priority value '1' as this is used when forcing reference selection via the cnfg_ref_selection register. If the user does not intend to use the cnfg_ref_selection register then priority value '1' need not be reserved.	
18		Bits (7:0) Must be set to '00000000' during initialisation	00110010
19		Bits (7:4) Programmed priority of input reference source SEC2 Bits (3:0) Programmed priority of input reference source SEC1	01010100
1A		Bits (7:4) Programmed priority of input reference source SEC2DIFF Bits (3:0) Programmed priority of input reference source SEC1DIFF	01110110
1B		Bits (7:0) Must be set to '00000000' during initialisation	10011000
1C		Bits (7:4) Must be set to '0000' during initialisation Bits (3:0) Programmed priority of input reference source SEC3	10111010
1D		Bits (7:0) Must be set to '00000000' during initialisation	11010001
1E		Bits (7:0) Must be set to '00000000' during initialisation	11111110

Table 11. Register Map Description (continued).

Addr. (Hex)	Parameter Name	Description	Default Value (bin)																														
	cnfg_ref_source_frequency	This register is used to set up each of the input reference sources. Bits (7:6) of each byte define the operation undertaken on the input frequency, in accordance with the following key: <table><tr><td>00</td><td>The input frequency is fed directly into the DPLL (default).</td></tr><tr><td>01</td><td>The input frequency is internally divided down to 8 kHz, before being fed into the DPLL. (For high jitter tolerance).</td></tr><tr><td>10</td><td>Unsupported configuration - do not use</td></tr><tr><td>11</td><td>Uses the division coefficient stored in registers 46 & 47 (cnfg_freq_divn) to divide the input by this value prior to being fed into the DPLL. The frequency monitors must be disabled. The divided down frequency should equal 8 kHz. The frequency (3:0) should be set to the nearest spot frequency just below the actual input frequency. The DivN feature works for input frequencies between 1.544 MHz and 100 MHz.</td></tr></table> Bits (5:4) together define which leaky bucket settings (0-3) are used, as defined in registers 50 to 5F. (default 00). Bits (3:0) define the frequency of the reference source in accordance with the following key: <table><tr><td>0000</td><td>8 kHz (default SEC1, SEC2)</td></tr><tr><td>0001</td><td>1544 kHz(SONET)/2048 kHz(SDH) (As defined by Register 34, bit 2)</td></tr><tr><td>0010</td><td>6.48 MHz</td></tr><tr><td>0011</td><td>19.44 MHz (default SEC1DIFF, SEC2DIFF, SEC3)</td></tr><tr><td>0100</td><td>25.92 MHz</td></tr><tr><td>0101</td><td>38.88 MHz</td></tr><tr><td>0110</td><td>51.84 MHz</td></tr><tr><td>0111</td><td>77.76 MHz</td></tr><tr><td>1000</td><td>155.52 MHz</td></tr><tr><td>1001</td><td>2 kHz</td></tr><tr><td>1010</td><td>4 kHz</td></tr></table>	00	The input frequency is fed directly into the DPLL (default).	01	The input frequency is internally divided down to 8 kHz, before being fed into the DPLL. (For high jitter tolerance).	10	Unsupported configuration - do not use	11	Uses the division coefficient stored in registers 46 & 47 (cnfg_freq_divn) to divide the input by this value prior to being fed into the DPLL. The frequency monitors must be disabled. The divided down frequency should equal 8 kHz. The frequency (3:0) should be set to the nearest spot frequency just below the actual input frequency. The DivN feature works for input frequencies between 1.544 MHz and 100 MHz.	0000	8 kHz (default SEC1, SEC2)	0001	1544 kHz(SONET)/2048 kHz(SDH) (As defined by Register 34, bit 2)	0010	6.48 MHz	0011	19.44 MHz (default SEC1DIFF, SEC2DIFF, SEC3)	0100	25.92 MHz	0101	38.88 MHz	0110	51.84 MHz	0111	77.76 MHz	1000	155.52 MHz	1001	2 kHz	1010	4 kHz	
00	The input frequency is fed directly into the DPLL (default).																																
01	The input frequency is internally divided down to 8 kHz, before being fed into the DPLL. (For high jitter tolerance).																																
10	Unsupported configuration - do not use																																
11	Uses the division coefficient stored in registers 46 & 47 (cnfg_freq_divn) to divide the input by this value prior to being fed into the DPLL. The frequency monitors must be disabled. The divided down frequency should equal 8 kHz. The frequency (3:0) should be set to the nearest spot frequency just below the actual input frequency. The DivN feature works for input frequencies between 1.544 MHz and 100 MHz.																																
0000	8 kHz (default SEC1, SEC2)																																
0001	1544 kHz(SONET)/2048 kHz(SDH) (As defined by Register 34, bit 2)																																
0010	6.48 MHz																																
0011	19.44 MHz (default SEC1DIFF, SEC2DIFF, SEC3)																																
0100	25.92 MHz																																
0101	38.88 MHz																																
0110	51.84 MHz																																
0111	77.76 MHz																																
1000	155.52 MHz																																
1001	2 kHz																																
1010	4 kHz																																
22		Frequency of reference source SEC1	00000000																														
23		Frequency of reference source SEC2	00000000																														
24		Frequency of reference source SEC1DIFF	00000011																														
25		Frequency of reference source SEC2DIFF	00000011																														
28		Frequency of reference source SEC3	00000011																														
32	cnfg_operating_mode	This register is used to force the device into a desired operating state, represented by the binary values shown in Figure 10. Value 0 (hex) allows the control state machine to operate automatically. Bits (7:3) Unused Bits (2:0) Desired operating state (as per Figure 10)	XXXXX000																														
33	cnfg_ref_selection	This register is used to force the device to select a particular input reference source, irrespective of its priority. Writing to this register temporarily raises the selected input to priority '1'. Provided no other input is already programmed with priority '1', and revertive mode is on, this source will be selected. Bits (7:4) Unused Bits (3:0) <table><tr><td>0000</td><td>Automatic selection</td></tr><tr><td>0011</td><td>SEC1</td></tr><tr><td>0100</td><td>SEC2</td></tr><tr><td>0101</td><td>SEC1DIFF</td></tr><tr><td>0110</td><td>SEC2DIFF</td></tr><tr><td>1001</td><td>SEC3</td></tr><tr><td>1111</td><td>Automatic selection (default)</td></tr></table> Other values should not be used.	0000	Automatic selection	0011	SEC1	0100	SEC2	0101	SEC1DIFF	0110	SEC2DIFF	1001	SEC3	1111	Automatic selection (default)	XXXX1111																
0000	Automatic selection																																
0011	SEC1																																
0100	SEC2																																
0101	SEC1DIFF																																
0110	SEC2DIFF																																
1001	SEC3																																
1111	Automatic selection (default)																																

Table 11. Register Map Description (continued).

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
34	cnfg_mode	This register contains several individual configuration fields, as detailed below: Bit 7 =1 Auto 2 kHz Sync Enable: External 2 kHz Sync will be enabled only when the source is locked to 6.48 MHz. Otherwise it will be disabled. (default). =0 Auto 2 kHz Sync Disable: The user controls this function using bit 3 of this register, as described below. Bit 6 =1 Phase Alarm Timeout enable: The phase alarm will timeout after 100 seconds. (default). =0 Phase Alarm Timeout disable: The phase alarm will not timeout and must be reset by software. Bit 5 =1 Rising Clock Edge selected: The device will reference to the rising edge of the external oscillator signal. =0 Falling Clock Edge selected: The device will reference to the falling edge of the external oscillator signal (default). Bit 4 Unused. Must be set to '0' during initialisation. Bit 3 =1 External 2 kHz Sync Enable: The device will align the phase of its internally generated Frame Sync signal (8 kHz) and Multi-Frame Sync signal (2 kHz) with that of the signal supplied to the Sync2k pin. This input should be from the 2 kHz Multi-Frame Sync of an ACS8510. =0 External 2 kHz Sync Disable: The device will ignore the Sync2k pin (default). Bit 2 =1 SONET mode: The device expects the input frequency of any input channel given the value '0001' in the cnfg_ref_source_frequency register to be 1544 kHz. =0 SDH mode: The device expects the input frequency of any input channel given the value '0001' in the cnfg_ref_source_frequency register to be 2048 kHz. At start up or reset the bit value will be defaulted to the setting of pin SONSDHB. This setting can subsequently be altered by changing this bit value. Bit 1 Unused Bit 0 = 1 Revertive Mode: The device will switch to the highest priority source shown in sts_priority_table register, bits (7:4). = 0 Non-revertive Mode: The device will retain the presently selected source (default).	110X00X0 (SONSDHB=0) 110X01X0 (SONSDHB=1)
35	cnfg_control3	Bits (7:6) Unused Bits (5:4) Must be set to '10' during initialisation. Bits (3:0) Unused	XX00XXXX
36	cnfg_differential_inputs	This register contains two individual configuration fields Bits (7:2) Unused Bit 1 =1 Input SEC2DIFF is PECL compatible (default) =0 Input SEC2DIFF is LVDS compatible Bit 0 =1 Input SEC1DIFF is PECL compatible =0 Input SEC1DIFF is LVDS compatible (default)	XXXXXX10

Table 11. Register Map Description (continued).

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
38	cnfg_output_enable	This register contains several individual configuration fields, as follows: Bit 7 =1 O1 output frequency set to 311.04 MHz =0 O1 output frequency set by Address 3A (5:4) (default) Bit 6 Unused. Must be set to '0' during initialisation. Bit 5 =1 SONET mode selected for Dig1 =0 SDH mode selected for Dig1 (default) - see register cnfg_O1_output_frequencies Bits (4:3) Unused. Must be set to '0' during initialisation. Bit 2 =1 Output port O2 enabled (19.44 MHz) (default) =0 Output port O2 disabled Bits (1:0) Unused. Must be set to '0' during initialisation. Note: "Disabled" means the output port holds a static logic value (the port is not Tri-stated).	0X0XX1XX
39	cnfg_O1_output_frequencies	This register holds the frequency selections for each output port, as detailed below. Bits (7:6) Unused Bits (5:4) Dig1 00 1544 kHz/2048 kHz (default) 01 3088 kHz/4096 kHz 10 6176 kHz/8192 kHz 11 12352 kHz/16384 kHz Bits (3:2) Unused Bits (1:0) Unused For Dig1 the frequency values are shown for SONET/SDH. They are selected via the SONET/SDH bits in register cnfg_output_enable.	XX00XXXX
3A	cnfg_differential_output	This register holds the frequency selections and the port-technology type for the differential output O1, as detailed below. Bits (7:6) Unused Bits (5:4) O1 00 38.88 MHz (default) 01 19.44 MHz 10 155.52 MHz 11 Dig1 Bits (3:2) Unused Bits (1:0) O1 00 Port disabled 01 PECL-compatible 10 LVDS-compatible (default) 11 Unused	XX00XX10
3B	cnfg_bandwidth	This register contains information used to control the operation of the digital PLL. When bandwidth selection is set to automatic, the DPLL will use the acquisition bandwidth setting when out of lock, and the normal/locked bandwidth setting when in lock. When set to manual, the DPLL will always use the normal/locked bandwidth setting. Bit 7 =1 Automatic operation =0 Manual operation (default) Bits (6:4) Acquisition bandwidth 000 0.1 Hz 001 0.3 Hz 010 0.5 Hz 011 1.0 Hz 100 2.0 Hz 101 4.0 Hz 110 8.0 Hz 111 17 Hz (default) Bit (2:0) Loop bandwidth 000 0.1 Hz 001 0.3 Hz 010 0.5 Hz 011 1.0 Hz 100 2.0 Hz 101 4.0 Hz (default) 110 8.0 Hz 111 17 Hz Bit 3 Unused	0111X101

Table 11. Register Map Description (continued).

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
	cnfg_nominal_frequency	This register holds a 16 bit unsigned integer allowing compensation for offset of the crystal oscillator from the nominal 12.8 MHz. See section Crystal Frequency Calibration. Default results in 0 ppm adjustment.	
3C		Bits (7:0) cnfg_nominal_frequency bits (7:0)	10011001
3D		Bits (7:0) cnfg_nominal_frequency bits (15:8)	10011001
	cnfg_holdover_offset	This register holds 1 bit which must be set to '0' during initialization.	
40		Bit 7 Must be set to '0' during initialization	1XXXXXX
		Bits (6:0) Unused	
	cnfg_freq_limit	This register holds a 10 bit unsigned integer representing the pull-in range of the DPLL. It should be set according to the accuracy of crystal implemented in the application, using the following formula; $\text{Frequency range } \pm (\text{ppm}) = (\text{cnfg_freq_limit} \times 0.0785) + 0.01647 \text{ or}$ $\text{cnfg_freq_limit} = (\text{Frequency range } \pm (\text{ppm}) - 0.01647) / 0.0785$ Default value when SRCSW is left unconnected or tied low is ± 9.3 ppm. Default value when SRCSW is high is the full range of around ± 80 ppm.	
41		Bits (7:0) cnfg_freq_limit bits (7:0)	01110110 (SRCSW low) 11111111 (SRCSW high)
42		Bits (7:2) Unused	XXXXXX00 (SRCSW low)
		Bits (1:0) cnfg_freq_limits bits (9:8)	XXXXXX11 (SRCSW high)
	cnfg_interrupt_mask	Each bit, if set '0' will disable the appropriate interrupt source in the interrupt status register.	
43		Bit (7:6) Must be set to '00' during initialisation Bit 5 Status SEC2DIFF Bit 4 Status SEC1DIFF Bit 3 Status SEC2 Bit 2 Status SEC1 Bit (1:0) Must be set to '00' during initialisation	11111111
44		Bit 7 Oper. mode Bit 6 Main ref Bit (5:1) Must be set to '00000' during initialisation	11111111
45		Bit 0 Interrupt source Bit (7:5) Unused Bit (4:0) Must be set to '00000' during initialisation	XXX11111
	cnfg_freq_divn	This 14 bit integer is used as the divisor for any input to get the phase locking frequency desired. Only active for inputs with the DivN bit set to '1'. This will cause the input frequency to be divided by (n+1) prior to phase comparison, e.g. program N to: $((\text{input freq})/8\text{kHz})-1$ The reference_source_frequency bits should be set to reflect the closest spot frequency to the input frequency, but must be lower than the input frequency.	
46		Bits (7:0) cnfg_freq_divn bits (7:0)	00000000
47		Bits (7:6) Unused	XX000000
		Bits (5:0) cnfg_freq_divn bits (13:8)	

Table 11. Register Map Description (continued).

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
48	cnfg_monitors	This register allows global configuration of monitors and control of phase build out. Bit 7 Unused Bit 6 Unused Bit 5 =1 Enables ultra fast switching: Allows the DPLL to raise an activity alarm on the currently selected source after missing only a few cycles. See section on Ultra Fast Switching. =0 Normal operation (default) Bit 4 =1 Forces locking to SEC1 (pin 29) if pin SRC5W high, or SEC2 (pin 30) if pin SRC5W low =0 Pin SRC5W ignored, and automatic control enabled Bit 3 =1 Will freeze the output phase relationship with the current input to output phase offset =0 Allows changes in input to output phase offset to take place (Normal phase build out mode) (default) Bit 2 =1 Enables phase build out (default) =0 DPLL will allow lock to 0° Bits (1:0) are for configuring frequency monitors- 00 = off, 01 = 15ppm, others are reserved for future use.	X0000101 (SRC5W low) X0010101 (SRC5W high)
50	cnfg_activ_upper_threshold 0	Bits (7:0) set the value in the leaky bucket that causes the activity alarm to be raised.	00000110
51	cnfg_activ_lower_threshold 0	Bits (7:0) set the value in the leaky bucket that causes the activity alarm to be cleared.	00000100
52	cnfg_bucket_size 0	Bits (7:0) set the maximum value that the leaky bucket can reach given an inactive input.	00001000
53	cnfg_decay_rate 0	Bits (7:2) Unused Bits (1:0) control the leak rate of the leaky bucket. The fill-rate of the bucket is +1 for every 128 ms interval that has experienced some level of inactivity. The decay rate is programmable in ratios of the fill rate. The ratio can be set to 1:1, 2:1, 4:1, 8:1 by using values of 00, 01, 10, 11 respectively. However, these buckets are not 'true' leaky buckets in nature. The bucket stops 'leaking' when it is being filled. This means that the fill and decay rates can be the same (00 = 1:1) with the net effect that an active input can be recognised at the same rate as an inactive one.	XXXXXX01
54	cnfg_activ_upper_threshold 1	As for register 50 but for bucket 1.	00000110
55	cnfg_activ_lower_threshold 1	As for register 51 but for bucket 1.	00000100
56	cnfg_bucket_size 1	As for register 52 but for bucket 1.	00001000
57	cnfg_decay_rate 1	As for register 53 but for bucket 1.	XXXXXX01
58	cnfg_activ_upper_threshold 2	As for register 50 but for bucket 2.	00000110
59	cnfg_activ_lower_threshold 2	As for register 51 but for bucket 2.	00000100
5A	cnfg_bucket_size 2	As for register 52 but for bucket 2.	00001000
5B	cnfg_decay_rate 2	As for register 53 but for bucket 2.	XXXXXX01
5C	cnfg_activ_upper_threshold 3	As for register 50 but for bucket 3.	00000110
5D	cnfg_activ_lower_threshold 3	As for register 51 but for bucket 3.	00000100
5E	cnfg_bucket_size 3	As for register 52 but for bucket 3.	00001000
5F	cnfg_decay_rate 3	As for register 53 but for bucket 3.	XXXXXX01

Selection of Input Reference Clock Source

Under normal operation, the input reference sources are selected automatically by an order of priority, where SEC1 is the highest priority, SEC2 is the second highest priority and SEC3 is the lowest priority. The priorities can be re-assigned with external software. The SEC1 reference source has inputs via either a low speed TTL input port or a high speed PECL/LVDS input port. Similarly, the SEC2 reference source has both a low speed TTL or a high speed PECL/LVDS input port. The SEC3 (standby) reference source only has provision via a low speed TTL input port. There is provision for one sync clock input via a TTL port. Whilst SEC1, SEC2 and SEC3 reference source inputs can all be active at the same time, only one of the TTL or PECL/LVDS input ports for the SEC1 and SEC2 reference sources may be used at any time, the inactive port is ignored, by setting the priority of that port to zero.

Restoration of repaired reference sources is handled carefully to avoid inadvertent disturbance of the output clock. The ACS8510 has two modes of operation; Revertive and Non-Revertive. In Revertive mode, if a re-validated (or newly validated) source has a higher priority than the reference source which is currently selected, a switch over will take place. Many applications prefer to minimise the clock switching events and choose Non-Revertive mode. In Non-Revertive mode, when a re-validated (or newly validated) source has a higher priority than the selected source will be maintained. The re-validation of the reference source will be flagged in the `sts_sources_valid` register and, if not masked, will generate an interrupt. Selection of the re-validated source can only take place under software control - the software should briefly enable Revertive mode to affect a switch-over to the higher priority source. If the selected source fails under these conditions the device will indicate that it is still locked to the failed reference. It will not select the higher priority source until instructed

to do so by the software; by briefly setting the Revertive mode bit. When there is a reference available with higher priority than the selected reference, there will be NO change of reference source as long as the Non-Revertive mode remains on AND the device will remain indicating a locked state on the failed reference. This is the case even if there are lower priority references available or the currently selected reference fails. When the ONLY valid reference sources that are available have a lower priority than the selected reference, a failure of the selected reference will always trigger a switch-over, regardless of whether Revertive or Non-Revertive mode has been chosen.

Automatic Control Selection

When automatic selection is required, the `cnfg_ref_selection` registers must be set to all-zero or all-one. The configuration registers, `cnfg_ref_selection_priority`, held in the μ P port are organised as 5, 4-bit registers with each representing an input reference port. Unused ports should be given the value '0000' in the relevant register to indicate they are not to be included in the priority table. On power-up, or following a reset, the whole of the configuration file will be defaulted to the values defined by Table 4. The selection priority values are all relative to each other, with lower-valued numbers taking higher priorities. Each reference source should be given a unique number, the valid values are 1 to 15 (dec). A value of 0 disables the reference source. However if two or more inputs are given the same priority number those inputs will be selected on a first in, first out basis. If the first of two same priority number sources goes invalid the second will be switched in. If the first then becomes valid again, it becomes the second source on the first in, first out basis, and there will not be a switch. If a third source with the same priority number as the other two becomes valid, it joins the priority list on the same first in, first out basis. There is no implied priority based on the channel numbers.

Ultra Fast Switching

A reference source is normally disqualified after the leaky bucket monitor thresholds have been crossed. An option for a faster disqualification has been implemented, whereby if register 48H, bit 5 (Ultra Fast Switching), is set then a loss of activity of just a few reference clock cycles will set the 'no activity alarm' and cause a reference switch. This can be chosen to cause an interrupt to occur instead of, or as well as, causing the reference switch.

External Protection Switching

Fast external switching between inputs SEC1 and SEC2 can also be triggered directly from a dedicated pin (SRCSW). This mode can be activated either by holding this pin high during reset, or by writing to bit 4 of register address 48Hex.

Once external protection switching is enabled, then the value of this pin directly selects either SEC1 (SRCSW high) or SEC2 (SRCSW low). If this mode is activated at reset by pulling the SRCSW pin high, then it configures the default frequency tolerance of SEC1 and SEC2 to ± 80 ppm (register address 41Hex and 42Hex).

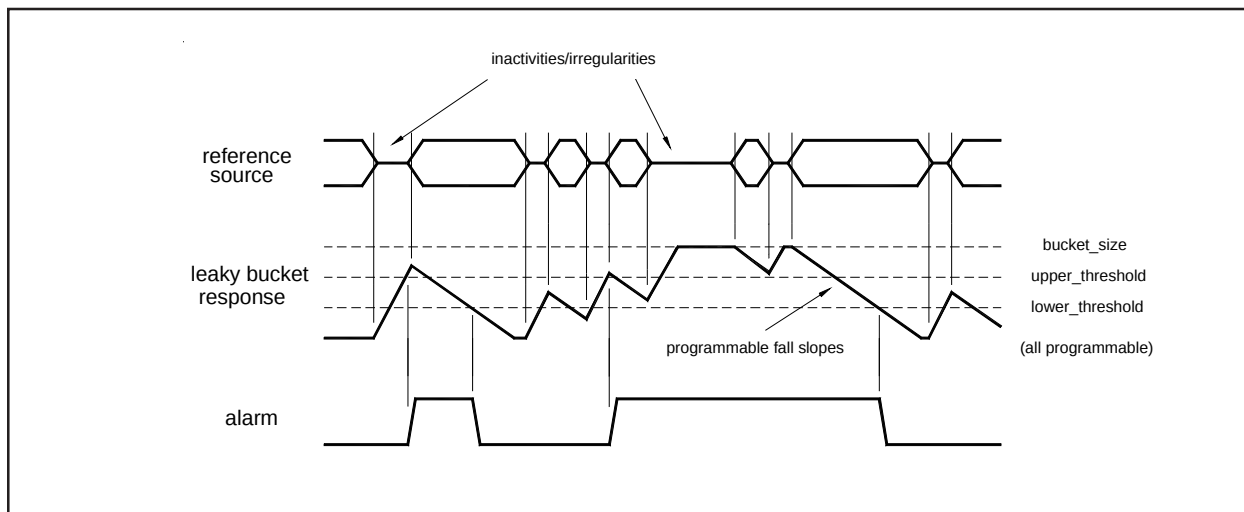
Any of these registers can be subsequently set by external s/w if required.

When external protection switching is enabled, the device will operate as a simple switch. All clock monitoring is disabled and the DPLL will simply be forced to try to lock on to the indicated reference source. The operating state (*sts_operating_mode* register) will always indicate 'locked' in the mode.

Activity Monitoring

The ACS8515 has a combined inactivity and irregularity monitor. The ACS8515 uses a 'leaky bucket' accumulator, which is a digital circuit which mimics the operation of an analog integrator, in which input pulses increase the output amplitude but die away over time. Such integrators are used when alarms have to be triggered either by fairly regular defect events, which occur sufficiently close together, or by defect events which occur in bursts. Events which are sufficiently spread out should not trigger the alarm. By controlling the alarm-setting threshold, the point at which the alarm is triggered can be controlled. The point at which

Figure 9. Inactivity and Irregularity Monitoring



the alarm is cleared depends upon the decay rate and the alarm-clearing threshold. On the alarm-setting side, if several events occur close together, each event adds to the amplitude and the alarm will be triggered quickly; if events occur a little more spread out, but still sufficiently close together to overcome the decay, the alarm will be triggered eventually. If events occur at a rate which is not sufficient to overcome the decay, the alarm will not be triggered. On the alarm-clearing side, if no defect events occur for a sufficient time, the amplitude will decay gradually and the alarm will be cleared when the amplitude falls below the alarm-clearing threshold. The ability to decay the amplitude over time allows the importance of defect events to be reduced as time passes by. This means that, in the case of isolated events, the alarm will not be set, whereas, once the alarm becomes set, it will be held on until normal operation has persisted for a suitable time (but if the operation is still erratic, the alarm will remain set). See Figure 9.

The 'leaky bucket' accumulators are programmable for size, alarm set & reset thresholds and decay rate. Each source is monitored over a 128 ms period. If, within a 128 ms period, an irregularity occurs that is not deemed to be due to allowable jitter/wander, then the accumulator is incremented. The accumulator will continue to increment up to the point that it reaches the programmed bucket size. The 'fill rate' of the leaky bucket is, therefore, 8 units/second. The "leak rate" of the leaky bucket is programmable to be in multiples of the fill rate (x1, x0.5, x0.25 and x0.125) to give a programmable leak rate from 8 units/sec down to 1 unit/sec. A conflict between trying to 'leak' at the same time as a 'fill' is avoided by preventing a 'leak' when a 'fill' event occurs.

Disqualification of a non-selected reference source is based on inactivity, or on an out of band result from the frequency monitors. The currently selected reference source can be

Leaky bucket timing

The time taken to raise an inactivity alarm on a reference source that has previously been fully active (leaky bucket empty) will be:

$$\frac{(\text{cnfg_activ_upper_threshold } N)}{8} \quad \text{secs}$$

where N is the number of the relevant leaky bucket configuration. If an input is intermittently inactive then this time can be longer. The default setting of *cnfg_activ_upper_threshold* is 6, therefore the default time is 0.75 s.

The time taken to cancel the activity alarm on a previously completely inactive reference source is calculated as:

$$\frac{2^{(\text{cnfg_decay_rate } N)} \times ((\text{cnfg_bucket_size } N) - (\text{cnfg_activ_lower_threshold } N))}{8} \quad \text{secs}$$

where N is the number of the relevant leaky bucket configuration in each case. The default settings are shown in the following:

$$\frac{2^1 \times (8-4)}{8} = 1.0 \text{ s}$$

disqualified for phase, frequency, inactivity or if the source is outside the DPLL lock range. If the currently selected reference source is disqualified, the next highest priority, active reference source is selected.

Restoration of repaired reference sources is handled carefully to avoid inadvertent disruption of the output clock. The ACS8515 operates in a Non-Revertive mode by default. In this mode, if the restored reference source has a higher priority than the reference source which is currently selected, a switch-over to the restored source will not take place automatically. A restored reference source will assume its correct place in the priority table but a switch-over will only take place automatically upon failure of the currently selected source. It is possible to invoke a switch-over by external control or by enabling Revertive mode.

Modes of Operation

The ACS8515 has three primary modes of operation (Free-run, Locked and Holdover) supported by three secondary, temporary modes (Pre-Locked, Lost_Phase and Pre-Locked2). These are shown in the State Transition Diagram, Figure 10.

The ACS8515 can operate in Forced or Automatic control. On reset, the ACS8515 reverts to Automatic Control, where transitions between states are controlled completely automatically. Forced Control can be invoked by configuration, allowing transitions to be performed under external control. This is not the normal mode of operation, but is provided for special occasions such as testing, or where a high degree of hands-on control is required.

Free-run Mode

The Free-run mode is typically used following a power-on-reset or a device reset before network synchronization has been achieved. In

the Free-run mode, the timing and synchronization signals generated from the ACS8515 are based on the Master clock frequency provided from the external oscillator and are not synchronized to an input reference source. The frequency of the output clock is a fixed multiple of the frequency of the external oscillator, and the accuracy of the output clock is equal to the accuracy of the Master clock.

The transition from Free-run to Pre-locked occurs when the ACS8515 selects a reference source.

Pre-Locked Mode

The ACS8515 will enter the Locked state in a maximum of 100 seconds, as defined by GR-1244-CORE specification, if the selected reference source is of good quality. If the device cannot achieve lock within 100 seconds, it reverts to Free-run mode and another reference source is selected.

Locked Mode

The Locked mode is used when an input reference source has been selected and the PLL has had time to lock. When the Locked mode is achieved, the output signal is in phase and locked to the selected input reference source. The selected input reference source is determined by the priority table. When the ACS8515 is in Locked mode, the output frequency and phase follows that of the selected input reference source. Variations of the external crystal frequency have a minimal effect on the output frequency. Only the minimum to maximum frequency range is affected. Note that the term, 'in phase', is not applied in the conventional sense when the ACS8515 is used as a frequency translator (e.g., when the input frequency is 2.048 MHz and the output frequency is 19.44 MHz) as the input and output cycles will be constantly moving past each other; however, this variation will itself be cyclical over time unless the input and output are not locked.

Lost-Phase Mode

Lost-phase mode is entered when the current phase error, as measured within the DPLL, is larger than a preset limit (see register 04, bits 5:3), as a result of a frequency or phase transient on the selected reference source. This mode is similar in behavior to the Pre-locked or Pre-locked(2) modes, although in this mode the DPLL is attempting to regain lock to the same reference rather than attempt lock to a new reference. If the DPLL cannot regain lock within 100 s, the source is disqualified, and one of the following transitions takes place:

1. Go to Pre-Locked(2);
 - If a known-good standby source is available.
2. Go to Holdover;
 - If no standby sources are available.

Holdover Mode

The Holdover mode is used when the circuit was in Locked mode but the selected reference source has become unavailable and a replacement has not yet been selected.

Holdover freezes the DPLL at the current frequency (as reported by the *sts_curr_inc_offset* register). The proportional DPLL path is ignored so that recent signal disturbances do not affect the Holdover frequency value.

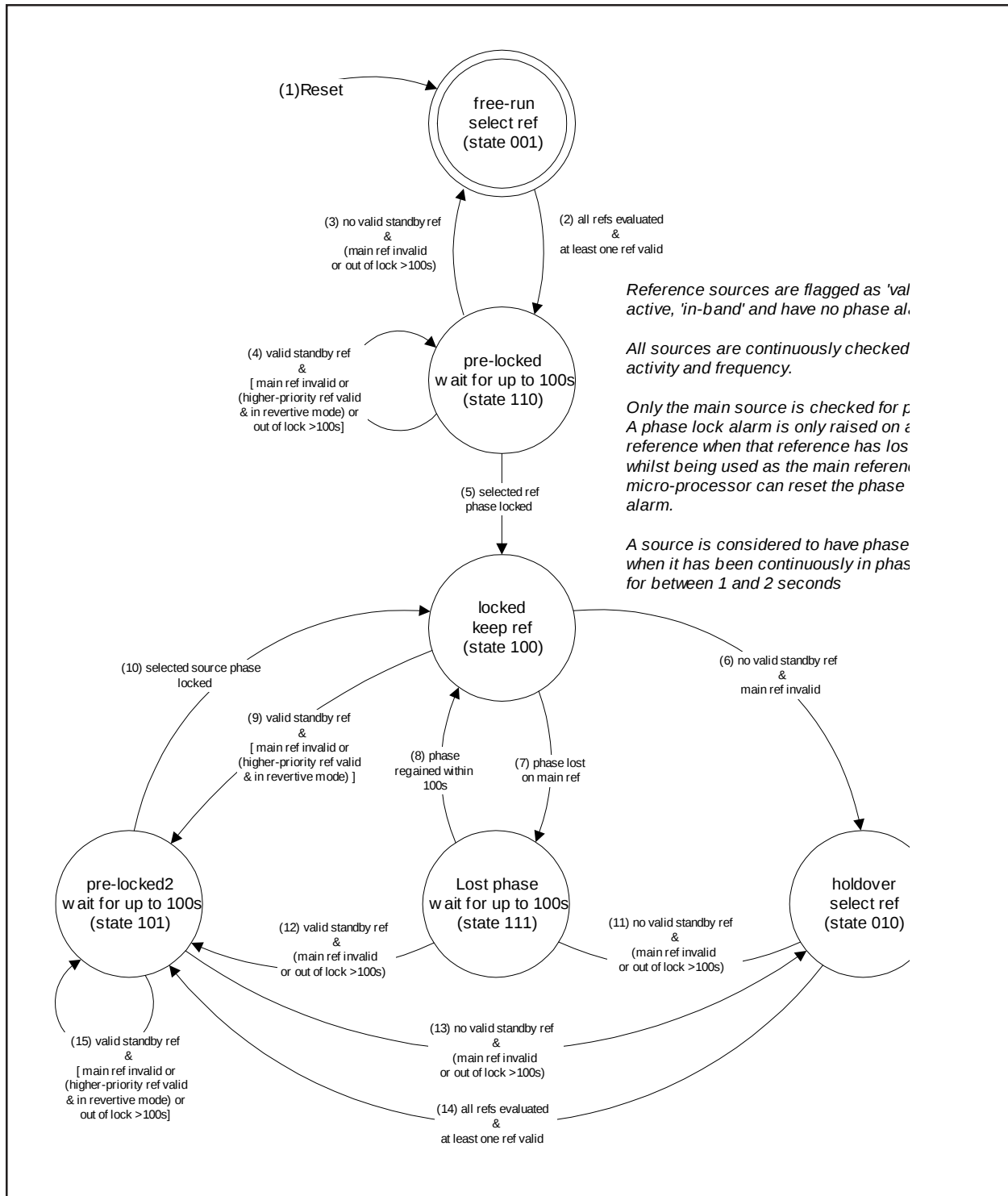
Pre-Locked(2) Mode

This state is very similar to the Pre-Locked state. It is entered from the Holdover state when a reference source has been selected and applied to the phase locked loop. It is also entered if the device is operating in Revertive mode and a higher-priority reference source is restored.

Power On Reset - PORB

The Power On Reset (PORB) pin resets the device if forced Low for a power-on-reset to be initiated. The reset is asynchronous, the minimum low pulse width is 5 ns. Reset is needed to initialize all of the register values to their defaults. Asserting Reset (POR) is required at power on, and may be re-asserted at any time to restore defaults. This is implemented most simplistically by an external capacitor to GND along with the internal pull-up resistor. The ACS8515 is held in a reset state for 250 ms after the PORB pin has been pulled High. In normal operation PORB should be held High.

Figure 10. Automatic Mode Control State Diagram



Electrical Specification

Important Note: The 'Absolute Maximum Ratings' are stress ratings only, and functional operation of the device at conditions other than those indicated in the 'Operating Conditions' sections of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

Table 12. Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage $V_{DD}, V_{D+}, V_{A1+}, V_{A2+}$	V_{DD}	-0.5	3.6	V
Input Voltage (non-supply pins)	V_{in}	-	5.5	V
Output Voltage (non-supply pins)	V_{out}	-	5.5	V
Ambient Operating Temperature Range	T_A	-40	85	°C
Storage Temperature	T_{stor}	-50	150	°C

Table 13. Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply (dc voltage) $V_{DD}, V_{D+}, V_{A1+}, V_{A2+}, V_{DD_DIFF}$	VDD	3.0	3.3	3.6	V
Power Supply (dc voltage) VDD5	VDD5	3.0	3.3/5.0	5.5	V
Ambient Temperature Range	T_A	-40	-	85	°C
Supply Current Typical - one 19 MHz output Maximum - 190 mA before s/w initialisation, 150 mA after s/w initialisation	IDD	-	110	190/150	mA
Total power dissipation	P_{TOT}	-	360	685	mW

Table 14. DC Characteristics: TTL Input Pad

Across all operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{in} High	V_{ih}	2.0	-	-	V
V_{in} Low	V_{il}	-	-	0.8	V
Input Current	I_{in}	-	-	10	μA

Table 15. DC Characteristics: TTL Input Pad with Internal Pull-up

Across all operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{in} High	V_{ih}	2.0	-	-	V
V_{in} Low	V_{il}	-	-	0.8	V
Pull-up Resistor	PU	30	-	80	k Ω
Input Current	I_{in}	-	-	120	μ A

Table 16. DC Characteristics: TTL Input Pad with Internal Pull-down

Across all operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{in} High	V_{ih}	2.0	-	-	V
V_{in} Low	V_{il}	-	-	0.8	V
Pull-down Resistor	PD	30	-	80	k Ω
Input Current	I_{in}	-	-	120	μ A

Table 17. DC Characteristics: TTL Output Pad

Across all operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Vout Low $I_{ol} = 4\text{mA}$	V_{ol}	0	-	0.4	V
Vout High $I_{oh} = 4\text{mA}$	V_{oh}	2.4	-		V
Drive Current	ID	-	-	4	mA

Table 18. DC Characteristics: PECL Input/Output Pad

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
PECL Input Low voltage Differential inputs (Note 1)	V_{ILPECL}	VDD-2.5	-	VDD-0.5	V
PECL Input High voltage Differential inputs (Note 1)	V_{IHPECL}	VDD-2.4	-	VDD-0.4	V
Input Differential voltage	V_{IDPECL}	0.1	-	1.4	V
PECL Input Low voltage Single ended input (Note 2)	V_{ILPECL_S}	VDD-2.4	-	VDD-1.5	V
PECL Input High voltage Single ended input (Note 2)	V_{IHPECL_S}	VDD-1.3	-	VDD-0.5	V
Input High current Input differential voltage $V_{ID} = 1.4V$	I_{IHPECL}	-10	-	+10	μA
Input Low current Input differential voltage $V_{ID} = 1.4V$	I_{ILPECL}	-10	-	+10	μA
PECL Output Low voltage (Note 3)	V_{OLPECL}	VDD-2.10	-	VDD-1.62	V
PECL Output High voltage (Note 3)	V_{OHPECL}	VDD-1.25	-	VDD-0.88	V
PECL Output Differential voltage (Note 1)	V_{ODPECL}	580	-	900	mV

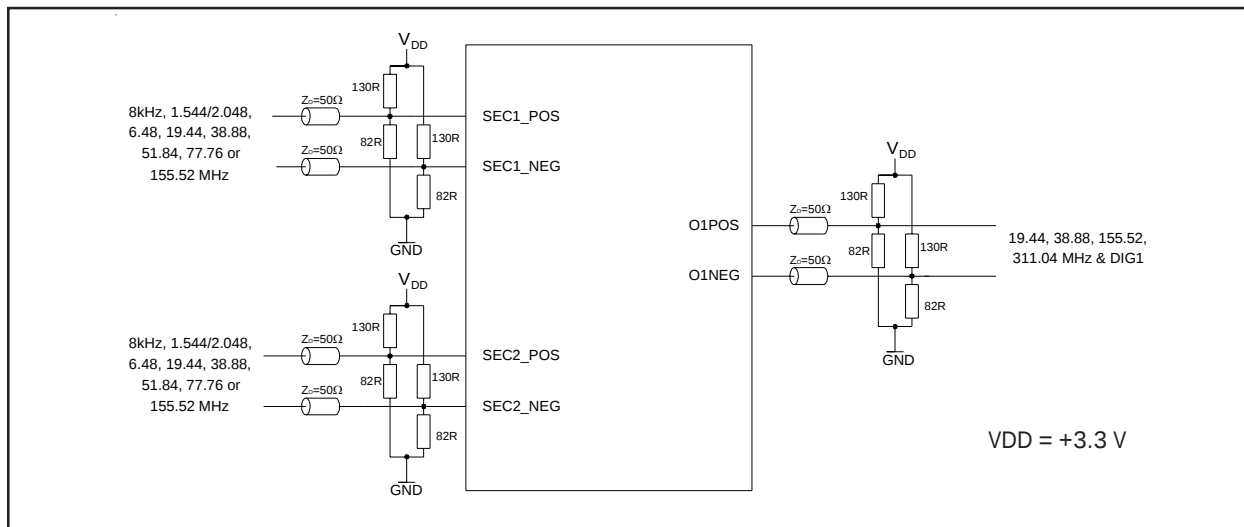
Notes for Table 18

Unused differential input ports should be left floating and set in LVDS mode, or the positive and negative inputs tied to VDD and GND respectively.

Note 1. Assuming a differential input voltage of at least 100 mV.

Note 2. Unused differential input terminated to VDD-1.4 V.

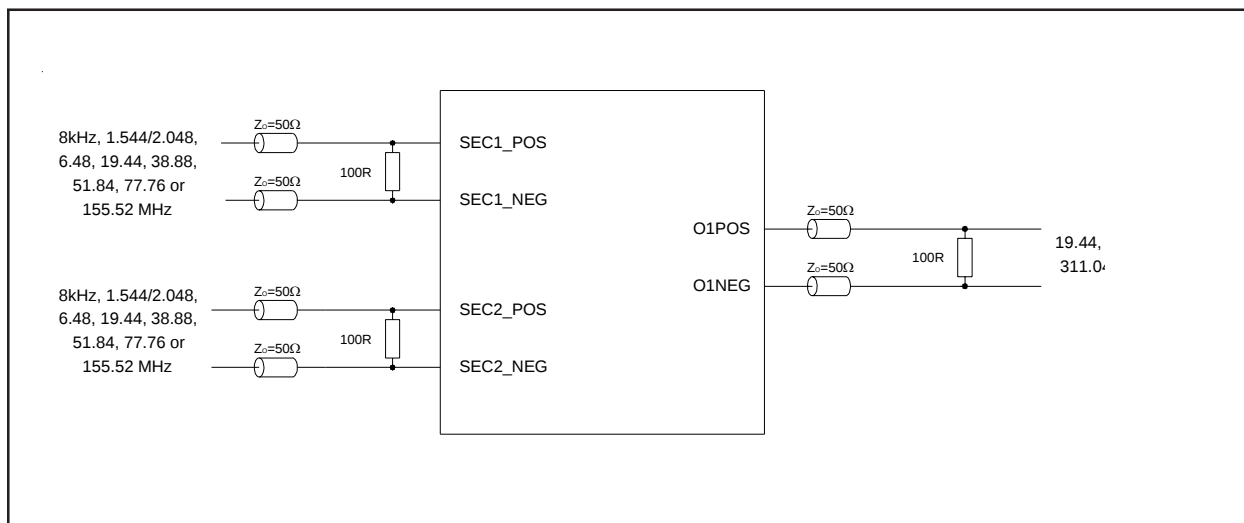
Note 3. With 50 Ω load on each pin to VDD-2 V . i.e. 82 Ω to GND and 130 Ω to VDD.

Figure 11. Recommended Line Termination for PECL Input/Output Ports

Table 19. DC Characteristics: LVDS Input/Output Pad

Across all operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
LVDS Input voltage range Differential input voltage = 100 mV	V _{VRLVDS}	0	-	2.40	V
LVDS Differential input threshold	V _{DITH}	-100	-	+100	mV
LVDS Input Differential voltage	V _{IDLVDS}	0.1	-	1.4	V
LVDS Input termination resistance Must be placed externally across the LVDS+/- input pins of ACS8515. Resistor should be 100 ohm with 5% tolerance	R _{TERM}	95	100	105	W
LVDS Output high voltage (Note 1)	V _{OHLVDS}	-	-	1.585	V
LVDS Output low voltage (Note 1)	V _{OLLVDS}	0.885	-	-	V
LVDS Differential output voltage (Note 1)	V _{ODLVDS}	250	-	450	mV
LVDS Charge in magnitude of differential output voltage for complimentary states (Note 1)	V _{DOSLVDS}	-	-	25	mV
LVDS output offset voltage Temperature = 25 °C (Note 1)	V _{OSLVDS}	1.125	-	1.275	V

Note 1. With 100 Ω load between the differential outputs.

Figure 12. Recommended Line Termination for LVDS Input/Output Ports

Table 20. DC Characteristics: Output Jitter Generation (Test definition G.813)

Across all operating conditions, unless otherwise stated

Output jitter generation measured over 60 seconds interval, UI pp max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

TEST DEFINITION	FILTER USED	UI SPEC	UI MEASUREMENT ON ACS8515 REV 2
G.813 for 155.52 MHz option 1	500 Hz to 1.3 MHz	$UI_{pp} = 0.5$	0.058 (Note 2)
G.813 for 155.52 MHz option 1	65 kHz to 1.3 MHz	$UI_{pp} = 0.1$	0.048 (Note 3) 0.048 (Note 2)
G.813 for 155.52 MHz option 2	12 kHz to 1.3 MHz	$UI_{pp} = 0.1$	0.053 (Note 4) 0.053 (Note 5)
			0.058 (Note 6) 0.053 (Note 7)
			0.053 (Note 2) 0.058 (Note 3)
			0.057 (Note 8) 0.055 (Note 9)
			0.057 (Note 10) 0.057 (Note 11)
			0.057 (Note 12) 0.053 (Note 13)
G.813 & G.812 for 2.048 MHz option 1	20 Hz to 100 kHz	$UI_{pp} = 0.05$	0.046 (Note 14)

Table 21. DC Characteristics: Output Jitter Generation (Test definition G.812)

Across all operating conditions, unless otherwise stated

Output jitter generation measured over 60 seconds interval, UI pp max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

TEST DEFINITION	FILTER USED	UI SPEC	UI MEASUREMENT ON ACS8515 REV 2
G.812 for 1.544 MHz	10 Hz to 40 kHz	$UI_{pp} = 0.05$	0.036 (Note 14)
G.812 for 155.52 MHz electrical	500 Hz to 1.3 MHz	$UI_{pp} = 0.5$	0.058 (Note 3)
G.812 for 2.048 MHz electrical	65 kHz to 1.3 MHz	$UI_{pp} = 0.075$	0.048 (Note 3)

Table 22. DC Characteristics: Output Jitter Generation (Test definition ETS-300-462-3)

Across all operating conditions, unless otherwise stated

Output jitter generation measured over 60 seconds interval, UI pp max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

TEST DEFINITION	FILTER USED	UI SPEC	UI MEASUREMENT ON ACS8515 REV 2
ETS-300-462-3 for 2.048 MHz SEC	20 Hz to 100 kHz	$UI_{pp} = 0.5$	0.046 (Note 14)
ETS-300-462-3 for 2.048 MHz SEC (Filter spec 49 Hz to 100 kHz)	20 Hz to 100 kHz	$UI_{pp} = 0.2$	0.046 (Note 14)
ETS-300-462-3 for 2.048 MHz SSU	20 Hz to 100 kHz	$UI_{pp} = 0.05$	0.046 (Note 14)
ETS-300-462-3 for 155.52 MHz	500 Hz to 1.3 MHz	$UI_{pp} = 0.5$	0.058 (Note 3)
ETS-300-462-3 for 155.52 MHz	65 kHz to 1.3 MHz	$UI_{pp} = 0.1$	0.048 (Note 3)

Table 23. DC Characteristics: Output Jitter Generation (Test definition GR-253-CORE)

Across all operating conditions, unless otherwise stated

Output jitter generation measured over 60 seconds interval, UI pp max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

TEST DEFINITION	FILTER USED	UI SPEC	UI MEASUREMENT ON ACS8515 REV 2
GR-253-CORE net i/f, 51.84 MHz	100 Hz to 400 kHz	UI _{pp} = 1.5	0.022 (Note 3)
GR-253-CORE net i/f, 51.84 MHz (Filter spec 20 kHz to 400 kHz)	18 kHz to 400 kHz	UI _{pp} = 0.15	0.019 (Note 3)
GR-253-CORE net i/f, 155.52 MHz	500 Hz to 1.3 MHz	UI _{pp} = 1.5	0.058 (Note 3)
GR-253-CORE net i/f, 155.52 MHz	65 kHz to 1.3 MHz	UI _{pp} = 0.15	0.048 (Note 3)
GR-253-CORE cat II elect i/f, 155.52 MHz	12 kHz to 1.3 MHz	UI _{pp} = 0.1	0.058 (Note 3)
		UI _{rms} = 0.01	0.006 (Note 3)
GR-253-CORE cat II elect i/f, 51.84 MHz	12 kHz to 400 kHz	UI _{pp} = 0.1	0.017 (Note 3)
		UI _{rms} = 0.01	0.003 (Note 3)
GR-253-CORE DS1 i/f, 1.544 MHz	10 Hz to 40 kHz	UI _{pp} = 0.1	0.036 (Note 14)
		UI _{rms} = 0.01	0.0055 (Note 14)

Table 24. DC Characteristics: Output Jitter Generation (Test definition AT&T 62411)

Across all operating conditions, unless otherwise stated

Output jitter generation measured over 60 seconds interval, UI pp max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

TEST DEFINITION	FILTER USED	UI SPEC	UI MEASUREMENT ON ACS8515 REV 2
AT&T 62411 for 1.544 MHz (Filter spec 10 Hz to 8 kHz)	10 Hz to 40 kHz	UI _{rms} = 0.02	0.0055 (Note 14)
AT&T 62411 for 1.544 MHz	10 Hz to 40 kHz	UI _{rms} = 0.025	0.0055 (Note 14)
AT&T 62411 for 1.544 MHz	10 Hz to 40 kHz	UI _{rms} = 0.025	0.0055 (Note 14)
AT&T 62411 for 1.544 MHz	Broadband	UI _{rms} = 0.05	0.0055 (Note 14)

Table 25. DC Characteristics: Output Jitter Generation (Test definition G.742)

Across all operating conditions, unless otherwise stated

Output jitter generation measured over 60 seconds interval, UI pp max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

TEST DEFINITION	FILTER USED	UI SPEC	UI MEASUREMENT ON ACS8515 REV 2
G.742 for 2.048 MHz	DC to 100 kHz	$UI_{pp} = 0.25$	0.047 (Note 14)
G.742 for 2.048 MHz (Filter spec 18 kHz to 100 kHz)	20 Hz to 100 kHz	$UI_{pp} = 0.05$	0.046 (Note 14)
G.742 for 2.048 MHz	20 Hz to 100 kHz	$UI_{pp} = 0.05$	0.046 (Note 14)

Table 26. DC Characteristics: Output Jitter Generation (Test definition TR-NWT-000499)

Across all operating conditions, unless otherwise stated

Output jitter generation measured over 60 seconds interval, UI pp max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

TEST DEFINITION	FILTER USED	UI SPEC	UI MEASUREMENT ON ACS8515 REV 2
TR-NWT-000499 & G.824 for 1.544 MHz	10 Hz to 40 kHz	$UI_{pp} = 5.0$	0.036 (Note 14)
TR-NWT-000499 & G.824 for 1.544 MHz (Filter spec 8 kHz to 40 kHz)	10 Hz to 40 kHz	$UI_{pp} = 0.1$	0.036 (Note 14)

Table 27. DC Characteristics: Output Jitter Generation (Test definition GR-1244-CORE)

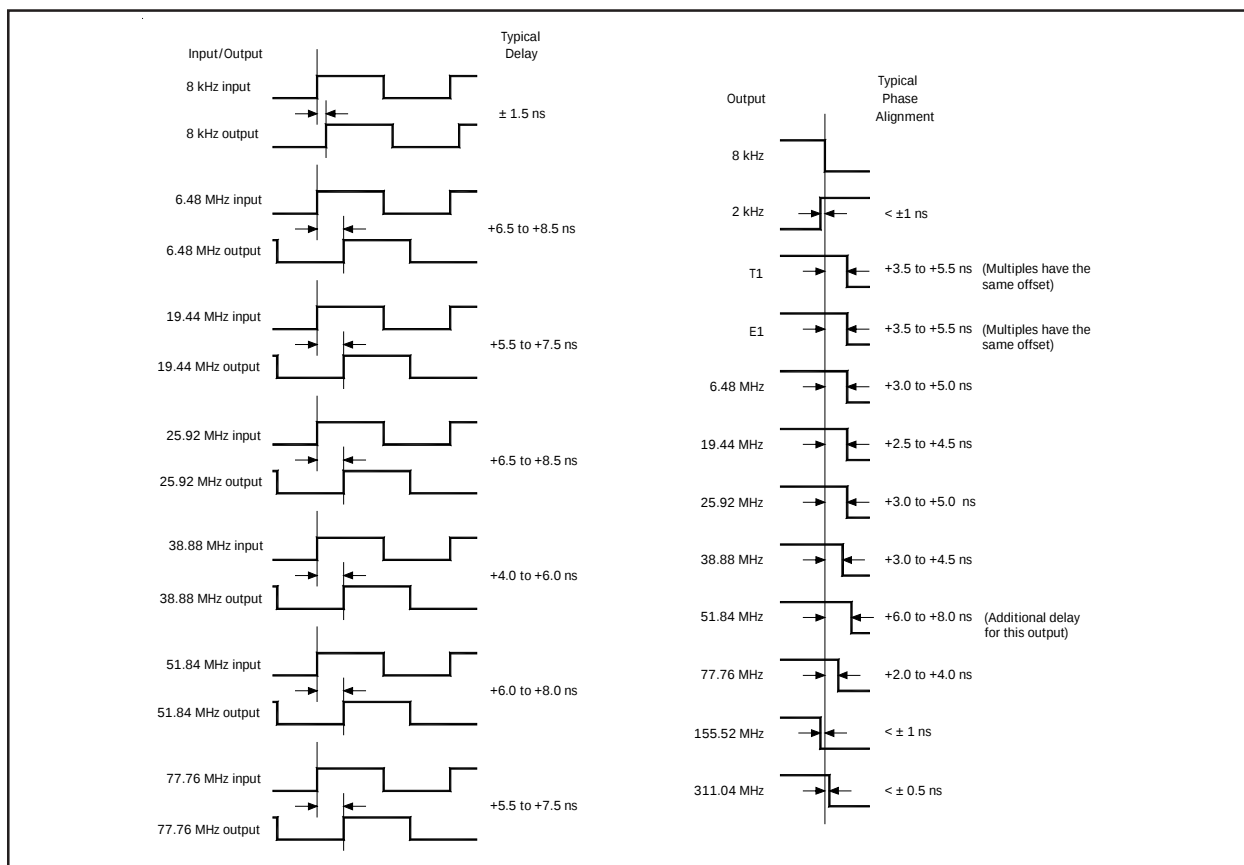
Across all operating conditions, unless otherwise stated

Output jitter generation measured over 60 seconds interval, UI pp max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

TEST DEFINITION	FILTER USED	UI SPEC	UI MEASUREMENT ON ACS8515 REV 2
GR-1244-CORE for 1.544 MHz	>10 Hz	$UI_{pp} = 0.05$	0.036 (Note 14)

Notes for tables 20 - 227

- Note 1. Filter used is that defined by test definition unless otherwise stated
- Note 2. 5 Hz bandwidth, 19.44 MHz input, direct lock
- Note 3. 5 Hz bandwidth, 19.44 MHz input, 8 kHz lock
- Note 4. 20 Hz bandwidth, 19.44 MHz input, direct lock
- Note 5. 20 Hz bandwidth, 19.44 MHz input, 8 kHz lock
- Note 6. 10 Hz bandwidth, 19.44 MHz input, direct lock
- Note 7. 10 Hz bandwidth, 19.44 MHz input, 8 kHz lock
- Note 8. 2.5 Hz bandwidth, 19.44 MHz input, direct lock
- Note 9. 2.5 Hz bandwidth, 19.44 MHz input, 8 kHz lock
- Note 10. 1.2 Hz bandwidth, 19.44 MHz input, direct lock
- Note 11. 1.2 Hz bandwidth, 19.44 MHz input, 8 kHz lock
- Note 12. 0.6 Hz bandwidth, 19.44 MHz input, direct lock
- Note 13. 0.6 Hz bandwidth, 19.44 MHz input, 8 kHz lock
- Note 14. 5 Hz bandwidth, 2.048 MHz input, 8 kHz lock

Figure 13. Input/Output Timing


Microprocessor Interface Timing

The device has a Serial microprocessor interface. The combined minimum High and Low times for SCLK define the maximum clock rate.

For Write access this is 2.77 MHz (360 ns). For Read access the maximum SCLK rate is slightly slower and is affected by the setting of CLKE, being either 2.0 MHz (500 ns) or 1 MHz (1 us).

This mismatch in rates is caused by the sampling technique used to detect the end of the address field in Read mode. It takes up to 3 cycles of an internal 6.40 MHz clock to start the Read process following receipt of the final address bit. This is 468 ns. The Read data is then decoded and clocked out onto SDO directly using SCLK. With CLKE=1, the falling edge of SCLK is used to clock out the SDO. With CLKE=0, the rising edge of SCLK is used to clock out the SDO.

A minimum period of 500 ns (468 capture plus 32 decode) is required between the final address bit and clocking it out onto SDO. This means that to guarantee the correct operation of the Serial interface, with CLKE=0, SCLK has a maximum clock rate of 2 MHz. With CLKE=1, SCLK has a maximum clock rate of 1 MHz.

SCLK is not required to run between accesses (i.e., when CSB = 1). The following Figures show the timing diagrams for Write and Read access for this mode.

Figure 14. Read Access Timing

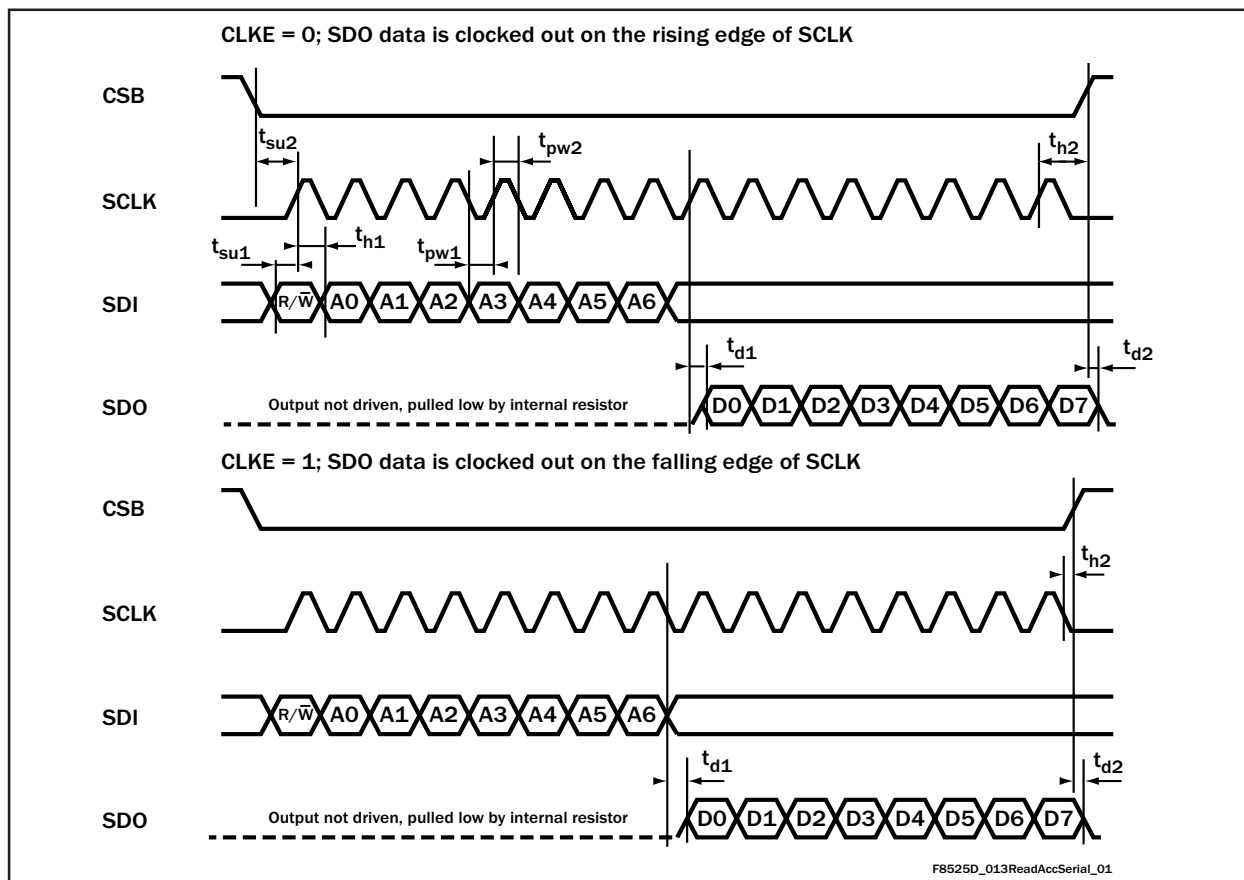
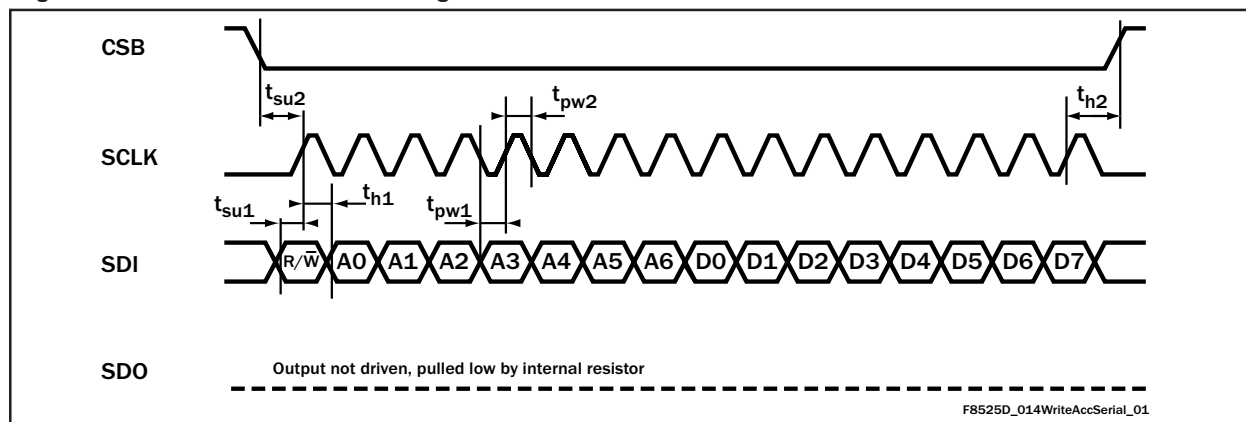


Table 28. Read Access Timing

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to SCLK _{rising edge}	0 ns	-	-
t_{su2}	Setup CSB _{falling edge} to SCLK _{rising edge}	160 ns	-	-
t_{d1}	Delay SCLK _{rising edge} (SCLK _{falling edge} for CLKE = 1) to SDO valid	-	-	17 ns
t_{d2}	Delay CSB _{rising edge} to SDO high-Z	-	-	10 ns
t_{pw1}	SCLK low time CLKE = 0 CLKE = 1	250 ns 500 ns	-	-
t_{pw2}	SCLK high time CLKE = 0 CLKE = 1	250 ns 500 ns	-	-
t_{h1}	Hold SDI valid after SCLK _{rising edge}	170 ns	-	-
t_{h2}	Hold CSB low after SCLK _{rising edge} for CLKE = 0 Hold CSB low after SCLK _{falling edge} for CLKE = 1	5 ns	-	-
t_p	Time between consecutive accesses (CSB _{rising edge} to CSB _{falling edge})	160 ns	-	-

Figure 15. Write Access Timing

Table 29. Write Access Timing

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to SCLK _{rising edge}	0 ns	-	-
t_{su2}	Setup CSB _{falling edge} to SCLK _{rising edge}	160 ns	-	-
t_{pw1}	SCLK low time	180 ns	-	-
t_{pw2}	SCLK high time	180 ns	-	-
t_{h1}	Hold SDI valid after SCLK _{rising edge}	170 ns	-	-
t_{h2}	Hold CSB low after SCLK _{rising edge}	5 ns	-	-
t_p	Time between consecutive accesses (CSB _{rising edge} to CSB _{falling edge})	160 ns	-	-

Package Information

Figure 16. LQFP Package

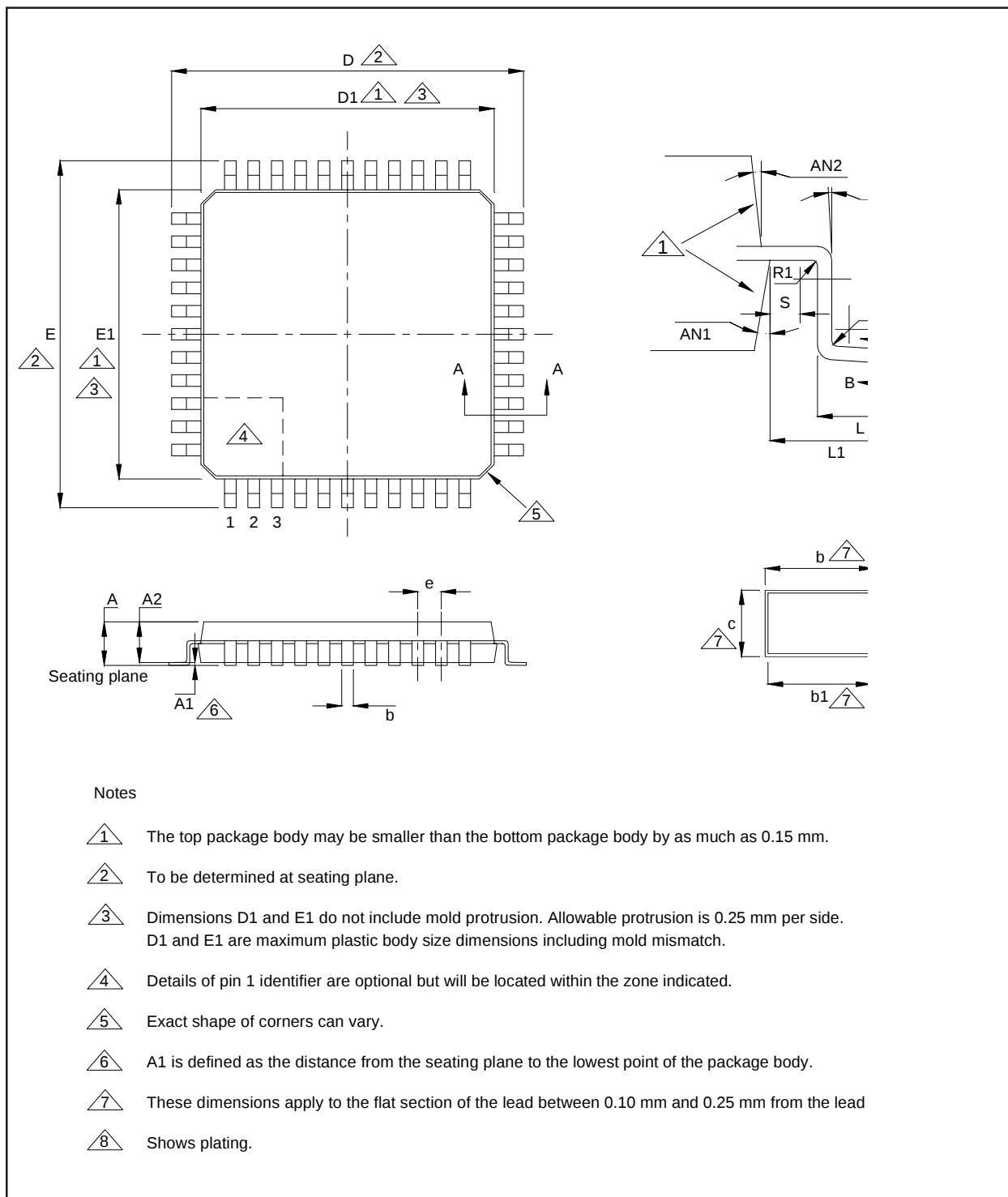
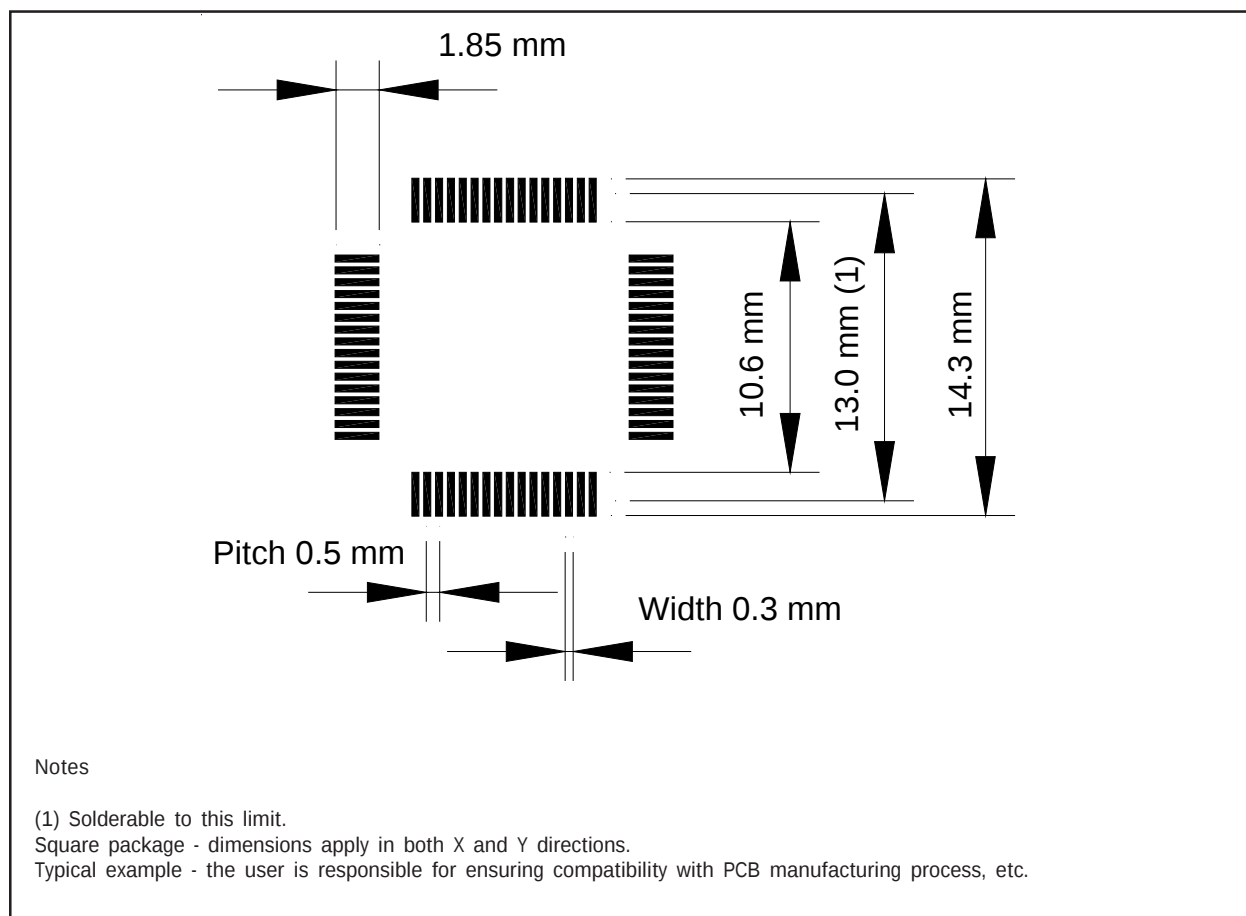


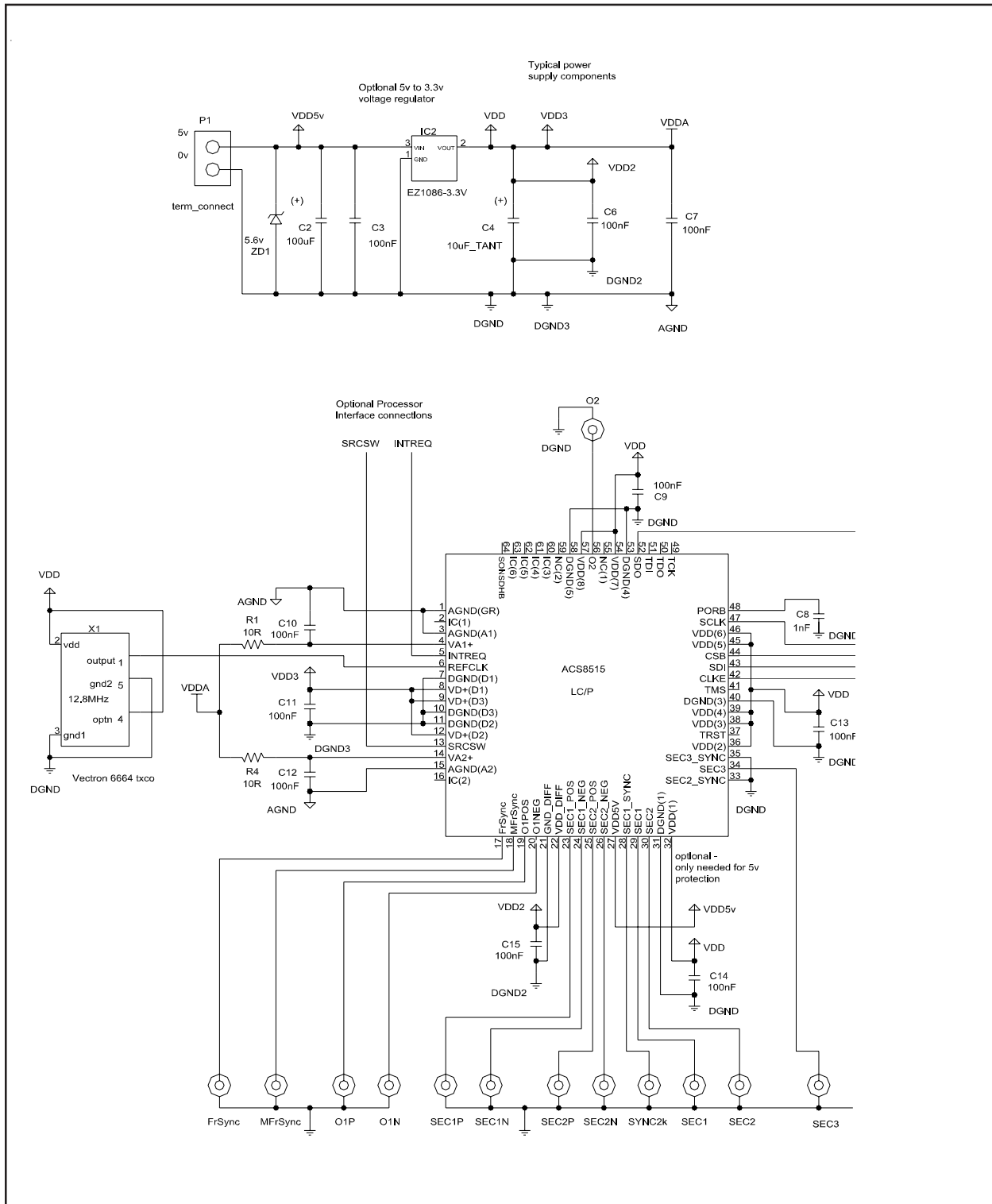
Table 30. 64 Pin LQFP Package Dimension Data (for use with Figure 16)

64 LQFP Package Dimensions in mm	D/E	D1/E1	A	A1	A2	e	AN1	AN2	AN3	AN4	R1	R2	L	L1	S	b	b1	c	c1
Min			1.40	0.05	1.35		11°	11°	0°	0°	0.08	0.08	0.45		0.20	0.17	0.17	0.09	0.09
Nom	12.00	10.00	1.50	0.10	1.40	0.50	12°	12°	-	3.5°	-	-	0.60	1.00 (ref)	-	0.22	0.20	-	-
Max			1.60	0.15	1.45		13°	13°	-	7°	-	0.20	0.75		-	0.27	0.23	0.20	0.16

Thermal Conditions

The device is rated for full temperature range when this package is used with a 4 layer or more PCB. Copper coverage must exceed 50%. All pins must be soldered to the PCB. Maximum operating temperature must be reduced when the device is used with a PCB with less than these requirements.

Figure 17. Typical 64 Pin LQFP Footprint


Application Information
Figure 18. Simplified Application Schematic


Appendix A Rev2.1 Changes Described**Summary**

This section summarizes the minor changes and improvements made to the ACS8515 from Rev2.0 to Rev2.1. The bulk of these changes are designed to remove the need for software work arounds associated with Phase Build Out.

Two new features have been added, necessitating changes to the control software. These are described in detail below.

Input Edge Alignment for 8k locking mode

An additional bit in the register *cnfg_control1* (Bit 2) has been allocated to select which edge of the input reference to lock to when the device is configured in 8k locking mode.

This bit, when set to one ensures that the rising edge of the output clock phase locks to the rising edge of the input clock, when 8k locking mode is used on the input.

Low Jitter n x E1/DS1 Mode

A second bit of the *cnfg_control1* register has been allocated to controlling what frequency is fed into the APLL. This allows the user to switch from the normal 77.76MHz to twice the dig2 output frequency.

This has the effect of replacing the normal OC/STM outputs with multiples of the E1 or DS1 rate. The E1/DS1 choice is controlled by the SONET/SDH bit in the *cnfg_mode* register.

Revision History

Table 31. Changes from Revision 1.05 to 2.00 September 2003.

Item	Section	Page	Description
1	Non-Revertive Mode	29	Updated Non-Revertive mode description

Ordering Information

PART NUMBER	DESCRIPTION
ACS8515 Rev2.1	SONET/SDH Line Card Protection, 64 pin LQFP
ACS8515 Rev2.1T	Lead (Pb) - free package version of ACS8515 rev 2.1

Disclaimers

Life support - This product is not designed or intended for use in life support equipment, devices or systems, or other critical applications. This product is not authorized or warranted by Semtech Corporation for such use.

Right to change - Semtech Corporation reserves the right to make changes, without notice, to this product. Customers are advised to obtain the latest version of the relevant information before placing orders.

Compliance to relevant standards - Operation of this device is subject to the user's implementation, and design practices. The user is responsible to ensure equipment using this device is compliant to any relevant standards.

For additional information, contact the following:

Semtech Corporation Advanced Communications Products

E-Mail: sales@semtech.com acsupport@semtech.com

Internet: <http://www.semtech.com>

USA: 200 Flynn Road, Camarillo, CA 93012-8790

Tel: +1 805 498 2111, Fax: +1 805 498 3804

FAR EAST: 11F, No. 46, Lane 11, Kuang Fu North Road, Taipei, Taiwan, R.O.C.

Tel: +886 2 2748 3380, Fax: +886 2 2748 3390

EUROPE: Units 2 & 3 Park Court, Premier Way, Abbey Park Industrial Estate,

Romsey, Hampshire, SO51 9DN, UK

Tel: +44 1794 527 600, Fax: +44 1794 527 601



ISO9001
CERTIFIED