Low Power, Wide Supply Range, Low Cost Difference Amplifiers, G = ½, 2

Preliminary Technical Data

AD8279

FEATURES

Wide input range beyond supplies
Rugged input overvoltage protection
Low supply current: 200 µA maximum
Low power dissipation: 0.5 mW at V_S = 2.5 V
Bandwidth: 1 MHz (G = ½)
CMRR: 80 dB minimum, dc to 20 kHz (G = ½)
Low offset voltage drift: ±2 µV/°C maximum (B Grade)
Low gain drift: 1 ppm/°C maximum (B Grade)
Enhanced slew rate: 1.4 V/µs
Wide power supply range:
Single supply: 2 V to 36 V
Dual supplies: ±2 V to ±18 V

APPLICATIONS

Voltage measurement and monitoring
Current measurement and monitoring
Instrumentation amplifier building block
Portable, battery-powered equipment
Test and measurement

GENERAL DESCRIPTION

The AD8279 consists of two general-purpose difference amplifiers intended for precision signal conditioning in power critical applications that require both high performance and low power. The AD8279 provides exceptional common-mode rejection ratio (80 dB) and high bandwidth while amplifying signals well beyond the supply rails. The on-chip resistors are laser-trimmed for excellent gain accuracy and high CMRR. They also have extremely low gain drift vs. temperature.

The common-mode range of the amplifiers extend to almost triple the supply voltage (for G = ½), making them ideal for single-supply applications that require a high common-mode voltage range. The internal resistors and ESD circuitry at the inputs also provide overvoltage protection to the op amp.

The AD8279 can be used as difference amplifiers with G = ½ or G = 2. It can also be connected in a high precision, single-ended configuration for non-inverting and inverting gains of −½, −2, +3, +2, +1½, +1, or +½. The AD8279 provide an integrated precision solution that has a smaller size, lower cost, and better performance than a discrete alternative.

FUNCTIONAL BLOCK DIAGRAM

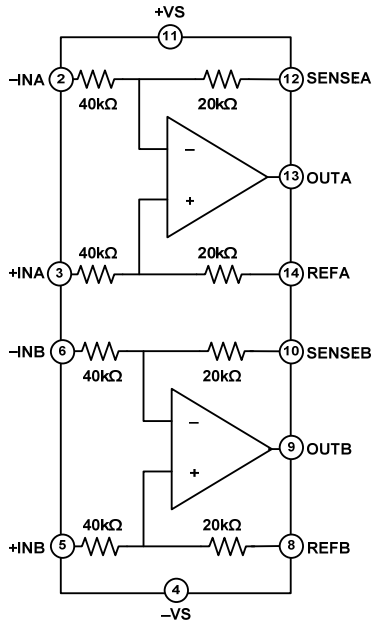

Figure 1.

The AD8279 operates on single supplies (2.0 V to 36 V) or dual supplies (±2 V to ±18 V). The maximum quiescent supply current is 200 µA per channel, which is ideal for battery-operated and portable systems.

The AD8279 is available in a 14-lead SOIC package. It is specified for performance over the industrial temperature range of −40°C to +85°C and are fully RoHS compliant.

Table 1. Difference Amplifiers by Category

Low Distortion	High Voltage	Current Sensing[1]	Low Power
AD8270	AD628	AD8202 (U)	AD8276
AD8271	AD629	AD8203 (U)	AD8277
AD8273		AD8205 (B)	AD8278
AD8274		AD8206 (B)	AD8279
AMP03		AD8216 (B)	

[1] U = unidirectional, B = bidirectional.

Rev. PrA

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REVISION HISTORY

SPECIFICATIONS

V_S = ±5 V to ±15 V, V_{REF} = 0 V, T_A = 25°C, R_L = 10 kΩ connected to ground, G = ½ difference amplifier configuration, unless otherwise noted.

Table 2.

		G = ½						
		Grade B			Grade A			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS								
System Offset[1]			50	100		50	250	µV
vs. Temperature	T_A = −40°C to +85°C			100			250	µV
Average Temperature Coefficient	T_A = −40°C to +85°C		0.3	1		2	5	µV/°C
vs. Power Supply	V_S = ±5 V to ±18 V			2.5			5	µV/V
Common-Mode Rejection Ratio (RTI)	V_S = ±15 V, V_{CM} = ±27 V, R_S = 0 Ω	80			74			dB
Input Voltage Range[2]		−3(V_S + 0.1)		+3(V_S − 1.5)	−3(V_S + 0.1)		+3(V_S − 1.5)	V
Impedance[3]								
Differential			120			120		kΩ
Common Mode			30			30		kΩ
DYNAMIC PERFORMANCE								
Bandwidth			1			1		MHz
Slew Rate		1.1	1.4		1.1	1.4		V/µs
Settling Time to 0.01%	10 V step on output, C_L = 100 pF			9			9	µs
Settling Time to 0.001%				10			10	µs
Channel Separation	f = 1 kHz		130			130		dB
GAIN								
Gain Error			0.005	0.02		0.01	0.05	%
Gain Drift	T_A = −40°C to +85°C			1			5	ppm/°C
Gain Nonlinearity	V_{OUT} = 20 V p-p			5			10	ppm
OUTPUT CHARACTERISTICS								
Output Voltage Swing[4]	V_S = ±15 V, R_L = 10 kΩ T_A = −40°C to +85°C	−V_S + 0.2		+V_S − 0.2	−V_S + 0.2		+V_S − 0.2	V
Short-Circuit Current Limit			±15			±15		mA
Capacitive Load Drive			200			200		pF
NOISE[5]								
Output Voltage Noise	f = 0.1 Hz to 10 Hz		1.4			1.4		µV p-p
	f = 1 kHz		47	50		47	50	nV/√Hz
POWER SUPPLY								
Supply Current[6]				200			200	µA
vs. Temperature	T_A = −40°C to +85°C			250			250	µA
Operating Voltage Range[7]		±2		±18	±2		±18	V
TEMPERATURE RANGE								
Operating Range		−40		+125	−40		+125	°C

[1] Includes input bias and offset current errors, RTO (referred to output)
[2] The input voltage range may also be limited by absolute maximum input voltage or by the output swing. See the Input Voltage Range section in the Theory of Operation for details.
[3] Internal resistors are trimmed to be ratio matched and have ±20% absolute accuracy.
[4] Output voltage swing varies with supply voltage and temperature. See Figure 19 through Figure 22 for details.
[5] Includes amplifier voltage and current noise, as well as noise from internal resistors.
[6] Supply current varies with supply voltage and temperature. See Figure 23 and Figure 25 for details.
[7] Unbalanced dual supplies can be used, such as −V_S = −0.5 V and +V_S = +2 V. The positive supply rail must be at least 2 V above the negative supply and reference voltage.

V_S = ±5 V to ±15 V, V_{REF} = 0 V, T_A = 25°C, R_L = 10 kΩ connected to ground, G = 2 difference amplifier configuration, unless otherwise noted.

Table 3.

		G = 2						
		Grade B			Grade A			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS								
System Offset[1]			100	200		100	500	µV
vs. Temperature	T_A = −40°C to +85°C			200			500	µV
Average Temperature Coefficient	T_A = −40°C to +85°C		0.6	2		2	5	µV/°C
vs. Power Supply	V_S = ±5 V to ±18 V			5			10	µV/V
Common-Mode Rejection Ratio (RTI)	V_S = ±15 V, V_{CM} = ±27 V, R_S = 0 Ω	86			80			dB
Input Voltage Range[2]		−1.5(V_S + 0.1)		+1.5(V_S − 1.5)	−1.5(V_S + 0.1)		+1.5(V_S − 1.5)	V
Impedance[3]								
Differential			120			120		kΩ
Common Mode			30			30		kΩ
DYNAMIC PERFORMANCE								
Bandwidth			550			550		kHz
Slew Rate		1.1	1.4		1.1	1.4		V/µs
Settling Time to 0.01%	10 V step on output, C_L = 100 pF			10			10	µs
Settling Time to 0.001%				11			11	µs
Channel Separation	f = 1 kHz		130			130		dB
GAIN								
Gain Error			0.005	0.02		0.01	0.05	%
Gain Drift	T_A = −40°C to +85°C			1			5	ppm/°C
Gain Nonlinearity	V_{OUT} = 20 V p-p			5			10	ppm
OUTPUT CHARACTERISTICS								
Output Voltage Swing[4]	V_S = ±15 V, R_L = 10 kΩ T_A = −40°C to +85°C	$-V_S$ + 0.2		$+V_S$ − 0.2	$-V_S$ + 0.2		$+V_S$ − 0.2	V
Short-Circuit Current Limit			±15			±15		mA
Capacitive Load Drive			350			350		pF
NOISE[5]								
Output Voltage Noise	f = 0.1 Hz to 10 Hz		2.8			2.8		µV p-p
	f = 1 kHz		90	95		90	95	nV/√Hz
POWER SUPPLY								
Supply Current[6]				200			200	µA
vs. Temperature	T_A = −40°C to +85°C			250			250	µA
Operating Voltage Range[7]		±2		±18	±2		±18	V
TEMPERATURE RANGE								
Operating Range		−40		+125	−40		+125	°C

[1] Includes input bias and offset current errors, RTO (referred to output).
[2] The input voltage range may also be limited by absolute maximum input voltage or by the output swing. See the Input Voltage Range section in the Theory of Operation for details.
[3] Internal resistors are trimmed to be ratio matched and have ±20% absolute accuracy.
[4] Output voltage swing varies with supply voltage and temperature. See Figure 19 through Figure 22 for details.
[5] Includes amplifier voltage and current noise, as well as noise from internal resistors.
[6] Supply current varies with supply voltage and temperature. See Figure 23 and Figure 25 for details.
[7] Unbalanced dual supplies can be used, such as $-V_S$ = −0.5 V and $+V_S$ = +2 V. The positive supply rail must be at least 2 V above the negative supply and reference voltage.

V_S = +2.7 V to <±5 V, V_{REF} = midsupply, T_A = 25°C, R_L = 10 kΩ connected to midsupply, G = ½ difference amplifier configuration, unless otherwise noted.

Table 4.

		G = ½						
		Grade B			Grade A			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS								
System Offset[1]			75	150		75	250	µV
vs. Temperature	T_A = −40°C to +85°C			150			250	µV
Average Temperature Coefficient	T_A = −40°C to +85°C		0.3	1		2	5	µV/°C
vs. Power Supply	V_S = ±5 V to ±18 V			2.5			5	µV/V
Common-Mode Rejection Ratio (RTI)	V_S = 2.7 V, V_{CM} = 0 V to 2.4 V, R_S = 0 Ω	80			74			dB
	V_S = ±5 V, V_{CM} = −10 V to +7 V, R_S = 0 Ω	80			74			dB
Input Voltage Range[2]		−3(V_S + 0.1)		+3(V_S − 1.5)	−3(V_S + 0.1)		+3(V_S − 1.5)	V
Impedance[3]								
Differential			120			120		kΩ
Common Mode			30			30		kΩ
DYNAMIC PERFORMANCE								
Bandwidth			870			870		kHz
Slew Rate			1.3			1.3		V/µs
Settling Time to 0.01%	2 V step on output, C_L = 100 pF, V_S = 2.7 V		7			7		µs
Channel Separation	f = 1 kHz		130			130		dB
GAIN								
Gain Error			0.005	0.02		0.01	0.05	%
Gain Drift	T_A = −40°C to +85°C			1			5	ppm/°C
OUTPUT CHARACTERISTICS								
Output Swing[4]	R_L = 10 kΩ , T_A = −40°C to +85°C	$-V_S$ + 0.1		$+V_S$ − 0.15	$-V_S$ + 0.1		$+V_S$ − 0.15	V
Short-Circuit Current Limit			±10			±10		mA
Capacitive Load Drive			200			200		pF
NOISE[5]								
Output Voltage Noise	f = 0.1 Hz to 10 Hz		1.4			1.4		µV p-p
	f = 1 kHz		47	50		47	50	nV/√Hz
POWER SUPPLY								
Supply Current[6]	T_A = −40°C to +85°C			200			200	µA
Operating Voltage Range		2.0		36	2.0		36	V
TEMPERATURE RANGE								
Operating Range		−40		+125	−40		+125	°C

[1] Includes input bias and offset current errors, RTO (referred to output).
[2] The input voltage range may also be limited by absolute maximum input voltage or by the output swing. See the Input Voltage Range section in the Theory of Operation section for details.
[3] Internal resistors are trimmed to be ratio matched and have ±20% absolute accuracy.
[4] Output voltage swing varies with supply voltage and temperature. See Figure 19 through Figure 22 for details.
[5] Includes amplifier voltage and current noise, as well as noise from internal resistors.
[6] Supply current varies with supply voltage and temperature. See Figure 24 and Figure 25 for details.

V_S = +2.7 V to <±5 V, V_{REF} = midsupply, T_A = 25°C, R_L = 10 kΩ connected to midsupply, G = 2 difference amplifier configuration, unless otherwise noted.

Table 5.

		G = 2						
		Grade B			Grade A			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS								
System Offset[1]			150	300		150	500	µV
vs. Temperature	T_A = −40°C to +85°C			300			500	µV
Average Temperature Coefficient	T_A = −40°C to +85°C		0.6	2		3	5	µV/°C
vs. Power Supply	V_S = ±5 V to ±18 V			5			10	µV/V
Common-Mode Rejection Ratio (RTI)	V_S = 2.7 V, V_{CM} = 0 V to 2.4 V, R_S = 0 Ω	86			80			dB
	V_S = ±5 V, V_{CM} = −10 V to +7 V, R_S = 0 Ω	86			80			dB
Input Voltage Range[2]		−1.5(V_S + 0.1)		+1.5(V_S − 1.5)	−1.5(V_S + 0.1)		+1.5(V_S − 1.5)	V
Impedance[3]								
Differential			120			120		kΩ
Common Mode			30			30		kΩ
DYNAMIC PERFORMANCE								
Bandwidth			450			450		kHz
Slew Rate			1.3			1.3		V/µs
Settling Time to 0.01%	2 V step on output, C_L = 100 pF, V_S = 2.7 V		9			9		µs
Channel Separation	f = 1 kHz		130			130		dB
GAIN								
Gain Error			0.005	0.02		0.01	0.05	%
Gain Drift	T_A = −40°C to +85°C			1			5	ppm/°C
OUTPUT CHARACTERISTICS								
Output Swing[4]	R_L = 10 kΩ, T_A = −40°C to +85°C	$-V_S$ + 0.1		$+V_S$ − 0.15	$-V_S$ + 0.1		$+V_S$ − 0.15	V
Short-Circuit Current Limit			±10			±10		mA
Capacitive Load Drive			200			200		pF
NOISE[5]								
Output Voltage Noise	f = 0.1 Hz to 10 Hz		2.8			2.8		µV p-p
	f = 1 kHz		94	100		94	100	nV/√Hz
POWER SUPPLY								
Supply Current[6]	T_A = −40°C to +85°C			200			220	µA
Operating Voltage Range		2.0		36	2.0		36	V
TEMPERATURE RANGE								
Operating Range		−40		+125	−40		+125	°C

[1] Includes input bias and offset current errors, RTO (referred to output).
[2] The input voltage range may also be limited by absolute maximum input voltage or by the output swing. See the Input Voltage Range section in the Theory of Operation section for details.
[3] Internal resistors are trimmed to be ratio matched and have ±20% absolute accuracy.
[4] Output voltage swing varies with supply voltage and temperature. See Figure 19 through Figure 22 for details.
[5] Includes amplifier voltage and current noise, as well as noise from internal resistors.
[6] Supply current varies with supply voltage and temperature. See Figure 24 and Figure 25 for details.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Supply Voltage	±18 V
Maximum Voltage at Any Input Pin	$-V_S + 40$ V
Minimum Voltage at Any Input Pin	$+V_S - 40$ V
Storage Temperature Range	−65°C to +150°C
Specified Temperature Range	−40°C to +85°C
Package Glass Transition Temperature (T_G)	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The θ_{JA} values in Table 7 assume a 4-layer JEDEC standard board with zero airflow.

Table 7. Thermal Resistance

Package Type	θ_{JA}	Unit
14-Lead SOIC	105	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8279 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 150°C for an extended period may result in a loss of functionality.

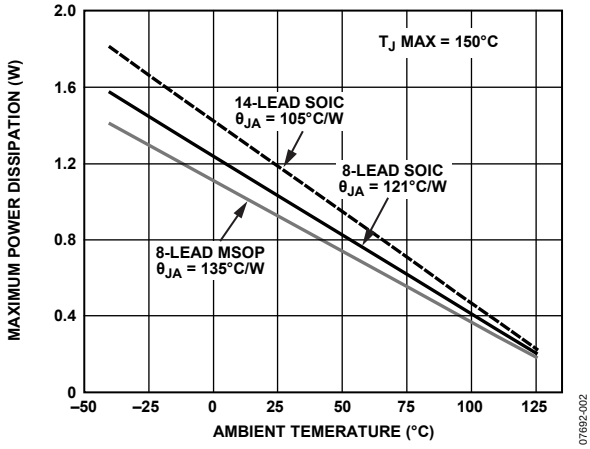


Figure 2. Maximum Power Dissipation vs. Ambient Temperature

SHORT-CIRCUIT CURRENT

The AD8279 has built-in, short-circuit protection that limits the output current (see Figure 26 for more information). While the short-circuit condition itself does not damage the part, the heat generated by the condition can cause the part to exceed its maximum junction temperature, with corresponding negative effects on reliability. Figure 2 and Figure 26, combined with knowledge of the supply voltages and ambient temperature of the part can be used to determine whether a short circuit will cause the part to exceed its maximum junction temperature.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

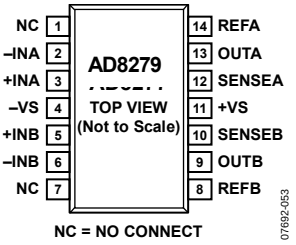


Figure 3. AD8279 14-Lead SOIC Pin Configuration

Table 8. AD8279 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect.
2	−INA	Channel A Inverting Input.
3	+INA	Channel A Noninverting Input.
4	−VS	Negative Supply.
5	+INB	Channel B Noninverting Input.
6	−INB	Channel B Inverting Input.
7	NC	No Connect.
8	REFB	Channel B Reference Voltage Input.
9	OUTB	Channel B Output.
10	SENSEB	Channel B Sense Terminal.
11	+VS	Positive Supply.
12	SENSEA	Channel A Sense Terminal.
13	OUTA	Channel A Output.
14	REFA	Channel A Reference Voltage Input.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±15 V, T_A = 25°C, R_L = 10 kΩ connected to ground, G = ½ difference amplifier configuration, unless otherwise noted.

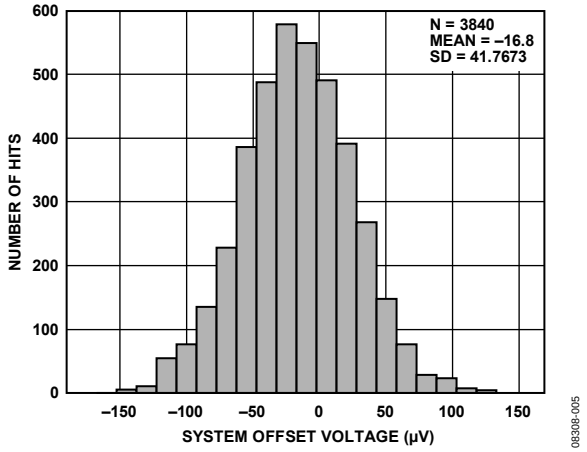


Figure 4. Distribution of Typical System Offset Voltage, G = 2

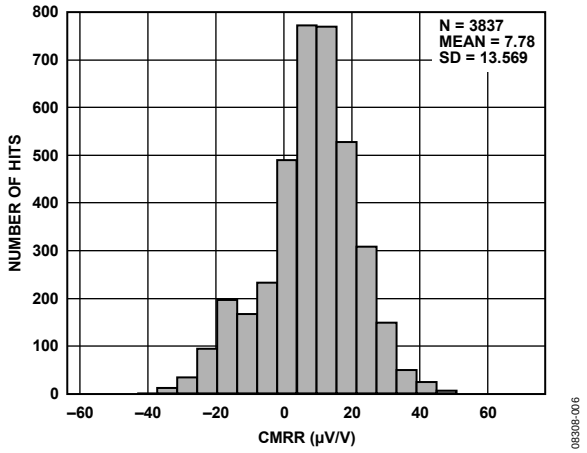


Figure 5. Distribution of Typical Common-Mode Rejection, G = 2

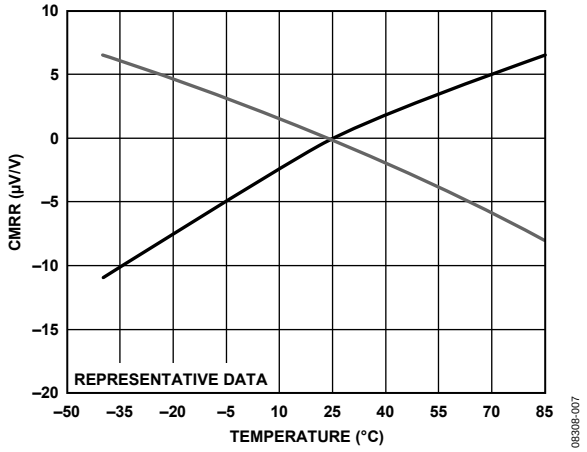


Figure 6. CMRR vs. Temperature, Normalized at 25°C, G = ½

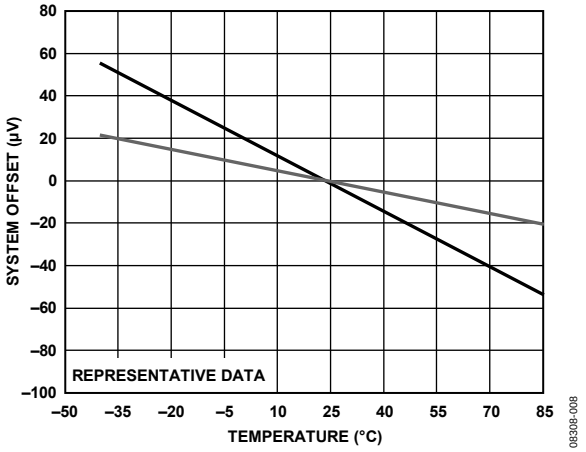


Figure 7. System Offset vs. Temperature, Normalized at 25°, G = ½

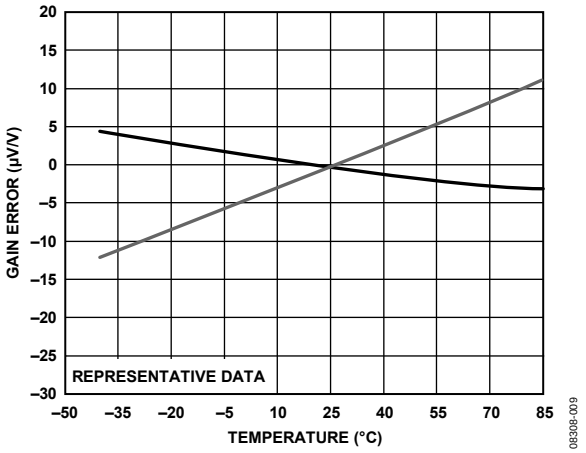


Figure 8. Gain Error vs. Temperature, Normalized at 25°C, G = ½

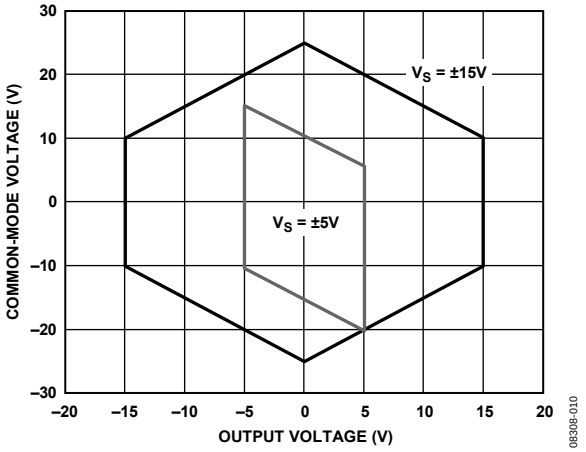


Figure 9. Input Common-Mode Voltage vs. Output Voltage, ±15 V and ±5 V Supplies, G = ½

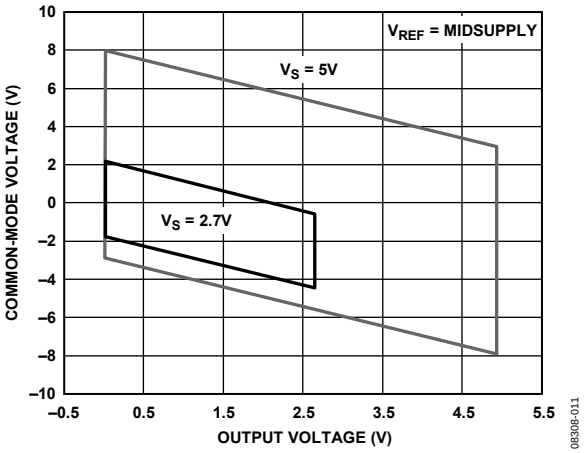


Figure 10. Input Common-Mode Voltage vs. Output Voltage, 5 V and 2.7 V Supplies, V_{REF} = Midsupply, G = ½

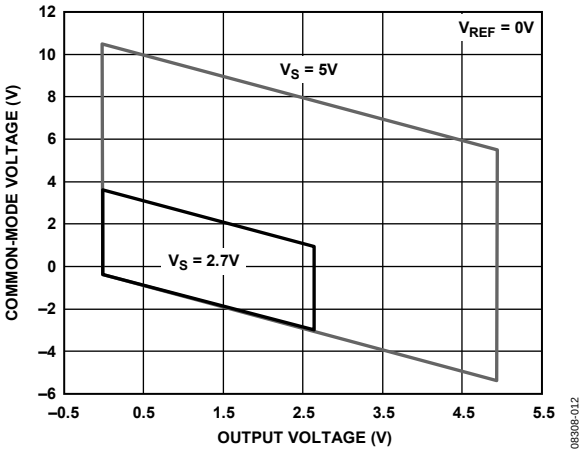


Figure 11. Input Common-Mode Voltage vs. Output Voltage, 5 V and 2.7 V Supplies, V_{REF} = 0 V, G = ½

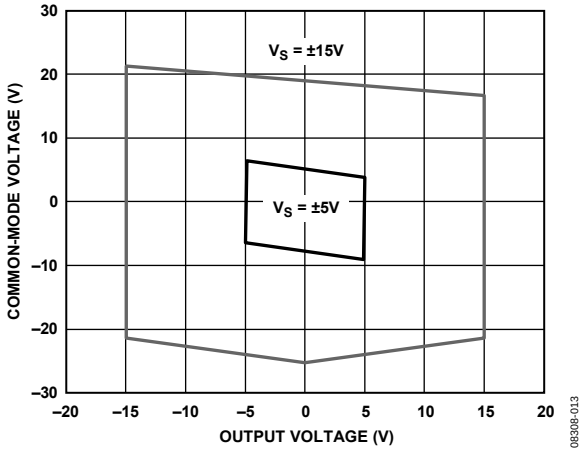


Figure 12. Input Common-Mode Voltage vs. Output Voltage, ±15 V and ±5 V Supplies, G = 2

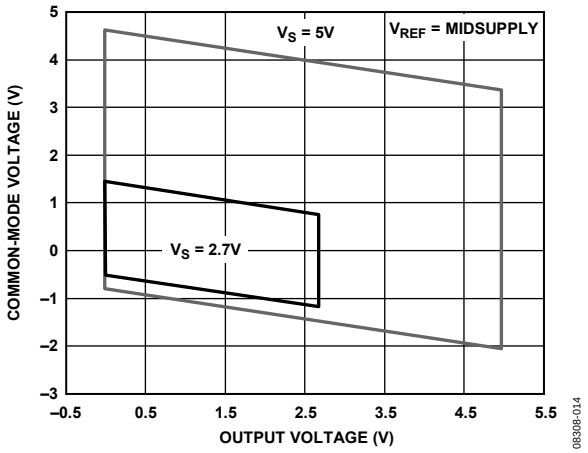


Figure 13. Input Common-Mode Voltage vs. Output Voltage, 5 V and 2.7 V Supplies, V_{REF} = Midsupply, G = 2

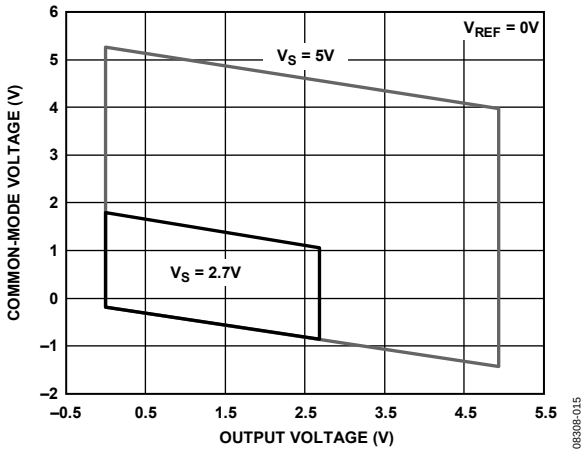


Figure 14. Input Common-Mode Voltage vs. Output Voltage, 5 V and 2.7 V Supplies, V_{REF} = 0 V, G = 2

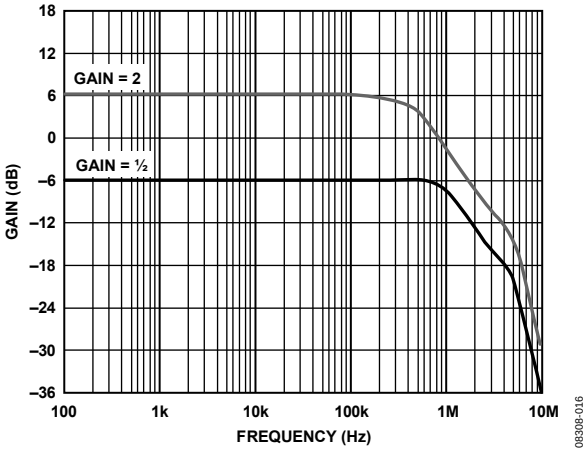


Figure 15. Gain vs. Frequency, ±15 V Supplies

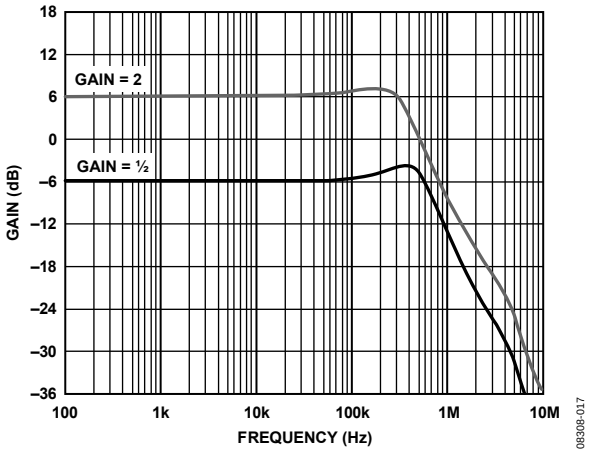


Figure 16. Gain vs. Frequency, +2.7 V Single Supply

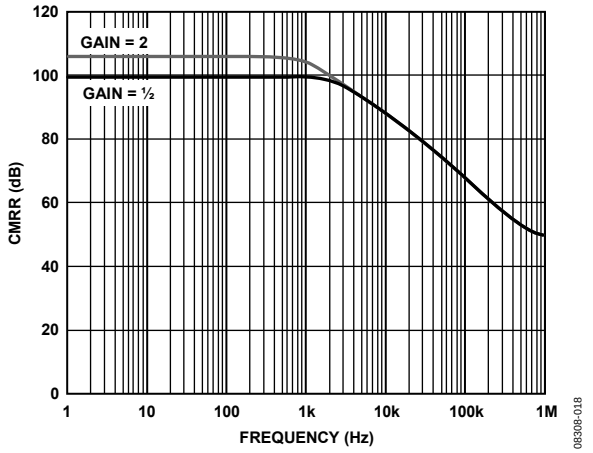


Figure 17. CMRR vs. Frequency

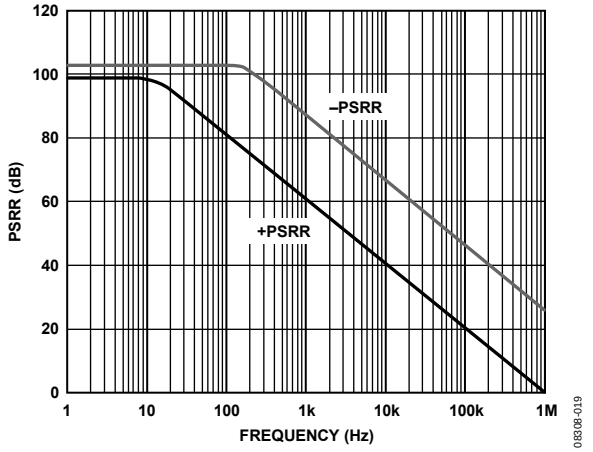


Figure 18. PSRR vs. Frequency

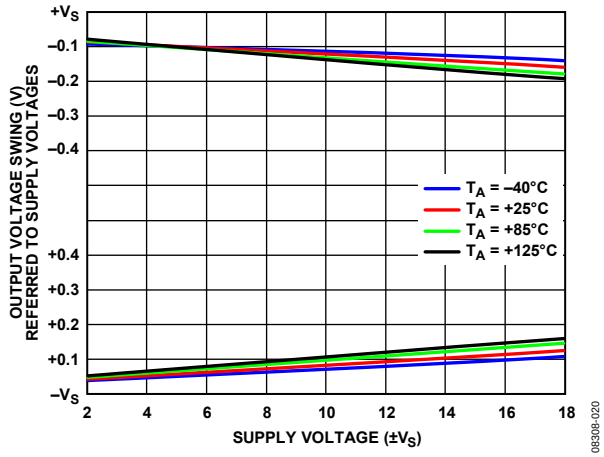


Figure 19. Output Voltage Swing vs. Supply Voltage and Temperature, R_L = 10 kΩ

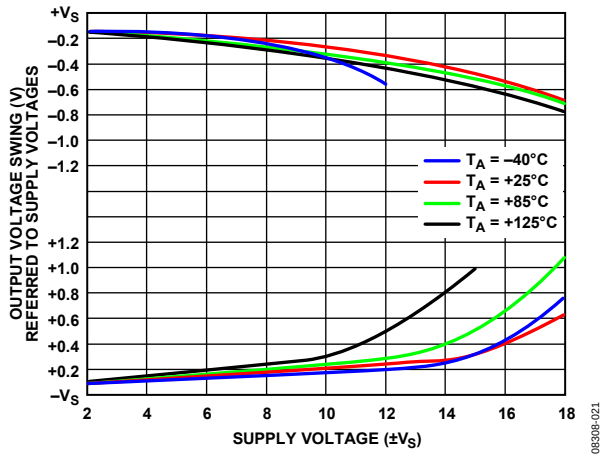


Figure 20. Output Voltage Swing vs. Supply Voltage and Temperature, R_L = 2 kΩ

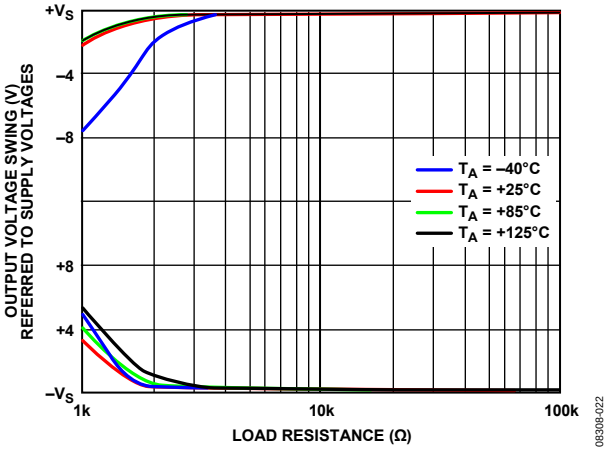


Figure 21. Output Voltage Swing vs. R_L and Temperature, V_S = ±15 V

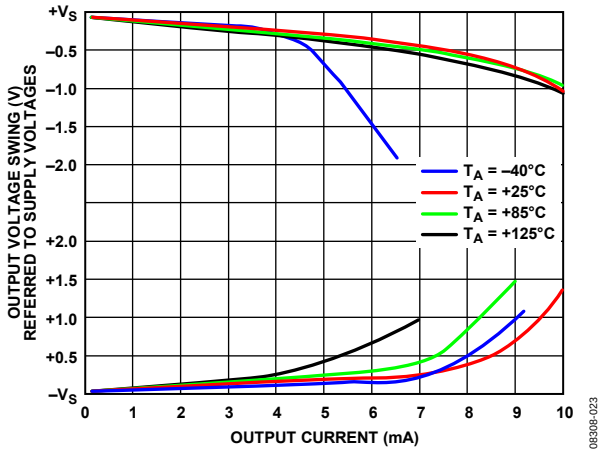


Figure 22. Output Voltage Swing vs. I_{OUT} and Temperature, V_S = ±15 V

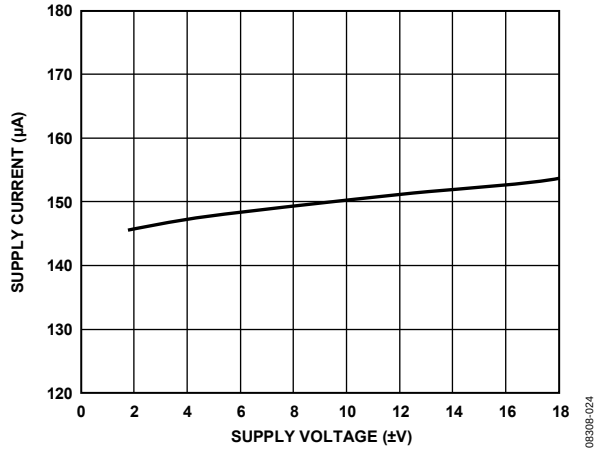


Figure 23. Supply Current per Channel vs. Dual-Supply Voltage, V_{IN} = 0 V

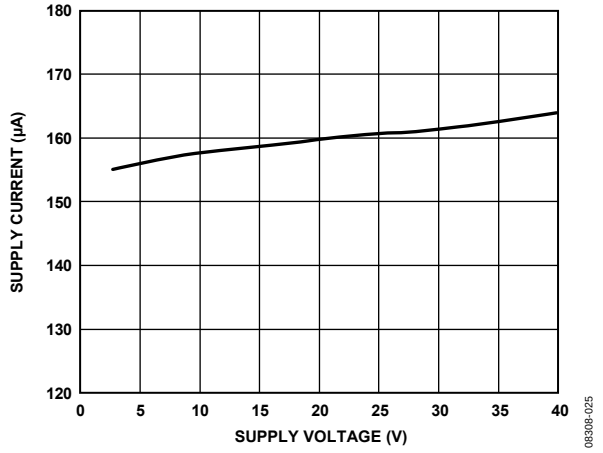


Figure 24. Supply Current per Channel vs. Single-Supply Voltage, V_{IN} = 0 V, V_{REF} = 0 V

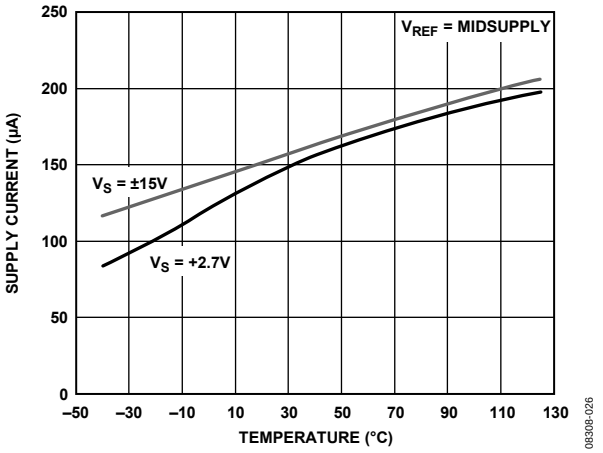


Figure 25. Supply Current per Channel vs. Temperature

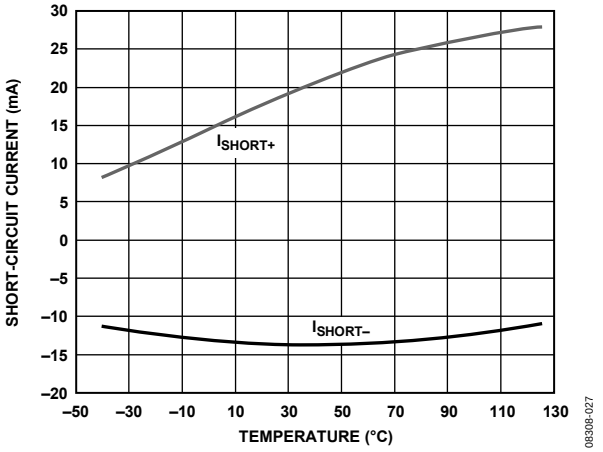


Figure 26. Short-Circuit Current per Channel vs. Temperature

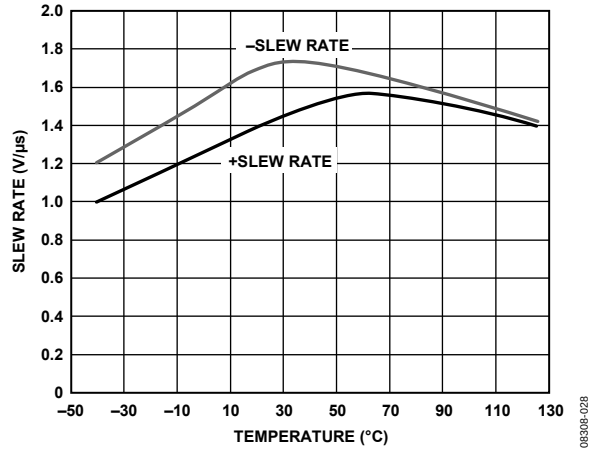


Figure 27. Slew Rate vs. Temperature, V_{IN} = 20 V p-p, 1 kHz

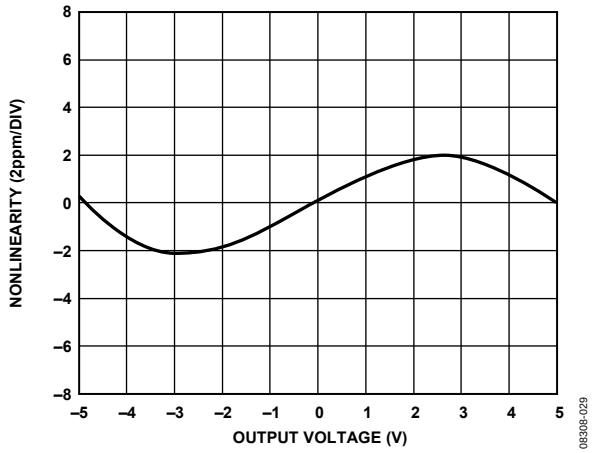


Figure 28. Gain Nonlinearity, $V_S = \pm 15$ V, $R_L \geq 2$ kΩ, G = ½

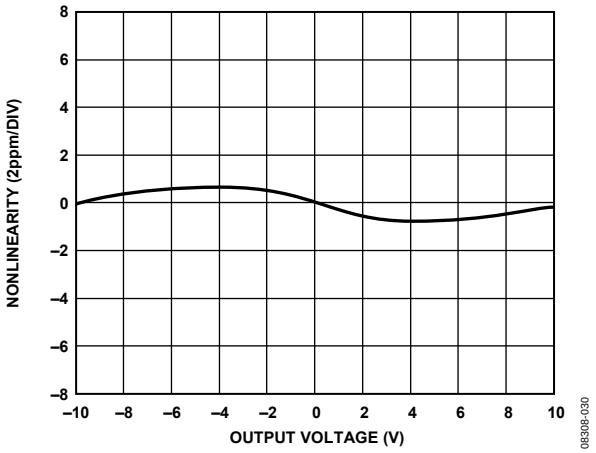


Figure 29. Gain Nonlinearity, $V_S = \pm 15$ V, $R_L \geq 2$ kΩ, G = 2

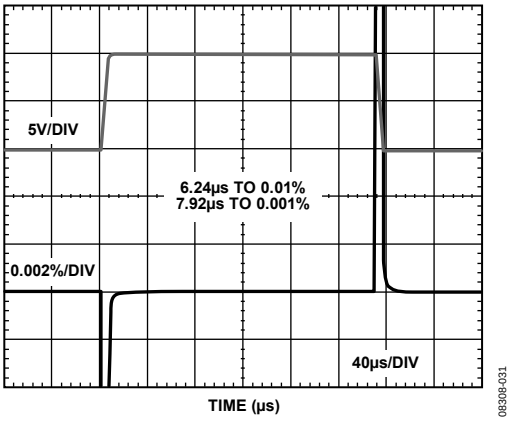


Figure 30. Large-Signal Pulse Response and Settling Time, 10 V Step, $V_S = \pm 15$ V, G = ½

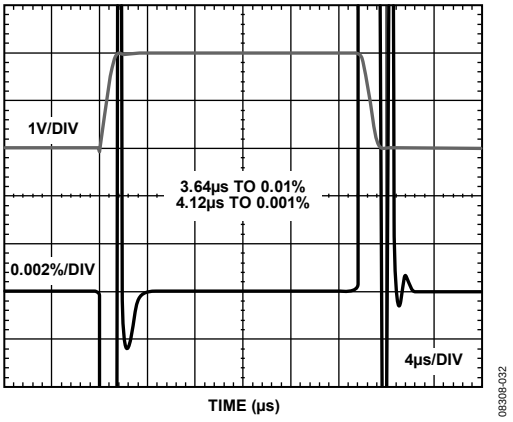


Figure 31. Large-Signal Pulse Response and Settling Time, 2 V Step, $V_S = 2.7$ V, G = ½

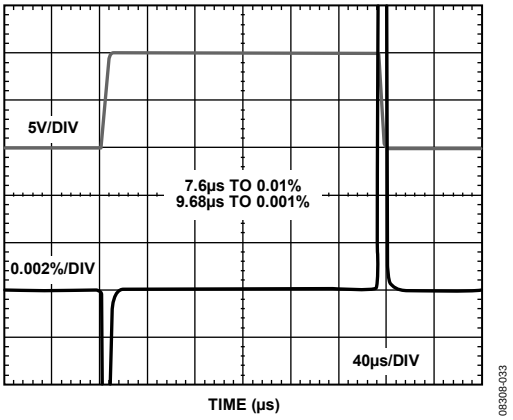


Figure 32. Large-Signal Pulse Response and Settling Time, 10 V Step, $V_S = \pm 15$ V, G = 2

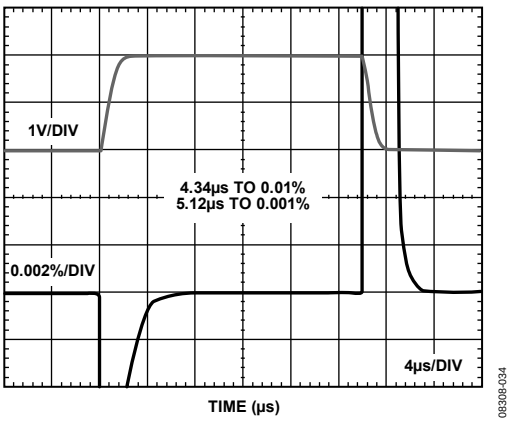


Figure 33. Large-Signal Pulse Response and Settling Time, 2 V Step, $V_S = 2.7$ V

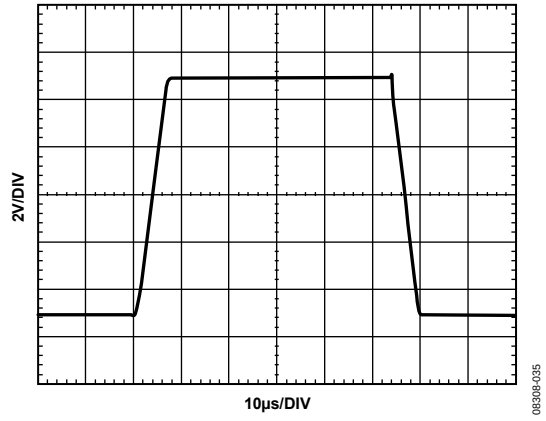


Figure 34. Large-Signal Step Response, G = ½

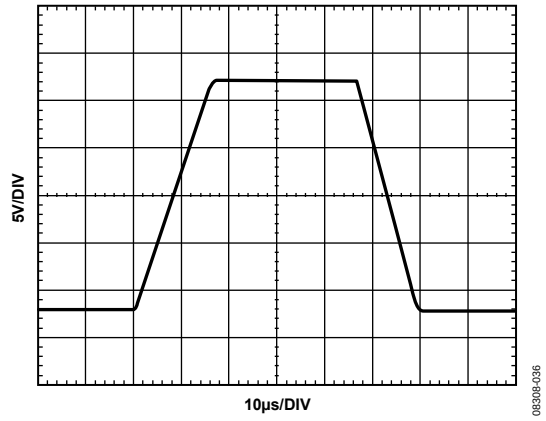


Figure 35. Large-Signal Step Response, G = 2

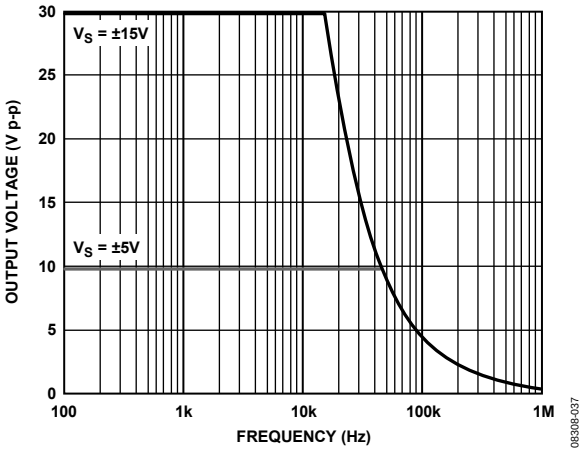


Figure 36. Maximum Output Voltage vs. Frequency, V_S = ±15 V, ±5 V

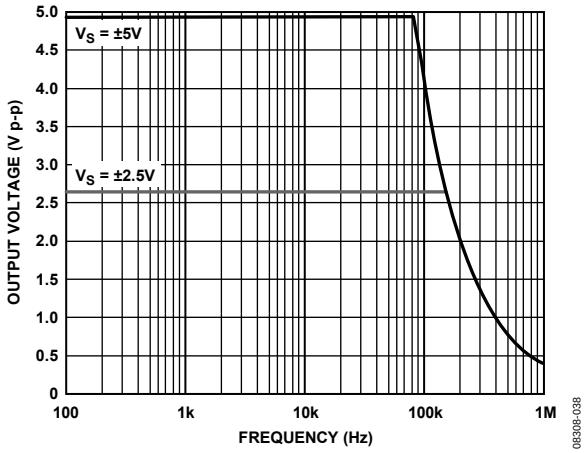


Figure 37. Maximum Output Voltage vs. Frequency, V_S = 5 V, 2.7 V

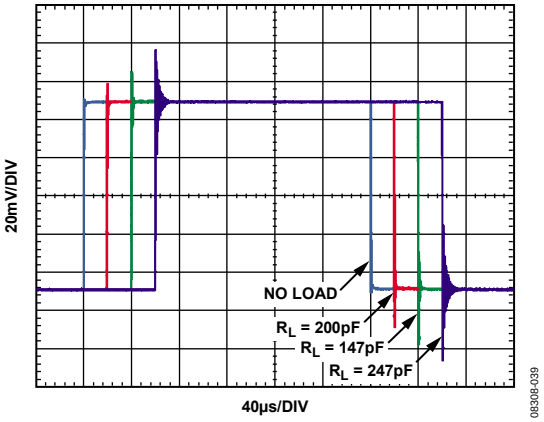


Figure 38. Small-Signal Step Response for Various Capacitive Loads, G = ½

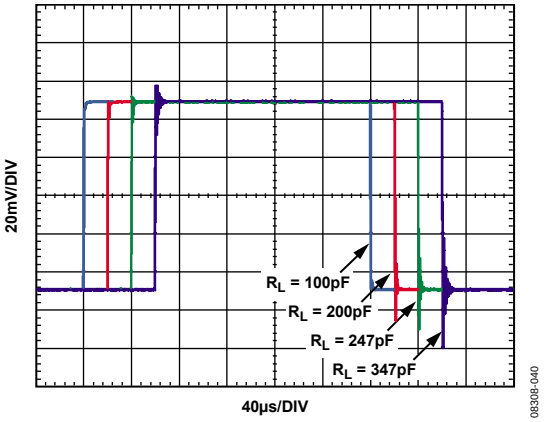


Figure 39. Small-Signal Step Response for Various Capacitive Loads, G = 2

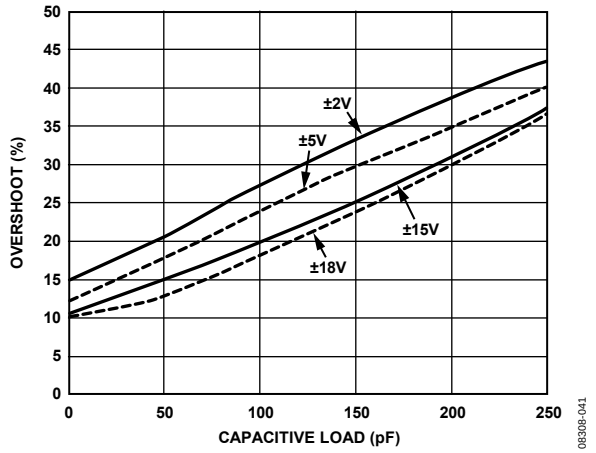


Figure 40. Small-Signal Overshoot vs. Capacitive Load, $R_L \geq 2$ kΩ, G = ½

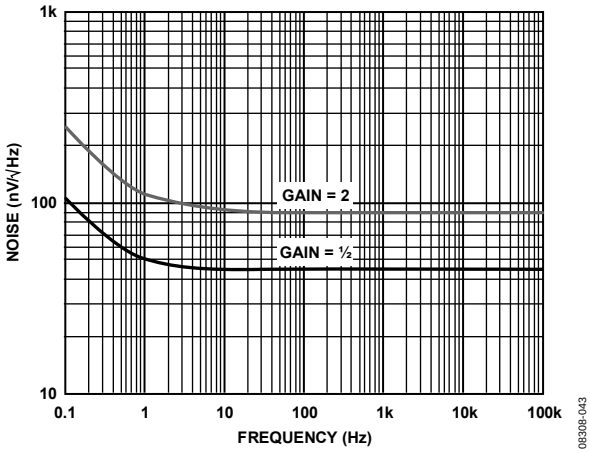


Figure 42. Voltage Noise Density vs. Frequency

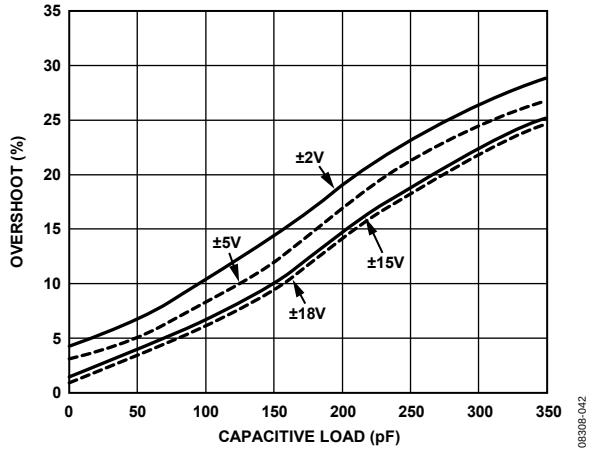


Figure 41. Small-Signal Overshoot vs. Capacitive Load, $R_L \geq 2$ kΩ, G = 2

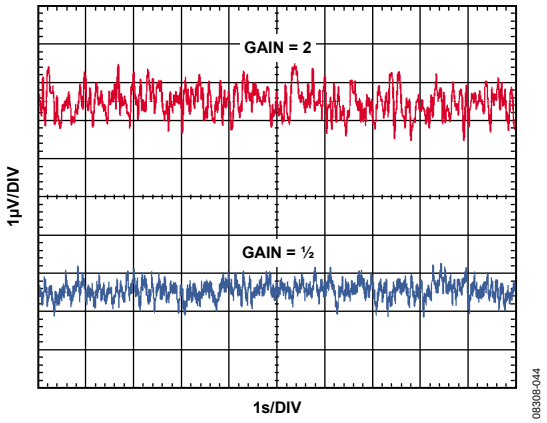


Figure 43. 0.1 Hz to 10 Hz Voltage Noise

THEORY OF OPERATION

CIRCUIT INFORMATION

Each channel of the AD8279 consists of a low power, low noise op amp and four laser-trimmed on-chip resistors. These resistors can be externally connected to make a variety of amplifier configurations, including difference, noninverting, and inverting configurations. Taking advantage of the integrated resistors of the AD8279 provides the designer with several benefits over a discrete design, including smaller size, lower cost, and better ac and dc performance.

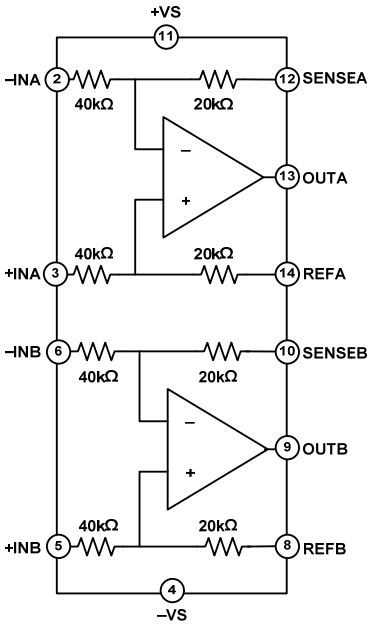


Figure 44. Functional Block Diagram

DC Performance

Much of the dc performance of op amp circuits depends on the accuracy of the surrounding resistors. Using superposition to analyze a typical difference amplifier circuit, as is shown in Figure 45, the output voltage is found to be

$$V_{OUT} = V_{IN+}\left(\frac{R2}{R1+R2}\right)\left(1+\frac{R4}{R3}\right) - V_{IN-}\left(\frac{R4}{R3}\right)$$

This equation demonstrates that the gain accuracy and common-mode rejection ratio of the AD8279 is determined primarily by the matching of resistor ratios. Even a 0.1% mismatch in one resistor degrades the CMRR to 69 dB for a G = 2 difference amplifier.

The difference amplifier output voltage equation can be reduced to

$$V_{OUT} = \frac{R4}{R3}\left(V_{IN+} - V_{IN-}\right)$$

as long as the following ratio of the resistors is tightly matched:

$$\frac{R2}{R1} = \frac{R4}{R3}$$

The resistors on the AD8279 are laser trimmed to match accurately. As a result, the AD8279 provides superior performance over a discrete solution, enabling better CMRR, gain accuracy, and gain drift, even over a wide temperature range.

AC Performance

Component sizes and trace lengths are much smaller in an IC than on a PCB, so the corresponding parasitic elements are also smaller. This results in better ac performance of the AD8279. For example, the positive and negative input terminals of the AD8279 op amps are intentionally not pinned out. By not connecting these nodes to the traces on the PCB, their capacitance remains low and balanced, resulting in improved loop stability and excellent common-mode rejection over frequency.

DRIVING THE AD8279

Care should be taken to drive the AD8279 with a low impedance source: for example, another amplifier. Source resistance of even a few kilohms (kΩ) can unbalance the resistor ratios and, therefore, significantly degrade the gain accuracy and common-mode rejection of the AD8279. Because all configurations present several kilohms (kΩ) of input resistance, the AD8279 does not require a high current drive from the source and so is easy to drive.

INPUT VOLTAGE RANGE

The AD8279 is able to measure input voltages beyond the supply rails. The internal resistors divide down the voltage before it reaches the internal op amp, and provide protection to the op amp inputs. Figure 45 shows an example of how the voltage division works in a difference amplifier configuration. For the AD8279 to measure correctly, the input voltages at the input nodes of the internal op amp must stay below 1.5 V of the positive supply rail and can exceed the negative supply rail by 0.1 V. Refer to the Power Supplies section for more details.

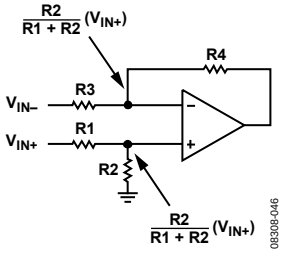


Figure 45. Voltage Division in the Difference Amplifier Configuration

The AD8279 has integrated ESD diodes at the inputs that provide overvoltage protection. This feature simplifies system design by eliminating the need for additional external protection circuitry, and enables a more robust system.

The voltages at any of the inputs of the parts can safely range from $+V_S - 40$ V up to $-V_S + 40$ V. For example, on ±10 V supplies, input voltages can go as high as ±30 V. Care should be taken to not exceed the $+V_S - 40$ V to $-V_S + 40$ V input limits to avoid risking damage to the parts.

POWER SUPPLIES

The AD8279 operates extremely well over a very wide range of supply voltages. They can operate on a single supply as low as 2 V and as high as 36 V, under appropriate setup conditions.

For best performance, the user must exercise care that the setup conditions ensure that the internal op amp is biased correctly. The internal input terminals of the op amp must have sufficient voltage headroom to operate properly. Proper operation of the part requires at least 1.5 V between the positive supply rail and the op amp input terminals. This relationship is expressed in the following equation:

$$\frac{R1}{R1+R2}V_{REF} < +V_S - 1.5\,\text{V}$$

For example, when operating on a $+V_S$= 2 V single supply and V_{REF} = 0 V, it can be seen from Figure 46 that the op amps input terminals are biased at 0 V, allowing more than the required 1.5 V headroom. However, if V_{REF} = 1 V under the same conditions, the input terminals of the op amp are biased at 0.66 V (G = ½). Now the op amp does not have the required 1.5 V headroom and can not function. Therefore, the user needs to increase the supply voltage or decrease V_{REF} to restore proper operation.

The AD8279 are typically specified at single- and dual-supplies, but it can be used with unbalanced supplies as well; for example, $-V_S$ = −5 V, $+V_S$ = 20 V. The difference between the two supplies must be kept below 36 V. The positive supply rail must be at least 2 V above the negative supply and reference voltage.

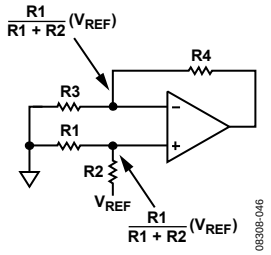
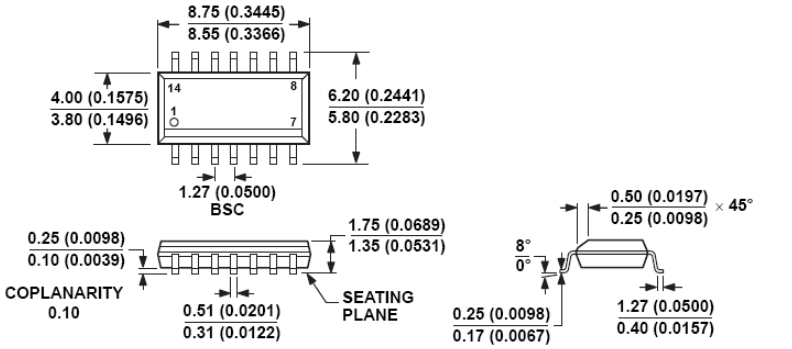


Figure 46. Ensure Sufficient Voltage Headroom on the Internal Op Amp Inputs

Use a stable dc voltage to power the AD8279. Noise on the supply pins can adversely affect performance. Place a bypass capacitor of 0.1 µF between each supply pin and ground, as close as possible to each supply pin. Use a tantalum capacitor of 10 µF between each supply and ground. It can be farther away from the supply pins and, typically, it can be shared by other precision integrated circuits.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AB

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 47. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-14)
Dimensions shown in millimeters and (inches)

PR08445-0-8/09(PrA)