Dual, 8-/10-/12-/14-Bit Low Power Digital-to-Analog Converters

AD9714/AD9715/AD9716/AD9717

FEATURES

Power dissipation @ 3.3 V, 2 mA output
- **37 mW @ 10 MSPS**
- **80 mW @ 125 MSPS**

Sleep mode: <3 mW @ 3.3 V
Supply voltage: 1.8 V to 3.3 V
SFDR to Nyquist
- **84 dBc @ 1 MHz output**
- **75 dBc @ 10 MHz output**

AD9717 NSD @ 1 MHz output, 125 MSPS, 2 mA: –151 dBc/Hz
Differential current outputs: 1 mA to 4 mA
Two on-chip auxiliary DACs
CMOS inputs with single-port operation
Output common mode: adjustable 0 V to 1.2 V
Small footprint 40-lead LFCSP Pb-free package

APPLICATIONS

Wireless infrastructures
- **Picocell, femtocell base stations**

Medical instrumentation
- **Ultrasound transducer excitation**

Portable instrumentation
- **Signal generators, arbitrary waveform generators**

GENERAL DESCRIPTION

The AD9714/AD9715/AD9716/AD9717 are pin-compatible dual, 8-/10-/12-/14-bit, low power digital-to-analog converters (DACs) that provide a sample rate of 125 MSPS. These TxDAC® converters are optimized for the transmit signal path of communication systems. All the devices share the same interface, LFCSP package, and pinout, providing an upward or downward component selection path based on performance, resolution, and cost.

The AD9714/AD9715/AD9716/AD9717 offer exceptional ac and dc performance and support update rates up to 125 MSPS.

The flexible power supply operating range of 1.8 V to 3.3 V and low power dissipation of the AD9714/AD9715/AD9716/AD9717 make them well-suited for portable and low power applications.

PRODUCT HIGHLIGHTS

1. Low Power.
   DACs operate on a single 1.8 V to 3.3 V supply; total power consumption reduces to 35 mW at 125 MSPS with a 1.8 V supply. Sleep and power-down modes are provided for low power idle periods.
2. CMOS Clock Input.
   High speed, single-ended CMOS clock input supports 125 MSPS conversion rate.
3. Easy Interfacing to Other Components.
   Adjustable output common mode from 0 V to 1.2 V allows for easy interfacing to other components that accept common-mode levels greater than 0 V.

Rev. 0

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REVISION HISTORY

8/08—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

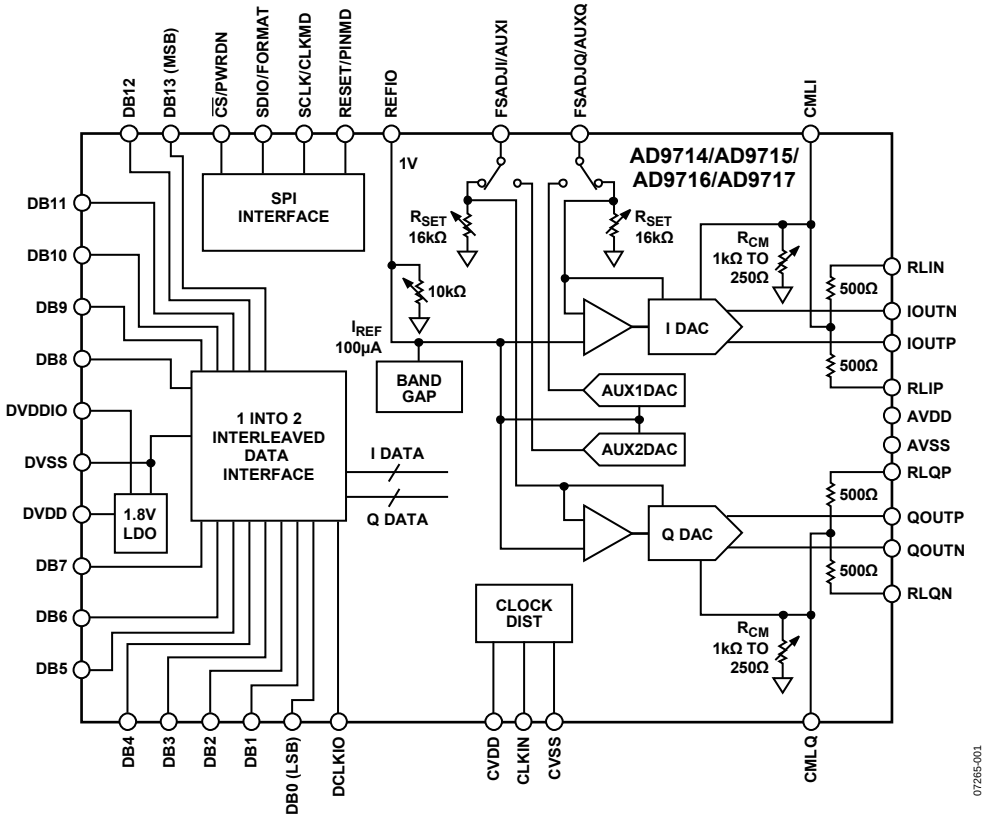

Figure 1.

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{OUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 1.

	AD9714			AD9715			AD9716			AD9717			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		8			10			12			14		Bits
ACCURACY @ 3.3 V													
Differential Nonlinearity (DNL)													
Precalibration		±0.02			±0.08			±0.4			±1.7		LSB
Postcalibration		±0.003			±0.01			±0.2			±1.0		LSB
Integral Nonlinearity (INL)													
Precalibration		±0.025			±0.13			±0.4			±1.8		LSB
Postcalibration		±0.01			±0.05			±0.3			±1.3		LSB
ACCURACY @ 1.8 V													
Differential Nonlinearity (DNL)													
Precalibration		±0.02			±0.08			±0.4			±1.2		LSB
Postcalibration		±0.005			±0.01			±0.2			±1.0		LSB
Integral Nonlinearity (INL)													
Precalibration		±0.025			±0.12			±0.4			±1.5		LSB
Postcalibration		±0.02			±0.05			±0.25			±1.1		LSB
MAIN DAC OUTPUTS													
Offset Error	−1	0	+1	−1	0	+1	−1	0	+1	−1	0	+1	mV
Gain Error													
Internal Reference	−2		+2	−2		+2	−2		+2	−2		+2	% of FSR
Full-Scale Output Current[1]													
V_{CC} = 3.3 V	1	2	4	1	2	4	1	2	4	1	2	4	mA
V_{CC} = 1.8 V	1	2	2.5	1	2	2.5	1	2	2.5	1	2	2.5	mA
Output Compliance Range	−0.5	0	+1.2	−0.5	0	+1.2	−0.5	0	+1.2	−0.5	0	+1.2	V
Output Resistance		200			200			200			200		MΩ
Crosstalk, Q DAC to I DAC													
f_{OUT} = 30 MHz		97			97			97			97		dB
f_{OUT} = 60 MHz		78			78			78			78		dB
MAIN DAC TEMPERATURE DRIFT													
Offset		0			0			0			0		ppm/°C
Gain		±40			±40			±40			±40		ppm/°C
Reference Voltage		±25			±25			±25			±25		ppm/°C
AUXDAC OUTPUTS													
Resolution		10			10			10			10		Bits
Full-Scale Output Current (Current Sourcing Mode)		125			125			125			125		µA
Voltage Output Mode	V_{SS}		V_{DD}	V_{SS}		V_{DD}	V_{SS}		V_{DD}	V_{SS}		V_{DD}	V
Output Compliance Range (Sourcing 1 mA)	V_{SS}		V_{DD} − 0.25	V_{SS}		V_{DD} − 0.25	V_{SS}		V_{DD} − 0.25	V_{SS}		V_{DD} − 0.25	V
Output Compliance Range (Sinking 1 mA)	V_{SS} + 0.25		V_{DD}	V_{SS} + 0.25		V_{DD}	V_{SS} + 0.25		V_{DD}	V_{SS} + 0.25		V_{DD}	V
Output Resistance in Current Output Mode V_{SS} to +1 V		1			1			1			1		MΩ
AUX DAC Monotonicity Guaranteed		10			10			10			10		Bits
REFERENCE OUTPUT													
Internal Reference Voltage	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	V
Output Resistance		10			10			10			10		kΩ
REFERENCE INPUT													
Voltage Compliance	0.1		1.25	0.1		1.25	0.1		1.25	0.1		1.25	V
Input Resistance		1			1			1			1		MΩ

Parameter	AD9714			AD9715			AD9716			AD9717			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DAC MATCHING													
Gain Matching	−1		+1	−1		+1	−1		+1	−1		+1	% FSR
ANALOG SUPPLY VOLTAGES													
AVDD	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
CVDD	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
DIGITAL SUPPLY VOLTAGES													
DVDD	1.7		1.9	1.7		1.9	1.7		1.9	1.7		1.9	V
DVDDIO	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
POWER CONSUMPTION @ 3.3 V													
f_{DAC} = 125 MSPS, IF = 12.5 MHz		86			86			86			86		mW
I_{AVDD}		10			10			10			10		mA
I_{DVDD} [2]		0			0			0			0		mA
I_{DVDDIO} [3]		11			11			11			11		mA
I_{CVDD}		3			3			3			3		mA
Power-Down Mode with Clock		50			50			50			50		mW
Power-Down Mode No Clock		1.5			1.5			1.5			1.5		mW
Power Supply Rejection Ratio		−0.04			−0.04			−0.04			−0.04		% FSR/V
POWER CONSUMPTION @ 1.8 V													
f_{DAC} = 125 MSPS, IF = 12.5 MHz		35			35			35			35		mW
I_{AVDD}		10			10			10			10		mA
$I_{DVDD} + I_{DVDDIO}$		8			8			8			8		mA
I_{CVDD}		1.5			1.5			1.5			1.5		mA
Power-Down Mode with Clock		12			12			12			12		mW
Power-Down Mode No Clock		850			850			850			850		µW
Power Supply Rejection Ratio		−0.001			−0.001			−0.001			−0.001		% FSR/V
OPERATING RANGE	−40	+25	+85	−40	+25	+85	−40	+25	+85	−40	+25	+85	°C

[1] Based on a 10 kΩ external resistor.
[2] Bypass only.
[3] LDO on.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{OUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKIN)				
V_{IH}	2.1	3		V
V_{IL}		0	0.9	V
Maximum Clock Rate			125	MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)		25		MHz
Minimum Pulse Width High		20		ns
Minimum Pulse Width Low		20		ns
INPUT DATA				
1.8 V Q-Channel or DCLKIO Falling Edge				
Setup		0.25		ns
Hold		1.2		ns
I-Channel or DCLKIO Rising Edge				
Setup		0.13		ns
Hold		1.1		ns
3.3 V Q-Channel or DCLKIO Falling Edge				
Setup		−0.2		ns
Hold		1.5		ns
I-Channel or DCLKIO Rising Edge				
Setup		−0.2		ns
Hold		1.6		ns
V_{IH}	2.1	3		V
V_{IL}		0	0.9	V

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, DVDDIO = 1.8 V, CVDD = 3.3 V, I_{OUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 3.

	AD9714			AD9715			AD9716			AD9717			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS FREE DYNAMIC RANGE (SFDR)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		75			82			83			84		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		60			61			62			63		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		86			87			88			89		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		71			71			71			71		dBc
NOISE SPECTRAL DENSITY (NSD) EIGHT-TONE, 500 kHz TONE SPACING													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		−129			−141			−149			−152		dBc/Hz
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		−123			−135			−137			−141		dBc/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER													
f_{DAC} = 61.44 MSPS, f_{OUT} = 20 MHz		−71			−71			−71			−71		dBc
f_{DAC} = 122.88 MSPS, f_{OUT} = 30 MHz		−72			−72			−72			−72		dBc

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = 3.3 V, DVDDIO = 1.8 V, CVDD = 3.3 V, I_{OUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 4.

	AD9714			AD9715			AD9716			AD9717			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS FREE DYNAMIC RANGE (SFDR)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		75			78			79			80		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		55			56			57			58		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		79			80			84			85		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		53			53			53			53		dBc
NOISE SPECTRAL DENSITY (NSD) EIGHT-TONE, 500 kHz TONE SPACING													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		−132			−141			−146			−148		dBc/Hz
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		−126			−131			−131			−132		dBc/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER													
f_{DAC} = 61.44 MSPS, f_{OUT} = 20 MHz		−68			−68			−68			−68		dBc
f_{DAC} = 122.88 MSPS, f_{OUT} = 30 MHz		−68			−68			−68			−68		dBc

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD, DVDDIO, CVDD to AVSS, DVSS, CVSS	−0.3 V to +3.9 V
DVDD to DVSS	−0.3 V to +2.1 V
AVSS to DVSS, CVSS	−0.3 V to +0.3 V
DVSS to AVSS, CVSS	−0.3 V to +0.3 V
CVSS to AVSS, DVSS	−0.3 V to +0.3 V
VREF, FSADJQ, FSADJI, CMLQ, CMLI to AVSS	−0.3 V to AVDD + 0.3 V
QOUTP, QOUTN, IOUTP, IOUTN, RLQP, RLQN, RLIP, RLIN to AVSS	−1.0 V to AVDD + 0.3 V
D13 to D0, $\overline{CS}$, SCLK, SDIO, SDO, RESET to DVSS	−0.3 V to DVDD + 0.3 V
CLKIN to CVSS	−0.3 V to CVDD + 0.3 V
$\overline{CS}$, SCLK, SDIO, SDO to DVSS	−0.3 V to DVDD + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6.

Package Type	θ_{JA}	Unit
40-Lead LFCSP (With No Airflow Movement)	29.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

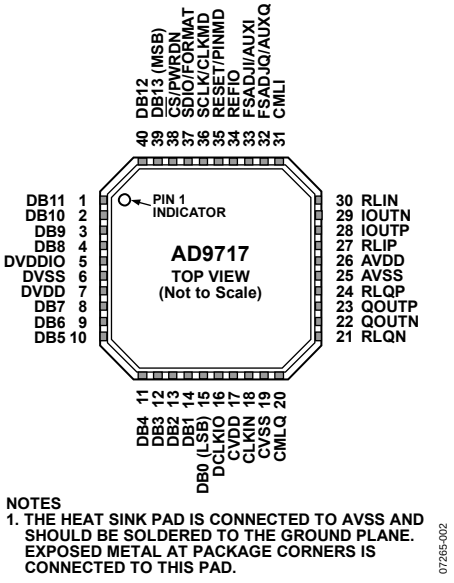

Figure 2. AD9717 Pin Configuration

Table 7. AD9717 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[11:8]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). Provides a 1.8 V output when the internal LDO regulator is enabled.
8 to 14	DB[7:1]	Digital Inputs.
15	DB0 (LSB)	Digital Input (LSB).
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin.
28	IOUTP	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
29	IOUTN	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin.
31	CMLI	I DAC Output Common-Mode Level.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust for Q DAC. Connect to AVSS through a resistor. Auxiliary Q DAC. The pin becomes the output of an optional, serial port driven, auxiliary DAC when the internal on-chip, R_{SET}, is enabled.
33	FSADJI/AUXI	Full-Scale Current Output Adjust for I DAC. Connect to AVSS through a resistor. Auxiliary I DAC. The pin becomes the output of an optional, serial port driven, auxiliary DAC when the internal on-chip, R_{SET}, is enabled.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).

Pin No.	Mnemonic	Description
35	RESET/PINMD	Reset. In SPI mode, pulse RESET high to reset SPI registers to default values. Pin Mode. A constant Logic 1 puts the device into pin mode.
36	SCLK/CLKMD	Serial Clock. Clock input for serial port in spi mode Clock Mode. In pin mode, CLKMD determines phase of internal retiming clock. DCLKIO = CLKIN: Tie to 0. DCLKIO ≠ CLKIN: Pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output. Bidirectional data line for serial port in spi mode. Data Format. In pin mode, FORMAT determines data format of digital data.
38	$\overline{CS}$/PWRDN	Chip Select. Active low chip select in spi mode. Power Down. In pin mode, PWRDN powers down the device except for the SPI port.
39	DB13 (MSB)	Digital Input (MSB).
40	DB12	Digital Input.
	Heat Sink Pad	The heat sink pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at package corners is connected to this pad.

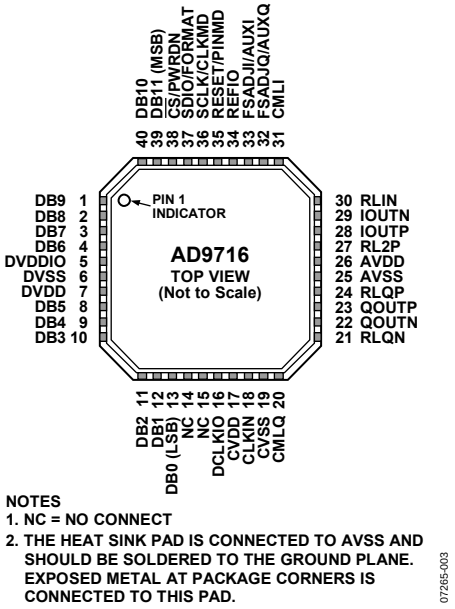

Figure 3. AD9716 Pin Configuration

Table 8. AD9716 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[9:6]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). Provides a 1.8 V output when in internal LDO regulator is enabled.
8 to 12	DB[5:1]	Digital Inputs.
13	DB0 (LSB)	Digital Input (LSB).
14,15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input Clock. Used to clock data in from digital source.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RL2P	Load Resistor (500 Ω) to the CMLI Pin.
28	IOUTP	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
29	IOUTN	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin.
31	CMLI	I DAC Output Common-Mode Level.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust for Q DAC. Connect to AVSS through a resistor. Auxiliary Q DAC. The pin becomes the output of an optional, serial port driven, auxiliary DAC when the internal on-chip, R_{SET}, is enabled.
33	FSADJI/AUXI	Full-Scale Current Output Adjust for I DAC. Connect to AVSS through a resistor. Auxiliary I DAC. The pin becomes the output of an optional, serial port driven, auxiliary DAC when the internal on-chip, R_{SET}, is enabled.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).

Pin No.	Mnemonic	Description
35	RESET/PINMD	Reset in SPI Mode. Pulse high to reset SPI registers to default values. Pin Mode. A constant Logic 1 puts the device into pin mode.
36	SCLK/CLKMD	Serial Clock. Clock input for serial port in spi mode. Clock Mode. In pin mode, CLKMD determines phase of internal retiming clock. DCLKIO = CLKIN: Tie to 0. DCLKIO ≠ CLKIN: Pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output. Bidirectional data line for serial port in spi mode. Data Format. In pin mode, FORMAT determines data format of digital data.
38	$\overline{CS}$/PWRDN	Chip Select. Active low chip select in spi mode. Power Down. In pin mode, PWRDN powers down the device except for the SPI port.
39	DB11 (MSB)	Digital Input (MSB).
40	DB10	Digital Input.
	Heat Sink Pad	The heat sink pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at package corners is connected to this pad.

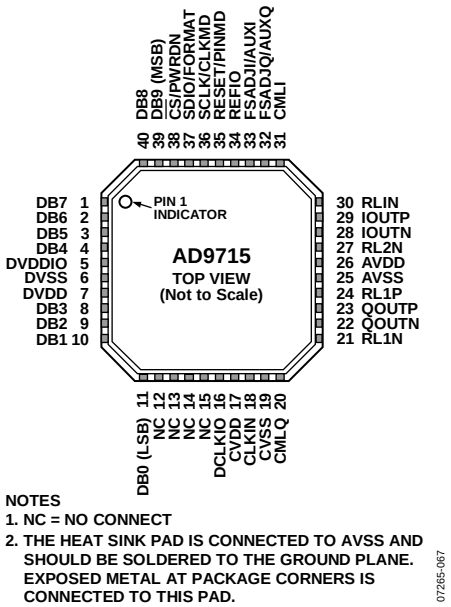

Figure 4. AD9715 Pin Configuration

Table 9. AD9715 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[7:4]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). Provides a 1.8 V output when in internal LDO regulator is enabled.
8 to 10	DB[3:1]	Digital Inputs.
11	DB0 (LSB)	Digital Input (LSB).
12 to 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input Clock. Used to clock data in from digital source.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level.
21	RL1N	Load Resistor (500 Ω) to the CMLQ Pin.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RL1P	Load Resistor (500 Ω) to the CMLQ Pin.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RL2N	Load Resistor (500 Ω) to the CMLI Pin.
28	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
29	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin.
31	CMLI	I DAC Output Common-Mode Level.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust for Q DAC. Connect to AVSS through a resistor. Auxiliary Q DAC. The pin becomes the output of an optional, serial port driven, auxiliary DAC when the internal on-chip, R_{SET}, is enabled.
33	FSADJI/AUXI	Full-Scale Current Output Adjust for I DAC. Connect to AVSS through a resistor. Auxiliary I DAC. The pin becomes the output of an optional, serial port driven, auxiliary DAC when the internal on-chip, R_{SET}, is enabled.
34	REFIO	Reference Input/Output. Serves as reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).

Pin No.	Mnemonic	Description
35	RESET/PINMD	Reset in SPI Mode. Pulse high to reset SPI registers to default values. Pin Mode. A constant Logic 1 puts device into pin mode.
36	SCLK/CLKMD	Serial Clock. Clock input for serial port in spi mode. Clock Mode. In pin mode, CLKMD determines phase of internal retiming clock. DCLKIO = CLKIN: Tie to 0. DCLKIO ≠ CLKIN: Pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output. Bidirectional data line for serial port in spi mode. Data Format. In pin mode, FORMAT determines data format of digital data.
38	$\overline{CS}$/PWRDN	Chip Select. Active low chip select in spi mode. Power Down. In pin mode, PWRDN powers down the device except for the SPI port.
39	DB9 (MSB)	Digital Input (MSB).
40	DB8	Digital Input.
	Heat Sink Pad	The heat sink pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at package corners is connected to this pad.

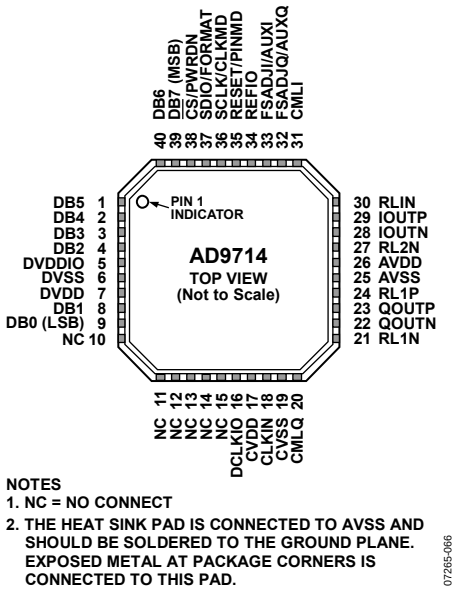

Figure 5. AD9714 Pin Configuration

Table 10. AD9714 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[5:2]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). Provides a 1.8 V output when the internal LDO regulator is enabled.
8	DB1	Digital Inputs.
9	DB0 (LSB)	Digital Input (LSB).
10 to 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input Clock. Used to clock data in from digital source.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level.
21	RL1N	Load Resistor (500 Ω) to the CMLQ Pin.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RL1P	Load Resistor (500 Ω) to the CMLQ Pin.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RL2N	Load Resistor (500 Ω) to the CMLI Pin.
28	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
29	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin.
31	CMLI	I DAC Output Common-Mode Level.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust for Q DAC. Connect to AVSS through a resistor. Auxiliary Q DAC. The pin becomes the output of an optional, serial port driven, auxiliary DAC when the internal on-chip, R_{SET}, is enabled.
33	FSADJI/AUXI	Full-Scale Current Output Adjust for I DAC. Connect to AVSS through a resistor. Auxiliary I DAC. The pin becomes the output of an optional, serial port driven, auxiliary DAC when the internal on-chip, R_{SET}, is enabled.
34	REFIO	Reference Input/Output. Serves as reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).

Pin No.	Mnemonic	Description
35	RESET/PINMD	Reset in SPI Mode. Pulse high to reset SPI registers to default values. Pin Mode. A constant Logic 1 puts device into pin mode.
36	SCLK/CLKMD	Serial Clock. Clock input for serial port in spi mode. Clock Mode. In pin mode, CLKMD determines phase of internal retiming clock. DCLKIO = CLKIN: Tie to 0. DCLKIO ≠ CLKIN: Pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output. Bidirectional data line for serial port in spi mode. Data Format. In pin mode, FORMAT determines data format of digital data.
38	$\overline{CS}$/PWRDN	Chip Select. Active low chip select in spi mode. Power Down. In pin mode, PWRDN powers down the device except for the SPI port.
39	DB7 (MSB)	Digital Input (MSB).
40	DB6	Digital Input.
	Heat Sink Pad	The heat sink pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at package corners is connected to this pad.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD, DVDD, DVDDIO, CVDD = 1.8 V, I_{OUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

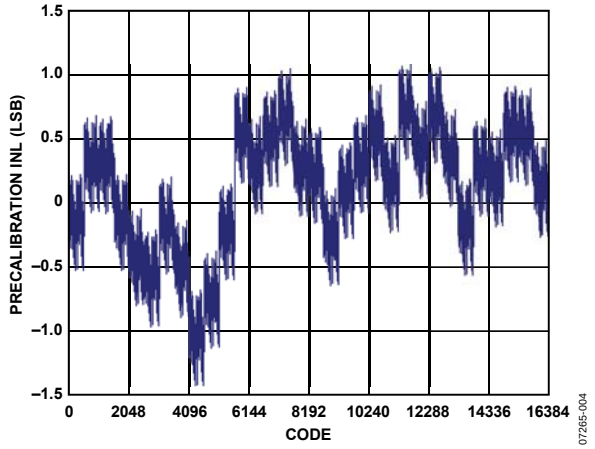

Figure 6. AD9717 Precalibration INL at 1.8 V

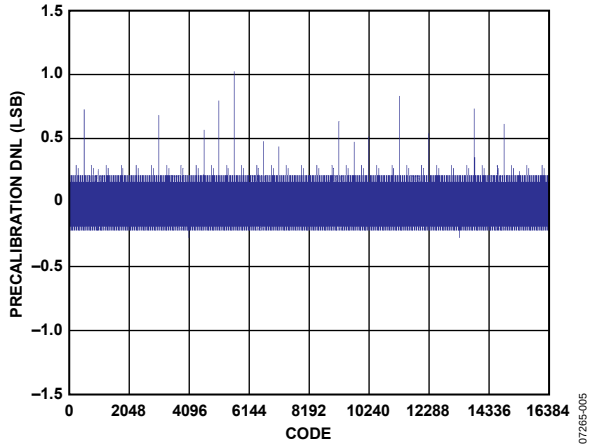

Figure 7. AD9717 Precalibration DNL at 1.8 V

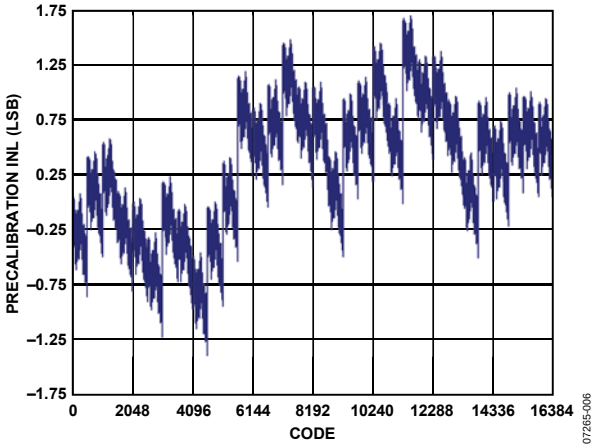

Figure 8. AD9717 Precalibration INL at 3.3 V

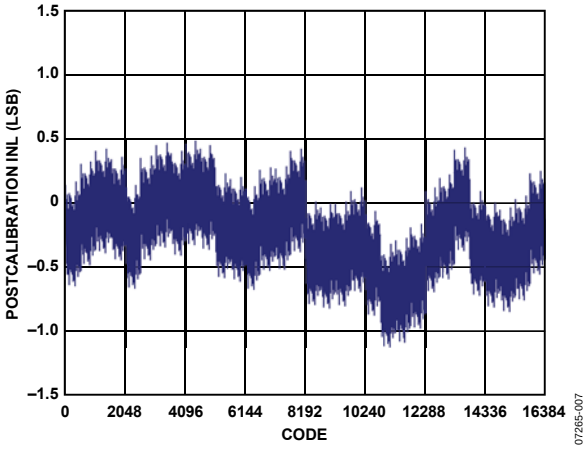

Figure 9. AD9717 Postcalibration INL at 1.8 V

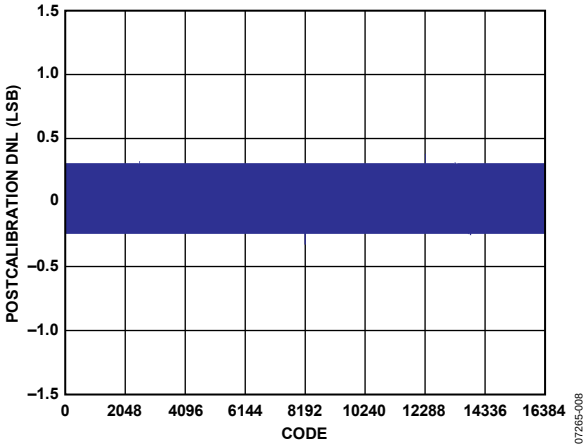

Figure 10. AD9717 Postcalibration DNL at 1.8 V

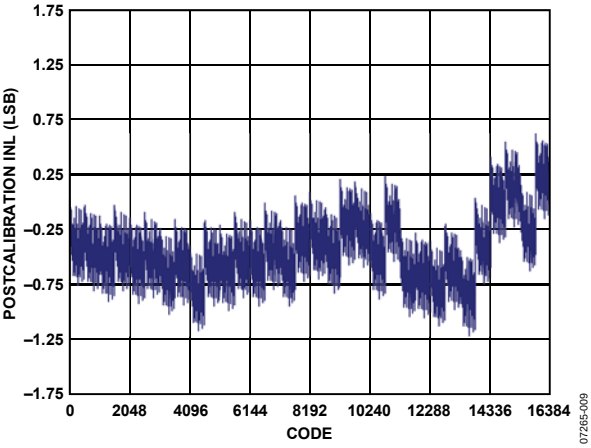

Figure 11. AD9717 Postcalibration INL at 3.3 V

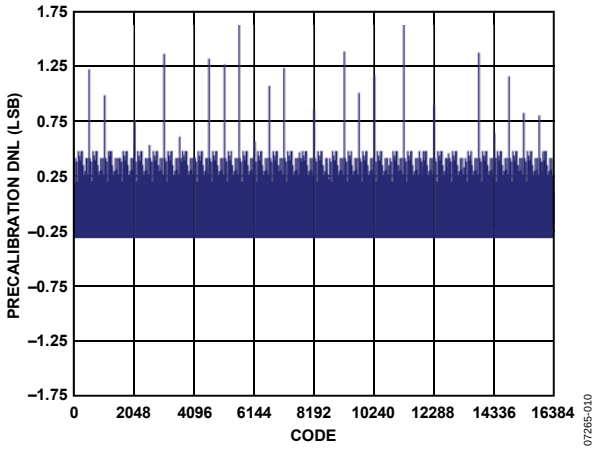

Figure 12. AD9717 Precalibration DNL at 3.3 V

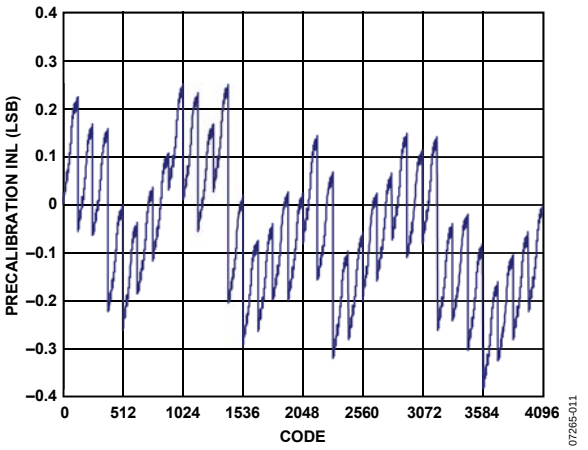

Figure 13. AD9716 Precalibration INL at 1.8 V

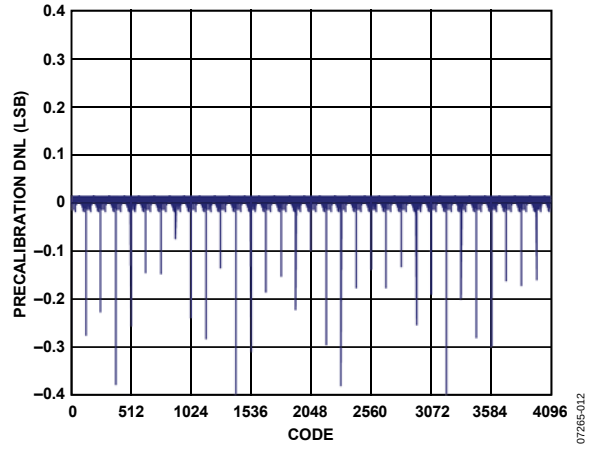

Figure 14. AD9716 Precalibration DNL at 1.8 V

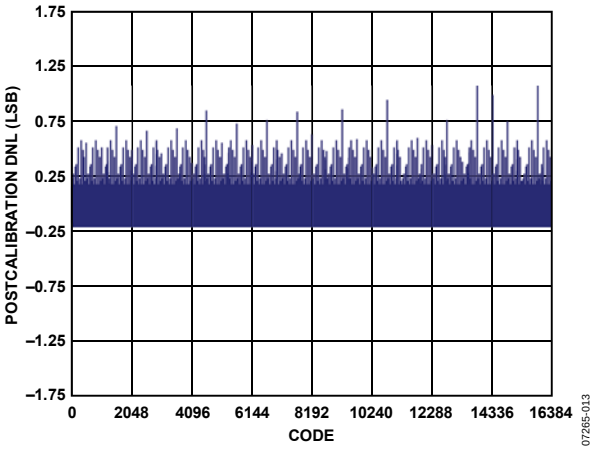

Figure 15. AD9717 Postcalibration DNL at 3.3 V

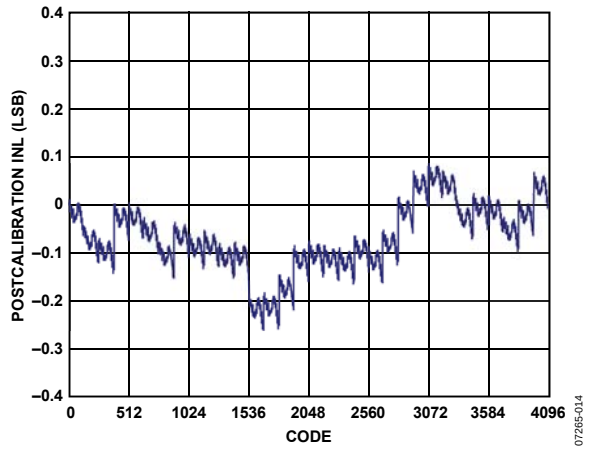

Figure 16. AD9716 Postcalibration INL at 1.8 V

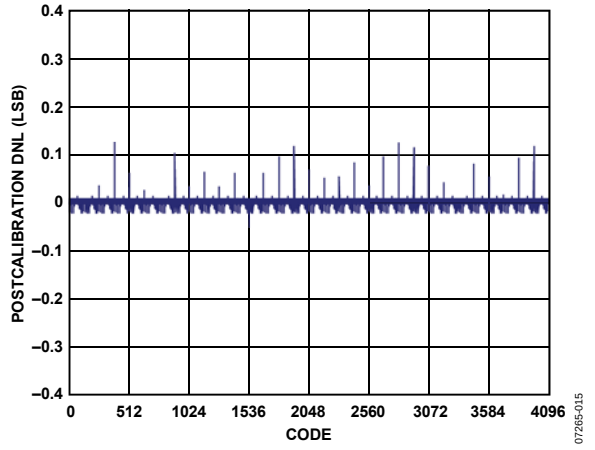

Figure 17. AD9716 Postcalibration DNL at 1.8 V

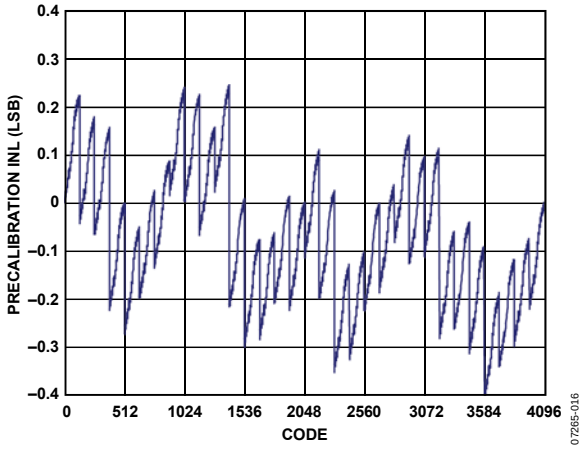

Figure 18. AD9716 Precalibration INL at 3.3 V

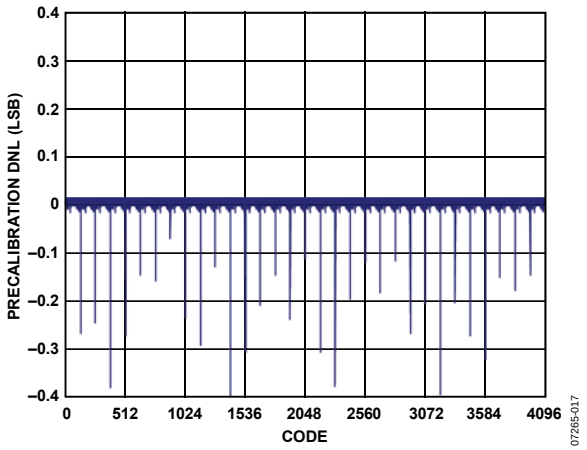

Figure 19. AD9716 Precalibration DNL at 3.3 V

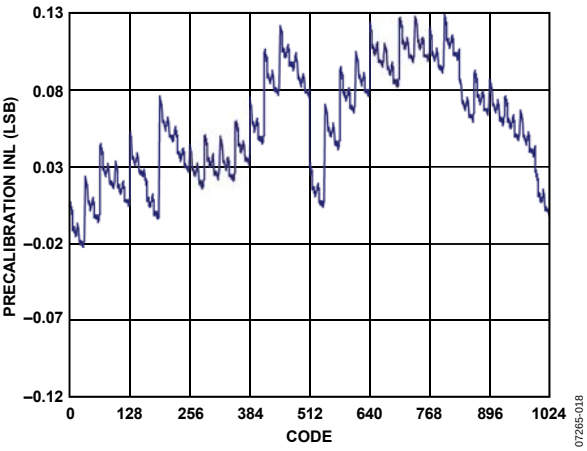

Figure 20. AD9715 Precalibration INL at 1.8 V

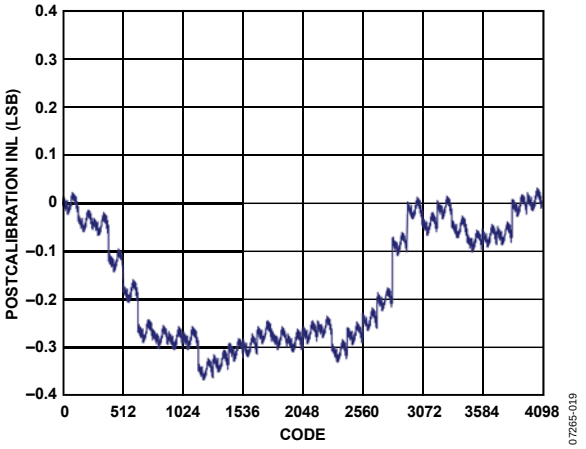

Figure 21. AD9716 Postcalibration INL at 3.3 V

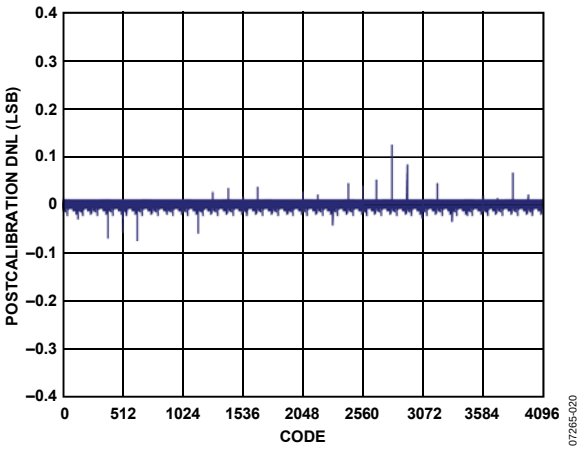

Figure 22. AD9716 Postcalibration DNL at 3.3 V

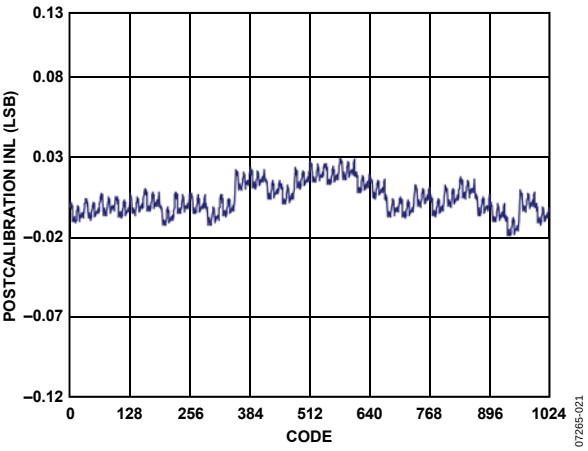

Figure 23. AD9715 Postcalibration INL at 1.8 V

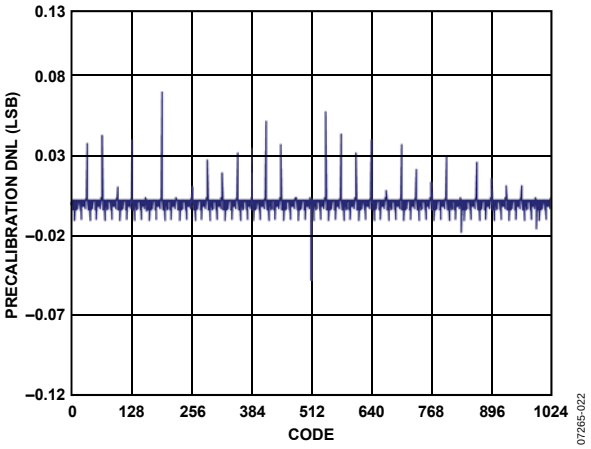

Figure 24. AD9715 Precalibration DNL at 1.8 V

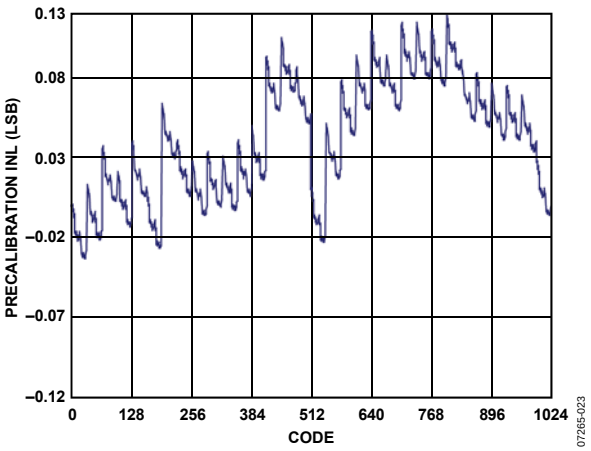

Figure 25. AD9715 Precalibration INL at 3.3 V

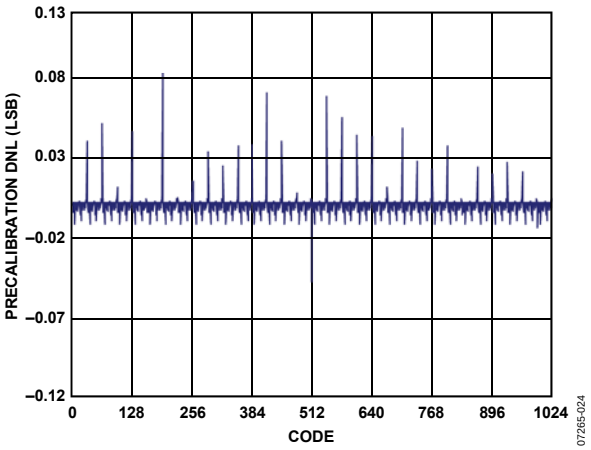

Figure 26. AD9715 Precalibration DNL at 3.3 V

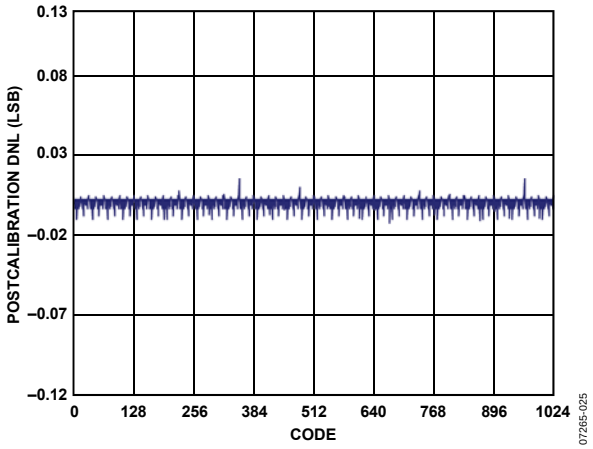

Figure 27. AD9715 Postcalibration DNL at 1.8 V

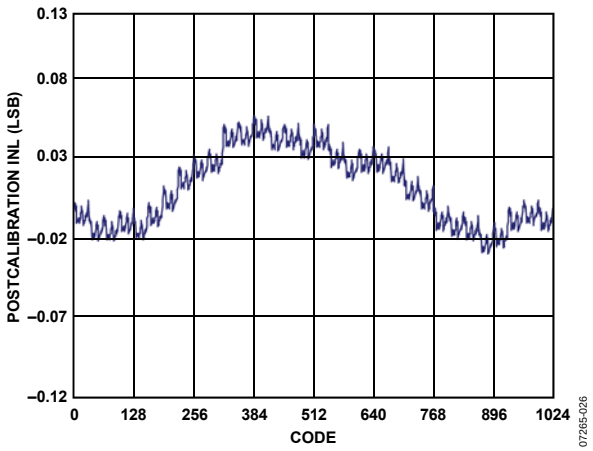

Figure 28. AD9715 Postcalibration INL at 3.3 V

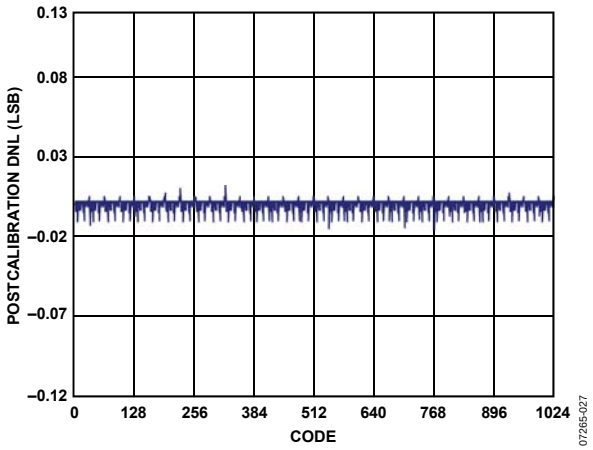

Figure 29. AD9715 Postcalibration DNL at 3.3 V

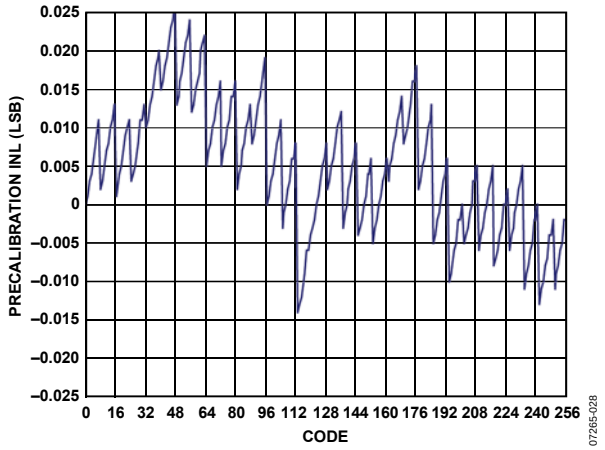

Figure 30. AD9714 Precalibration INL at 1.8 V

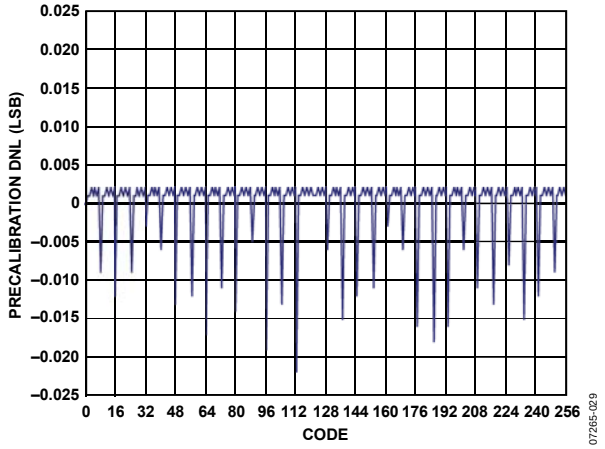

Figure 31. AD9714 Precalibration DNL at 1.8 V

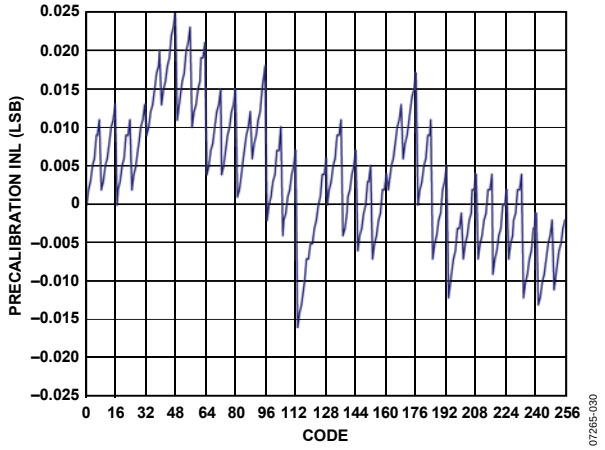

Figure 32. AD9714 Precalibration INL at 3.3 V

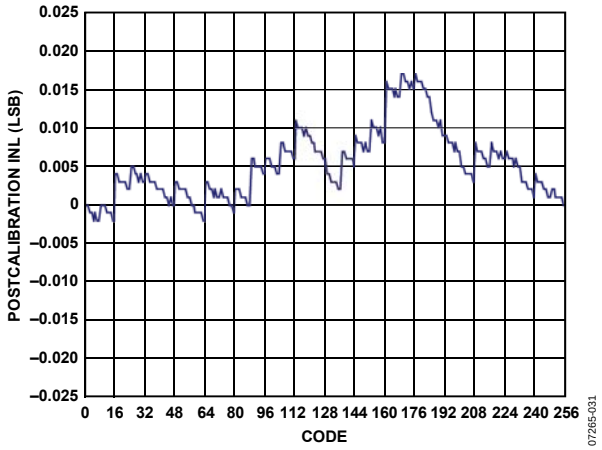

Figure 33. AD9714 Postcalibration INL at 1.8 V

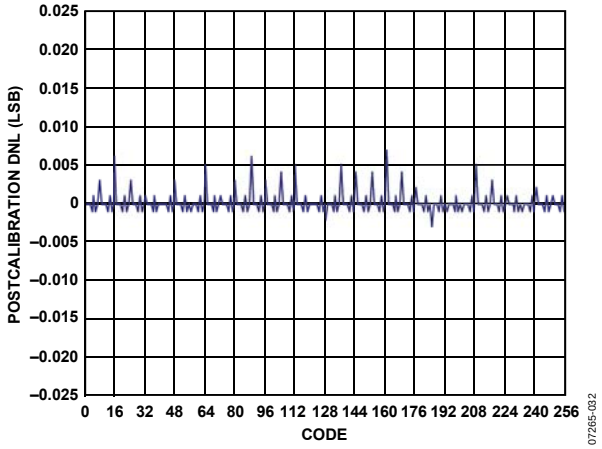

Figure 34. AD9714 Postcalibration DNL at 1.8 V

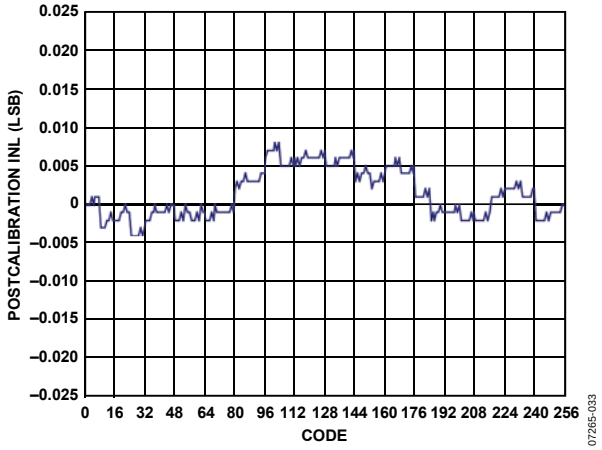

Figure 35. AD9714 Postcalibration INL at 3.3 V

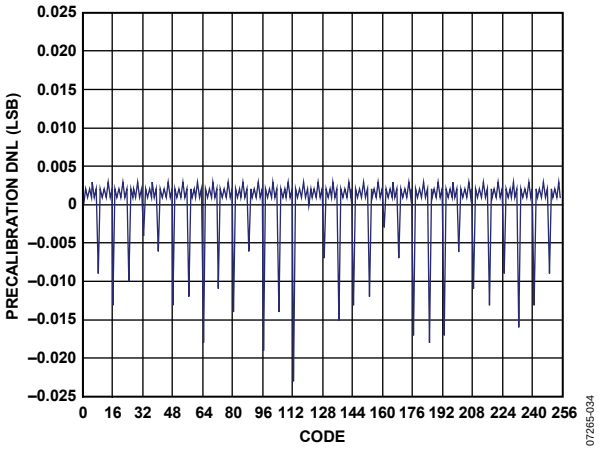

Figure 36. AD9714 Precalibration DNL at 3.3 V

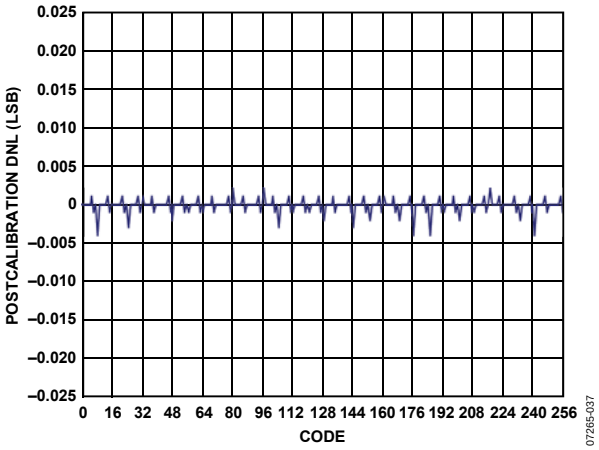

Figure 39. AD9714 Postcalibration DNL at 3.3 V

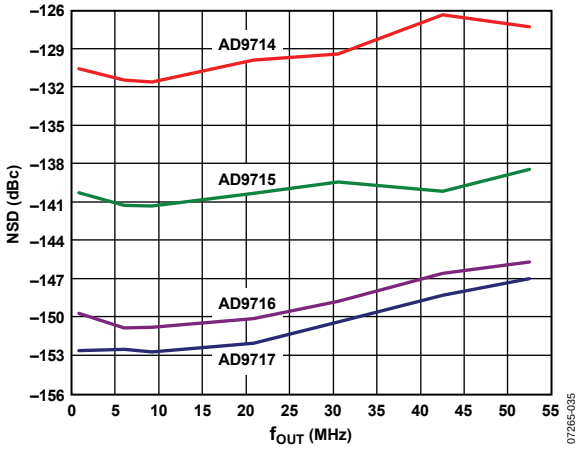

Figure 37. Noise Spectral Density at 3.3 V

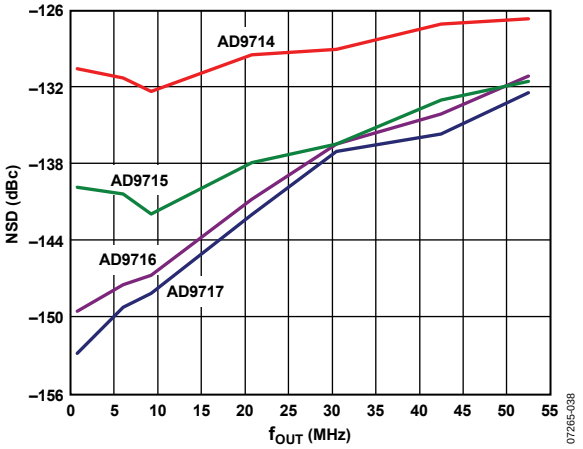

Figure 40. AD9714/AD9715/AD9716/AD9717 Noise Spectral Density at 1.8 V

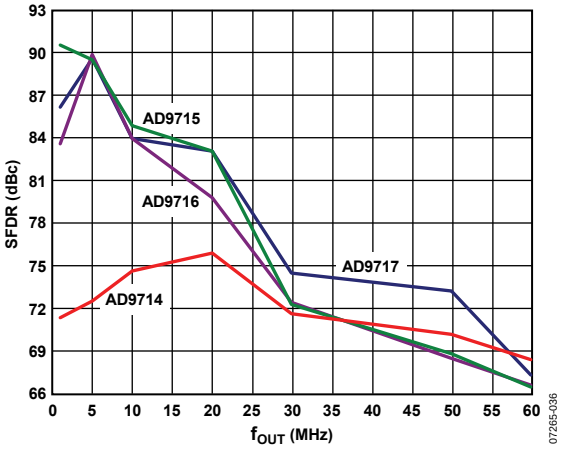

Figure 38. AD9714/AD9715/AD9716/AD9717 SFDR at 3.3 V

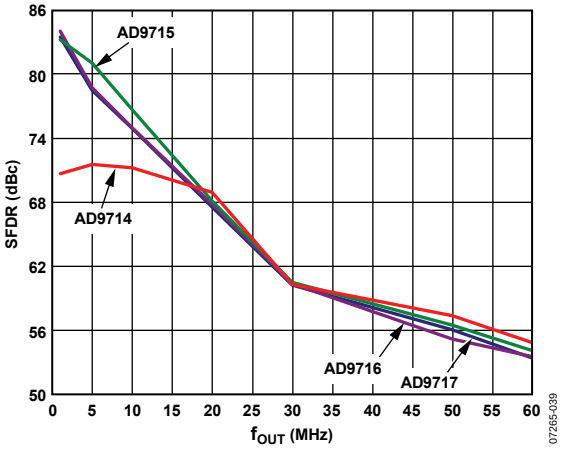

Figure 41. AD9714/AD9715/AD9716/AD9717 SFDR at 1.8 V

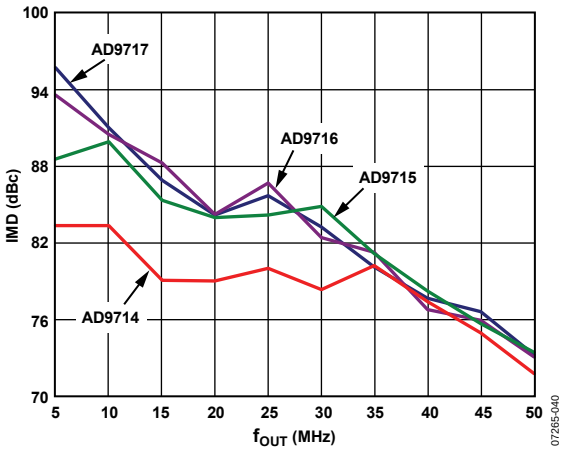

Figure 42. AD9714/AD9715/AD9716/AD9717 IMD at 3.3 V

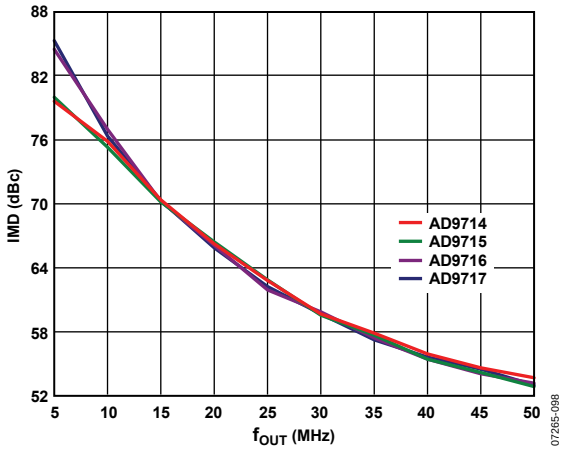

Figure 43. AD9714/AD9715/AD9716/AD9717 IMD at 1.8 V

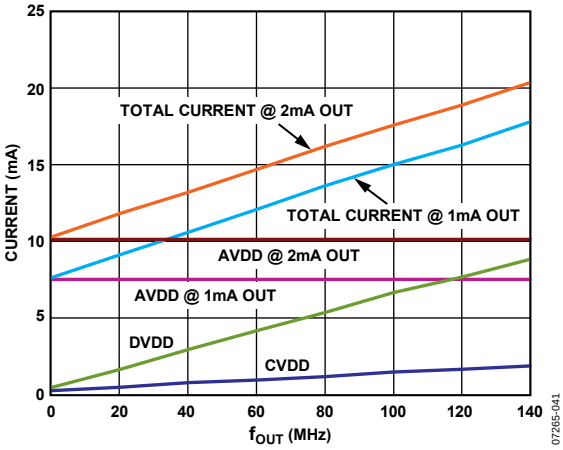

Figure 44. Supply Current vs. Frequency at 1.8 V

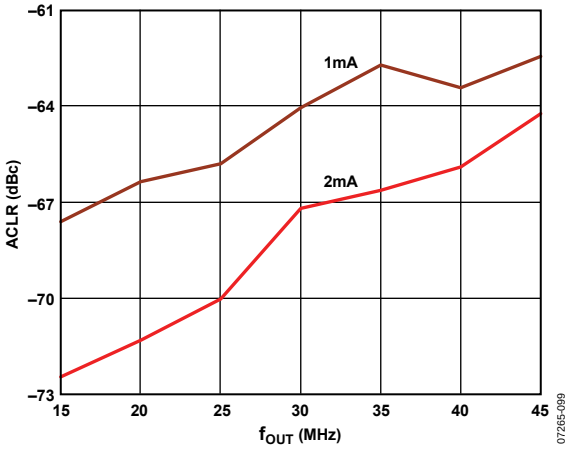

Figure 45. 1 Carrier ACLR First Adjacent Channel at 1.8 V

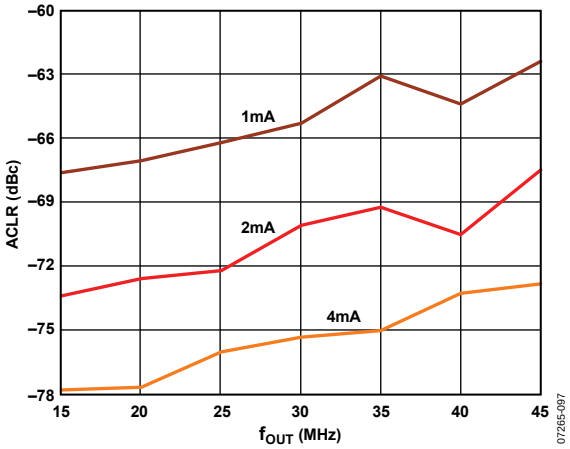

Figure 46. 1 Carrier ACLR First Adjacent Channel at 3.3 V

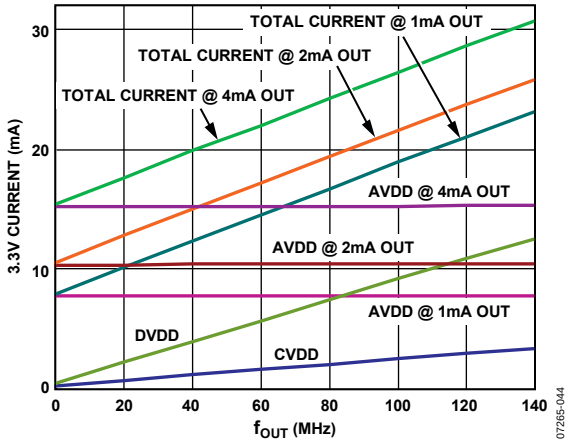

Figure 47. Supply Current vs. Frequency at 3.3 V

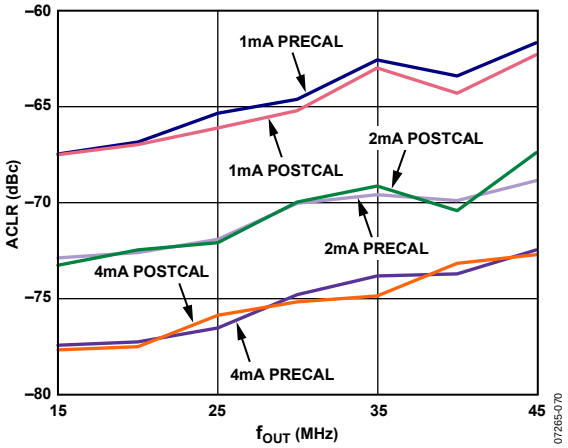

Figure 48. AD9717 1-Carrier W-CDMA First Adjacent Channel ACLR 3.3 V

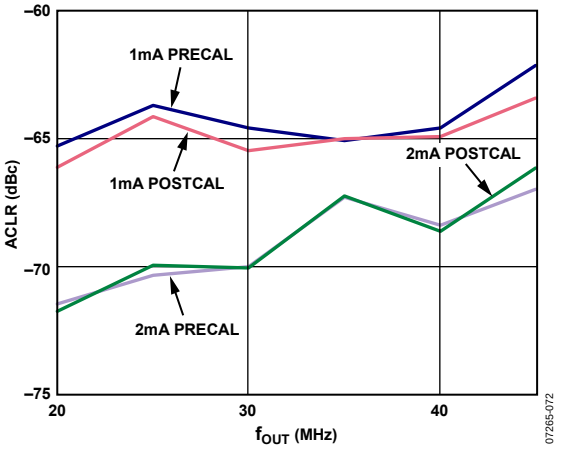

Figure 51. AD9717 1-Carrier W-CDMA Third Adjacent Channel ACLR 1.8 V

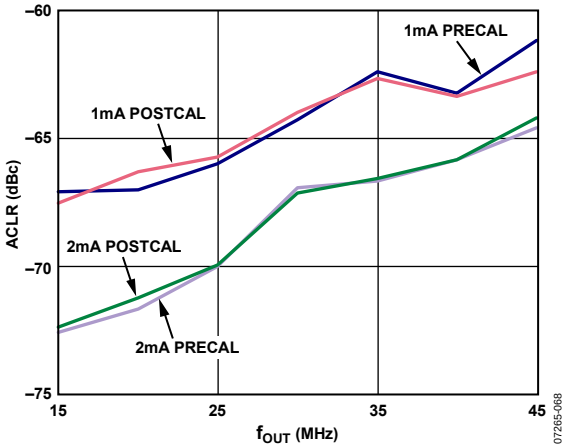

Figure 49. AD9717 1-Carrier W-CDMA First Adjacent Channel ACLR 1.8 V

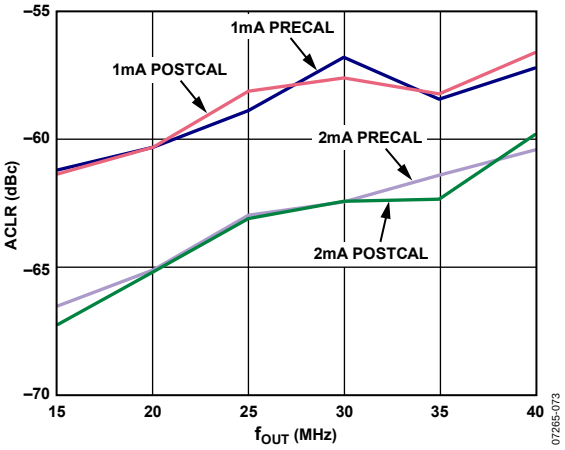

Figure 52. AD9717 1-Carrier W-CDMA First Adjacent Channel ACLR 1.8 V

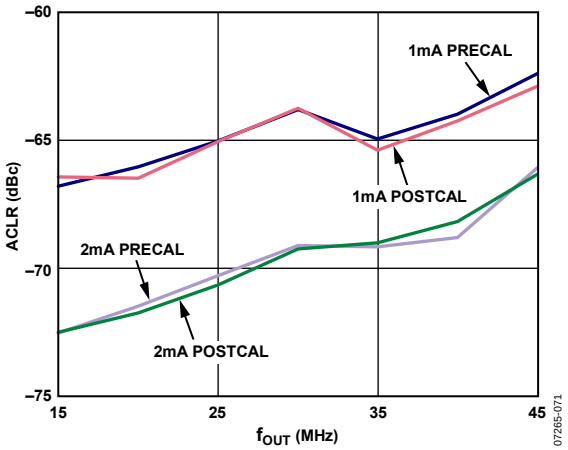

Figure 50. AD9717 1-Carrier W-CDMA Second Adjacent Channel ACLR 1.8 V

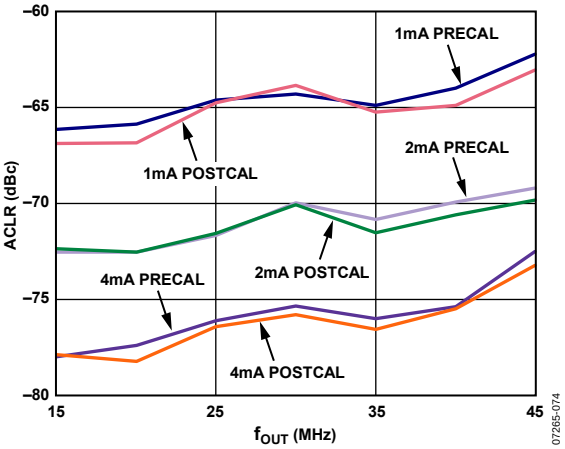

Figure 53. AD9717 1-Carrier W-CDMA Second Adjacent Channel ACLR 3.3 V

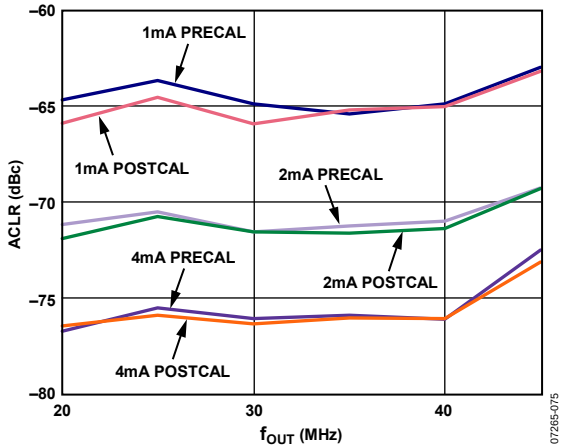

Figure 54. AD9717 1-Carrier W-CDMA Third Adjacent Channel ACLR 3.3 V

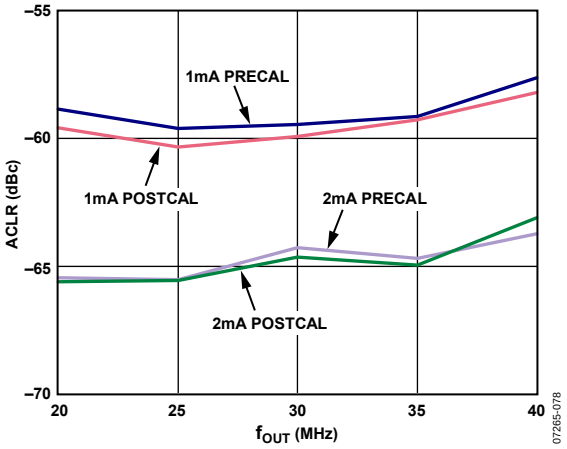

Figure 57. AD9717 2-Carrier W-CDMA Third Adjacent Channel ACLR 1.8 V

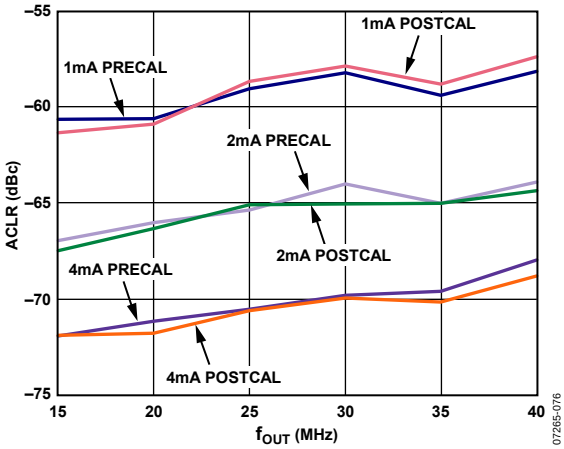

Figure 55. AD9717 1-Carrier W-CDMA First Adjacent Channel ACLR 3.3 V

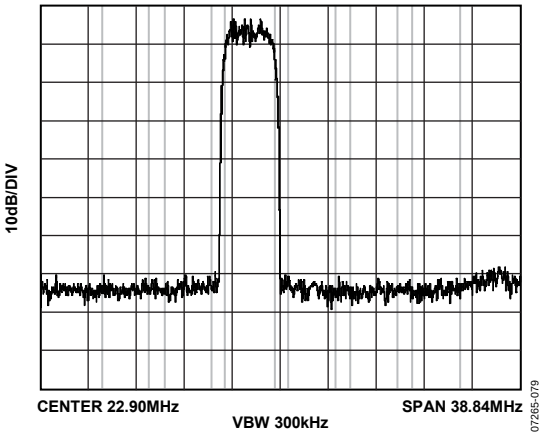

Figure 58. AD9717 ACLR 1-Carrier 1.8 V

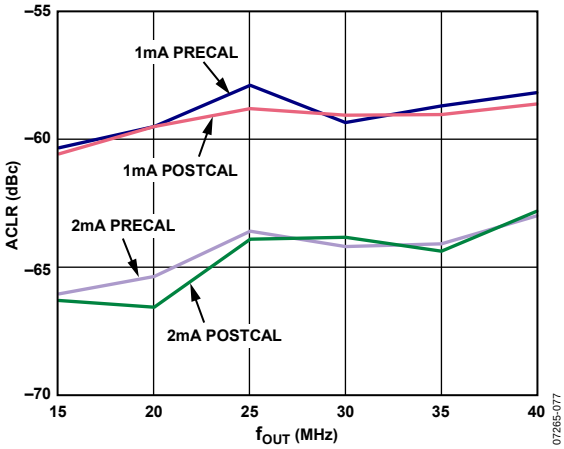

Figure 56. AD9717 2-Carrier W-CDMA Second Adjacent Channel ACLR 1.8 V

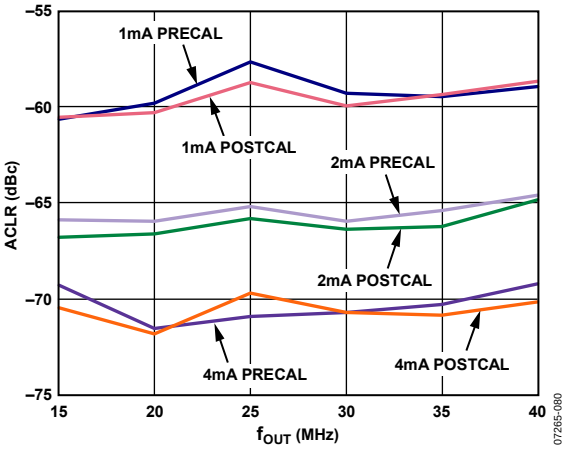

Figure 59. AD9717 2-Carrier W-CDMA Second Adjacent Channel ACLR 3.3 V

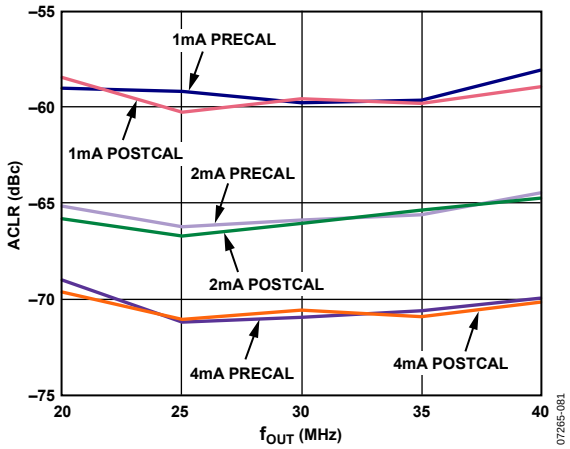

Figure 60. AD9717 2-Carrier W-CDMA Third Adjacent Channel ACLR 3.3 V

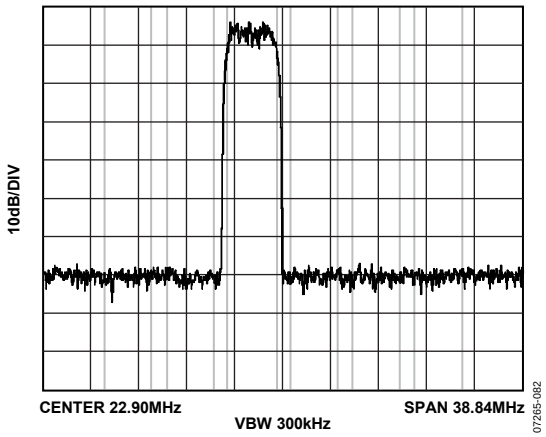

Figure 61. AD9717 ACLR 1-Carrier 3.3 V

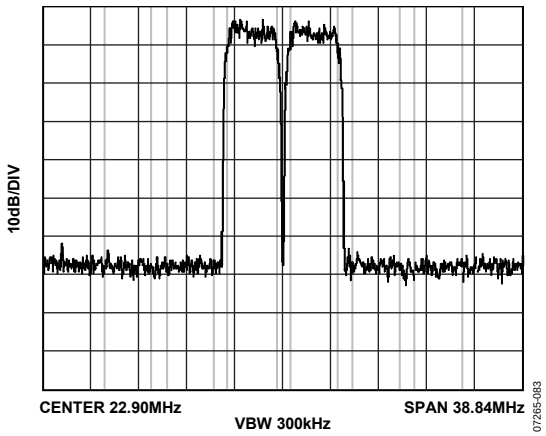

Figure 62.AD9717 ACLR 2-Carrier 1.8 V

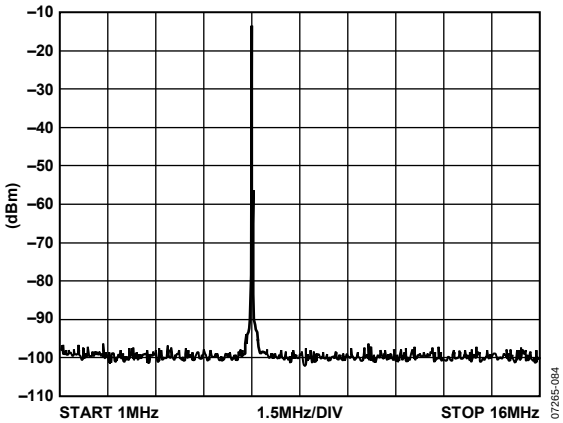

Figure 63. AD9717 Single Tone 1.8 V

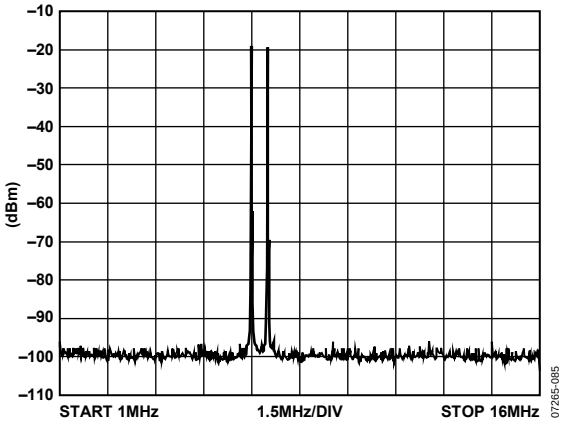

Figure 64. AD9717 Two Tone 1.8 V

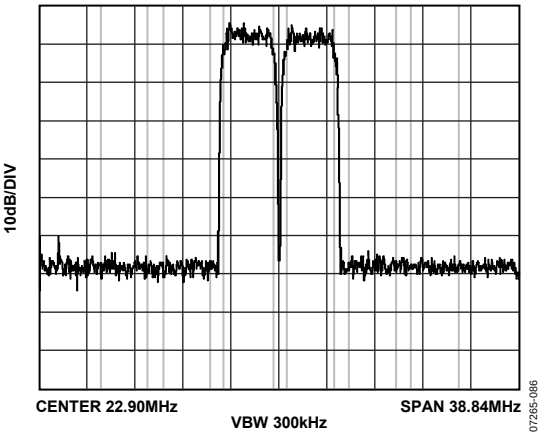

Figure 65. AD9717 ACLR 2-Carrier 3.3 V

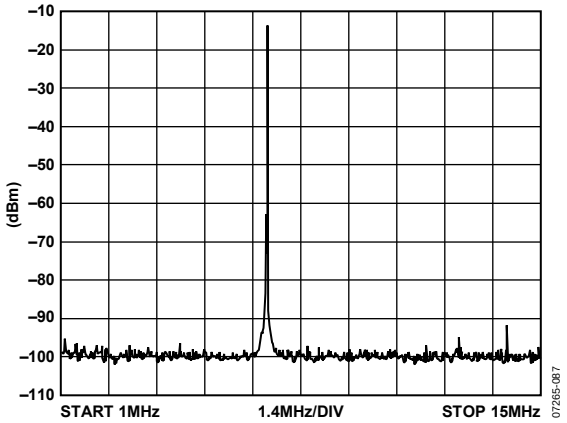

Figure 66. AD9717 Single Tone, 3.3 V

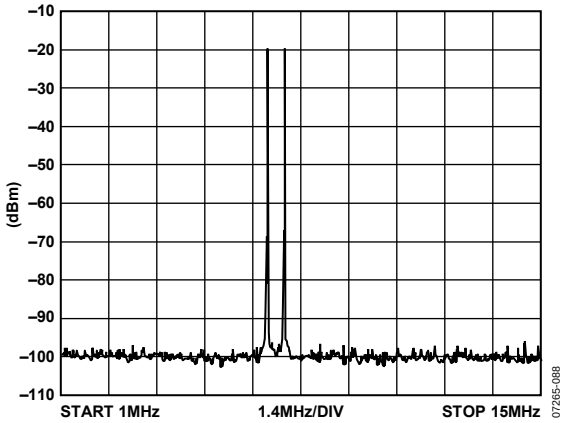

Figure 67. AD9717 Two Tone, 3.3 V

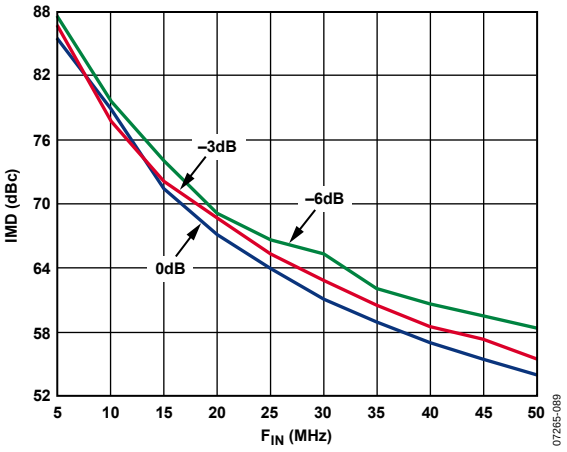

Figure 68. IMD vs. Digital Input Level 1.8 V

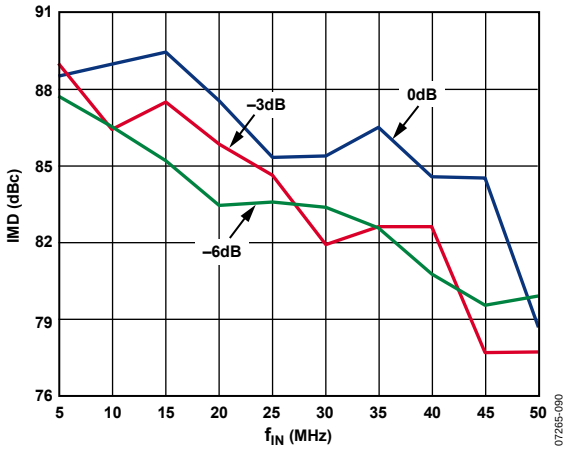

Figure 69. IMD vs. Digital Input Level 3.3 V

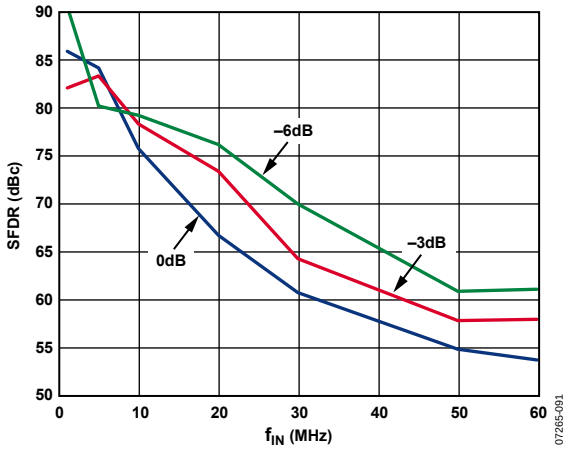

Figure 70. SFDR vs. Digital Input Level 3.3 V

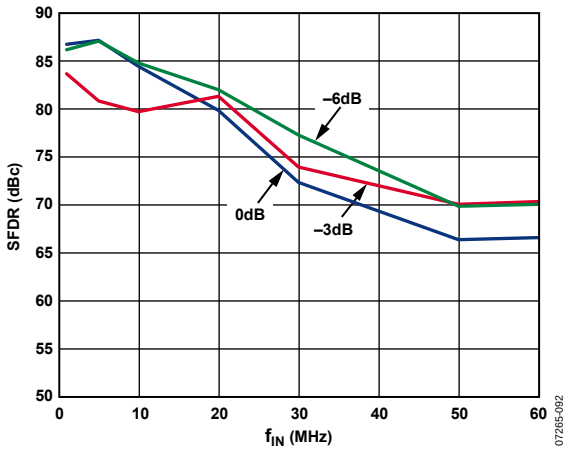

Figure 71. SFDR vs. Digital Input Level 1.8 V

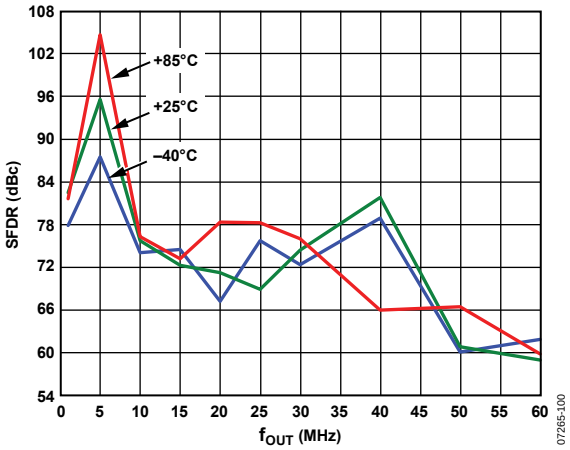

Figure 72. SFDR Over Temperature at 3.3 V

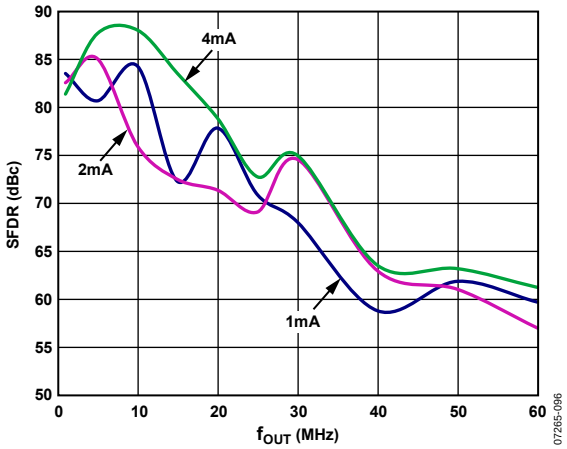

Figure 74. SFDR vs. f_{OUT}

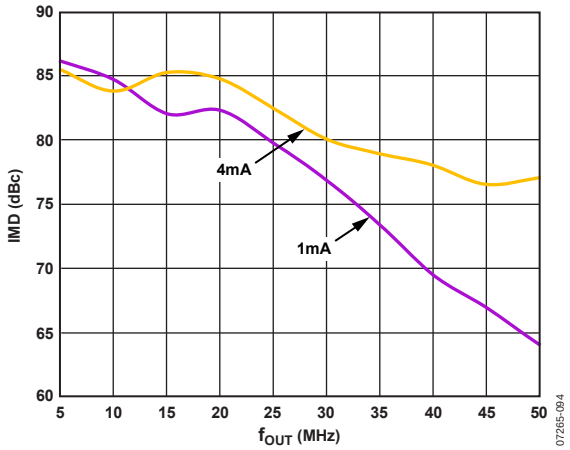

Figure 73. IMD vs. f_{OUT}, F_{CLK} = 125 MHz

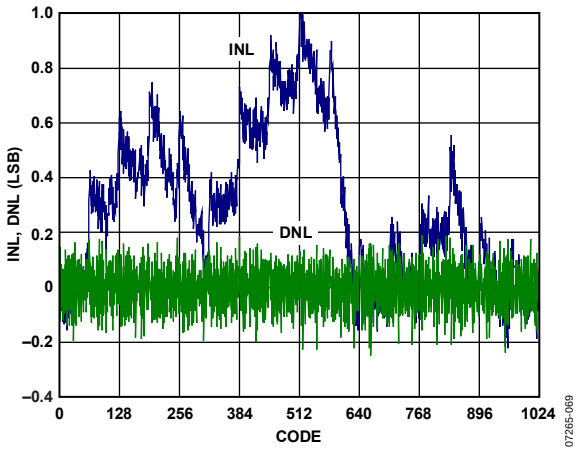

Figure 75. AUXDAC DNL and INL

TERMINOLOGY

Linearity Error or Integral Nonlinearity (INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
Offset error is the deviation of the output current from the ideal of zero. For I_{OUTP}, 0 mA output is expected when the inputs are all 0. For I_{OUTN}, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range
Output compliant range is the range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient value (25°C) to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range per degree Celsius (ppm FSR/°C). For reference drift, the drift is reported in parts per million per degree Celsius (ppm/°C).

Power Supply Rejection
Power supply rejection is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal between dc and the frequency equal to half the input data rate.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in dBc between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

THEORY OF OPERATION

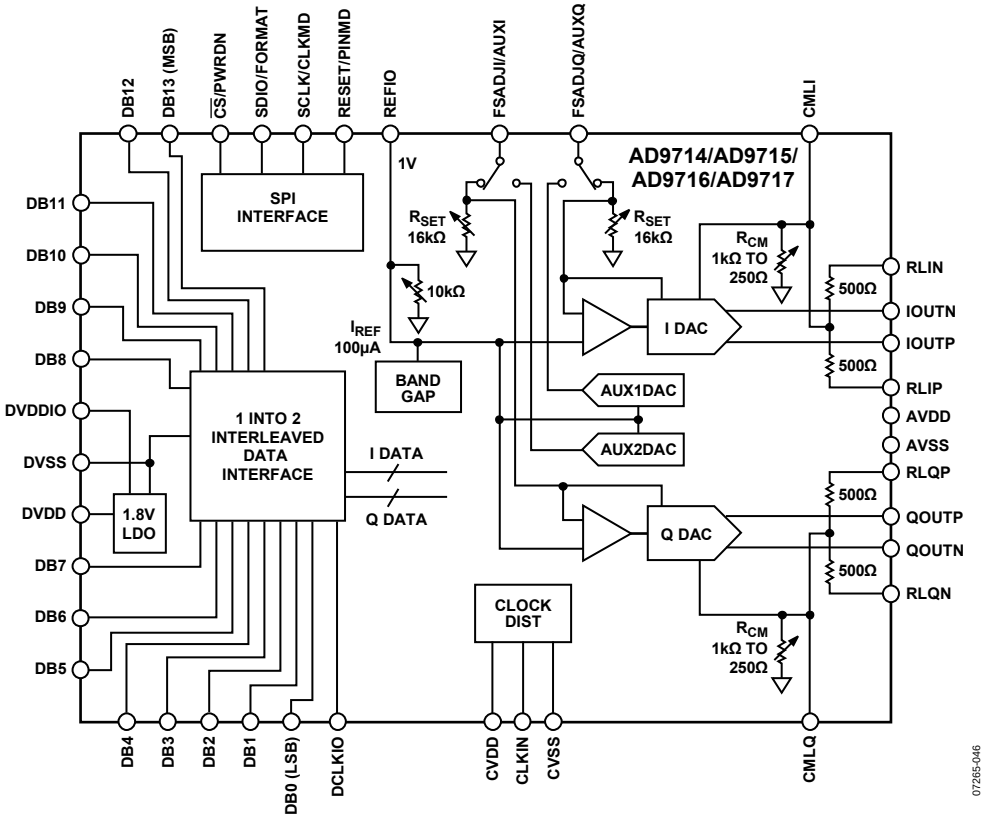

Figure 76. Simplified Block Diagram

Figure 76 shows a simplified block diagram of the AD9714/AD9715/AD9716/AD9717 that consists of two DACs, digital control logic, and a full-scale output current control. The DAC contains a PMOS current source array capable of providing a nominal full-scale current (I_{OUTFS}) of 2 mA and a maximum of 4 mA. The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16 of an MSB current source. The remaining LSBs are binary weighted fractions of the current sources of the middle bits. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the high output impedance of the DAC (that is, >200 MΩ).

All of these current sources are switched to one or the other of the two output nodes (I_{OUTP} or I_{OUTN}) via PMOS differential current switches. The switches are based on the architecture that was pioneered in the AD976x family, with further refinements to reduce distortion contributed by the switching transient. This switch architecture also reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital I/O sections of the AD9714/AD9715/AD9716/AD9717 have separate power supply inputs (AVDD and DVDDIO) that can operate independently over a 1.7 V to 3.5 V range. The core digital section, which is powered optionally by either the on-chip LDO or through DVDD (Pin 7), is capable of operating at a rate of up to 125 MSPS. It consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.0 V band gap voltage reference, and a reference control amplifier.

Each DAC full-scale output current is regulated by the reference control amplifier and can be set from 1 mA to 4 mA via an external resistor, R_{SET}, connected to its full-scale adjust pin (FSADJ).

The external resistor, in combination with both the reference control amplifier and voltage reference, V_{REFIO}, sets the reference current, I_{REF}, which is replicated to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is $32 \times I_{REF}$.

Optional on-chip R_{SET} resistors are provided that can be programmed between a nominal value of 8 kΩ to 32 kΩ (4 mA to 1 mA I_{OUTFS}).

The AD9714/AD9715/AD9716/AD9717 provide the option of setting the output common mode to a value other than ACOM via the output common-mode pins (CMLI and CMLQ). This facilitates directly interfacing the output of the AD9714/AD9715/AD9716/AD9717 to components that require common-mode levels greater than 0 V.

SERIAL PERIPHERAL INTERFACE (SPI)

The serial port of the AD9714/AD9715/AD9716/AD9717 is a flexible, synchronous serial communications port allowing easy interfacing to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI® and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9714/AD9715/AD9716/AD9717. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The serial interface port of the AD9714/AD9715/AD9716/AD9717 is configured as a single I/O pin on the SDIO pin.

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to a communications cycle on the AD9714/AD9715/AD9716/AD9717. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9714/AD9715/AD9716/AD9717, coinciding with the first eight SCLK rising edges. In Phase 2, the instruction byte provides the serial port controller of the AD9714/AD9715/AD9716/AD9717 with information regarding the data transfer cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9714/AD9715/AD9716/AD9717.

A Logic 1 on Pin 35 (RESET/PINMD), followed by a Logic 0, resets the SPI port timing to the initial state of the instruction cycle. This is true regardless of the present state of the internal registers or the other signal levels present at the inputs to the SPI port. If the SPI port is in the midst of an instruction cycle or a data transfer cycle, none of the present data is written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9714/AD9715/AD9716/AD9717 and the system controller. Phase 2 of the communication cycle is a transfer of one, two, three, or four data bytes, as determined by the instruction byte. Using one multibyte transfer is the preferred method. Single byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte.

INSTRUCTION BYTE

The instruction byte contains the information shown in Table 11.

Table 11.

MSB							LSB
DB7	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

R/$\overline{W}$ (Bit 7 of the instruction byte) determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation. Logic 0 indicates a write operation. N1 and N0 (Bit 6 and Bit 5 of the instruction byte) determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in Table 12.

Table 12. Byte Transfer Count

N1	N0	Description
0	0	Transfer 1 byte
0	1	Transfer 2 bytes
1	0	Transfer 3 bytes
1	1	Transfer 4 bytes

A4, A3, A2, A1, and A0 (Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0 of the instruction byte) determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The following register addresses are generated internally, based on the LSBFIRST bit (Register 0x00, Bit 6).

SERIAL INTERFACE PORT PIN DESCRIPTIONS

SCLK—Serial Clock

The serial clock pin is used to synchronize data to and from the AD9714/AD9715/AD9716/AD9717 and to run the internal state machines. The SCLK maximum frequency is 20 MHz. All data input to the AD9714/AD9715/AD9716/AD9717 is registered on the rising edge of SCLK. All data is driven out of the AD9714/AD9715/AD9716/AD9717 on the falling edge of SCLK.

$\overline{CS}$—Chip Select

An active low input starts and gates a communications cycle. It allows more than one device to be used on the same serial communications lines. The SDIO/FORMAT pin reaches a high impedance state when this input is high. Chip select should stay low during the entire communications cycle.

SDIO—Serial Data I/O

The SDIO pin is used as a bidirectional data line to transmit and receive data.

MSB/LSB TRANSFERS

The serial port of the AD9714/AD9715/AD9716/AD9717 can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the LSBFIRST bit (Register 0x00, Bit 6). The default is MSB first (LSBFIRST = 0).

When LSBFIRST = 0 (MSB first), the instruction and data bytes must be written from the most significant bit to the least significant bit. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow in order from a high address to a low address. In MSB first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communications cycle.

When LSBFIRST = 1 (LSB first), the instruction and data bytes must be written from the least significant bit to the most significant bit. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial port internal byte address generator increments for each byte of the multibyte communication cycle.

The serial port controller data address of the AD9714/AD9715/AD9716/AD9717 decrements from the data address written toward 0x00 for multibyte I/O operations if the MSB first mode is active. The serial port controller address increments from the data address written toward 0x1F for multibyte I/O operations if the LSB first mode is active.

SERIAL PORT OPERATION

The serial port configuration of the AD9714/AD9715/AD9716/AD9717 is controlled by Register 0x00. It is important to note that the configuration changes immediately upon writing to the last bit of the register. For multibyte transfers, writing to this register can occur during the middle of the communications cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communications cycle.

The same considerations apply to setting the software reset, RESET (Register 0x00, Bit 5). All registers are set to their default values except Register 0x00, which remains unchanged.

Use of single-byte transfers or initiating a software reset is recommended when changing serial port configurations to prevent unexpected device behavior.

PIN MODE

The AD9714/AD9715/AD9716/AD9717 can also be operated without ever writing to the serial port. With RESET/PINMD pin tied high, the SCLK pin becomes CLKMD to provide for clock mode control (see the Retimer section), the former SDIO pin selects the input data format, and the $\overline{CS}$ pin serves to power down the device.

Operation is otherwise exactly as defined by the default register values in Table 12, therefore external resistors at FSADJI and FSADJQ are needed to set the DAC currents, and both DACs are active. This is also a convenient quick checkout mode.

DAC currents can be externally adjusted in pin mode by sourcing or sinking currents at the FSADJI/AUXI and FSADJQ/AUXQ pins as desired with the fixed resistors installed. An op amp output with appropriate series resistance would be one of many possibilities. This has the same effect as changing the resistor value. Place at least 10 kΩ resistors in series right at the DAC to guard against accidental short circuits and noise modulation. The REFIO pin can be adjusted ±25% in a similar manner, if desired.

SPI REGISTER MAP

Table 13.

Name	Addr	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI Control	0x00	0x00		LSBFIRST	RESET	LNGINS				
Power Down	0x01	0x40	LDOOFF	LDOSTAT	PWRDN	Q DACOFF	I DACOFF	QCLKOFF	ICLKOFF	EXTREF
Data Control	0x02	0x34	TWOS		IFIRST	IRISING	SIMULBIT	DCI_EN	DCOSGL	DCODBL
I DAC Gain	0x03	0x00	I DACGAIN[5:0]							
IRSET	0x04	0x00	IRSETEN	IRSET[5:0]						
IRCML	0x05	0x00	IRCMLEN	IRCML[5:0]						
Q DAC Gain	0x06	0x00	Q DACGAIN[5:0]							
QRSET	0x07	0x00	QRSETEN	QRSET[5:0]						
QRCML	0x08	0x00	QRCMLEN	QRCML[5:0]						
AUXDAC Q	0x09	0x00	QAUXDAC[7:0]							
AUX CTLQ	0x0A	0x00	QAUXEN	QAUXRNG[1:0]		QAUXOFS[2:0]			QAUXDAC[9:8]	
AUXDAC I	0x0B	0x00	IAUXDAC[7:0]							
AUX CTLI	0x0C	0x00	IAUXEN	IAUXRNG[1:0]		IAUXOFS[2:0]			IAUXDAC[9:8]	
Reference Resistor	0x0D	0x00	RREF[5:0]							
Cal Control	0x0E	0x00	PRELDQ	PRELDI	CALSELQ	CALSELI	CALCLK	DIVSEL[2:0]		
Cal Memory	0x0F	0x00	CALSTATQ	CALSTATI			CALMEMQ[1:0]		CALMEMI[1:0]	
Memory Address	0x10	0x00	MEMADDR[5:0]							
Memory Data	0x11	0x34	MEMDATA[5:0]							
Memory R/W	0x12	0x00	CALRSTQ	CALRSTI		CALEN	SMEMWR	SMEMRD	UNCALQ	UNCALI
CLKMODE	0x14	0x00	CLKMODEQ[1:0]			SEARCHING	REACQUIRE	CLKMODEN	CLKMODEI[1:0]	
Version	0x1F	N/A	VERSION[7:0]							

SPI REGISTER DESCRIPTIONS

Reading these registers returns previously written values for all defined register bits, unless otherwise noted.

Table 14.

Register	Address	Bit	Name	Function
SPI Control	0x00	6	LSBFIRST	0: MSB first, per SPI standard 1: LSB first, per SPI standard Note that the user must always change the LSB/MSB order in single-byte instructions to avoid erratic behavior due to bit order errors
		5	RESET	Execute software reset of SPI and controllers, reload default register values except Register 0x00 1: Set software reset; write 0 on the next (or any following) cycle to release the reset
		4	LNGINS	0: The SPI instruction word utilizes a 5-bit address 1: The SPI instruction word utilizes a 13-bit address
Power Down	0x01	7	LDOOFF	1: turn core LDO voltage regulator off
		6	LDOSTAT	0: Indicates core LDO voltage regulator is off 1: Indicates core LDO voltage regulator is on
		5	PWRDN	1: Powers down all analog and digital circuitry except for SPI logic
		4	Q DACOFF	1: Turns off Q DAC output current
		3	I DACOFF	1: Turns off I DAC output current
		2	QCLKOFF	1: Turns off Q DAC clock
		1	ICLKOFF	1: Turns off I DAC clock
		0	EXTREF	1: Powers down internal voltage reference (external reference required)
Data Control	0x02	7	TWOS	0: Unsigned binary input data format 1: Twos complement input data format
		5	IFIRST	0: Pairing of data—Q first of pair on data input pads 1: Pairing of data—I first of pair on data input pads (default)
		4	IRISING	0: Q data latched on DCLKIO rising edge 1: I data latched on DCLKIO falling edge (default)
		3	SIMULBIT	0: Allows simultaneous input and output enable on DCLKIO 1: Disallows simultaneous input and output enable on DCLKIO
		2	DCI_EN	Controls the use of DCLKIO pad for data clock input 0: Data clock input disabled 1: Data clock input enabled (default)
		1	DCOSGL	Controls the use of DCLKIO pad for data clock output 0: Data clock output disabled 1: Data clock output enabled; regular strength driver
		0	DCODBL	Controls the use of DCLKIO pad for data clock output 0: DCOBL data clock output disabled 1: DCOBL data clock output enabled; paralleled with DCOSGL for 2× drive current
I DAC Gain	0x03	5:0	I DACGAIN[5:0]	DAC I fine gain adjustment; alters the full-scale current as shown in Figure 86
IRSET	0x04	7	IRSETEN	1: Enables the on-chip R_{SET} value to be changed
		5:0	IRSET[5:0]	Changes the value of the on-chip R_{SET} resistor; this scales the full-scale current of the DAC in ~0.25 dB steps (nonlinear); see Figure 85 000000: R_{SET} = 8 kΩ 100000: R_{SET} = 16 kΩ 111111: R_{SET} = 32 kΩ

Register	Address	Bit	Name	Function
IRCML	0x05	7	IRCMLEN	1: Enables on-chip R_{CML} adjustment
		5:0	IRCML[5:0]	Changes the value of the on-chip R_{CML} resistor; this adjusts the common-mode level of the DAC output stage 000000: R_{SET} = 250 Ω 100000: R_{SET} = 625 Ω 111111: R_{SET} = 1 kΩ
Q DAC Gain	0x06	5:0	Q DACGAIN[5:0]	DAC Q fine gain adjustment; alters the full-scale current as shown in Figure 86
QRSET	0x07	7	QRSETEN	1: Enables on-chip R_{CML} adjustment
		5:0	QRSET[5:0]	Changes the value of the on-chip R_{SET} resistor; this scales the full-scale current of the DAC in ~0.25 dB steps (nonlinear), see Figure 85 000000: R_{SET} = 8 kΩ 100000: R_{SET} = 16 kΩ 111111: R_{SET} = 32 kΩ
QRCML	0x08	7	QRCMLEN	1: Enables on-chip R_{CML} adjustment
		5:0	QRCML[5:0]	Changes the value of the on-chip R_{CML} resistor; this adjusts the common-mode level of the DAC output stage 000000, R_{SET} = 250 Ω 100000, R_{SET} = 625 Ω 111111, R_{SET} = 1 kΩ
AUXDAC Q	0x09	7:0	QAUXDAC[7:0]	AUXDAC Q output voltage adjustment word LSBs 0x3FF: Sets AUXDAC Q output to full scale 0x200: Sets AUXDAC Q output to midscale 0x000: Sets AUXDAC Q output to bottom of scale
AUX CTLQ	0x0A	7	QAUXEN	1: enables AUXDAC Q
		6:5	QAUXRNG[1:0]	00: Sets AUXDAC Q output voltage range to 2 V 01: Sets AUXDAC Q output voltage range to 1.5 V 10: Sets AUXDAC Q output voltage range to 1.0 V 11: Sets AUXDAC Q output voltage range to 0.5 V
		4:2	QAUXOFS[2:0]	000: Sets AUXDAC Q top of range to 1.0 V 001: Sets AUXDAC Q top of range to 1.5 V 010: Sets AUXDAC Q top of range to 2.0 V 011: Sets AUXDAC Q top of range to 2.5 V 100: Sets AUXDAC Q top of range to 2.9 V
		1:0	QAUXDAC[9:8]	AUXDAC Q output voltage adjustment word MSBs
AUXDAC I	0x0B	7:0	IAUXDAC[7:0]	AUXDAC I output voltage adjustment word LSBs 0x3FF: Sets AUXDAC I output to full scale 0x200: Sets AUXDAC I output to midscale 0x000: Sets AUXDAC I output to bottom of scale
AUX CTLI	0x0C	7	IAUXEN	1: enables AUXDAC I
		6:5	IAUXRNG[1:0]	00: Sets AUXDAC I output voltage range to 2 V 01: Sets AUXDAC I output voltage range to 1.5 V 10: Sets AUXDAC I output voltage range to 1.0 V 11: Sets AUXDAC I output voltage range to 0.5 V
		4:2	IAUXOFS[2:0]	000: Sets AUXDAC I top of range to 1.0 V 001: Sets AUXDAC I top of range to 1.5 V 010: Sets AUXDAC I top of range to 2.0 V 011: Sets AUXDAC I top of range to 2.5 V 100: Sets AUXDAC I top of range to 2.9 V
		1:0	IAUXDAC[9:8]	AUXDAC I output voltage adjustment word MSBs
Reference Resistor	0x0D	5:0	RREF[5:0]	Permits an adjustment of the on-chip reference voltage and output at REFIO (see Figure 84) 000000: Sets the value of R_{REF} to 8 kΩ, V_{REF} = 0.8 V 100000: Sets the value of R_{REF} to 10 kΩ, V_{REF} = 1.0 V 111111: Sets the value of R_{REF} to 12 kΩ, V_{REF} = 1.2 V

Register	Address	Bit	Name	Function
Cal Control	0x0E	7	PRELDQ	0: Preload Q DAC calibration reference set to 32 1: Preload Q DAC calibration reference set by user (Cal Address 1)
		6	PRELDI	0: Preload I DAC calibration reference set to 32 1: Preload I DAC calibration reference set by user (Cal Address 1)
		5	CALSELQ	1: Select Q DAC self-calibration
		4	CALSELI	1: Select I DAC self-calibration
		3	CALCLK	1: Calibration clock enabled
		2:0	DIVSEL[2:0]	Calibration clock divide ratio from DAC clock rate 000 = divide by 256; 001 = divide by 128 … 110 = divide by 4; 111 = divide by 2
Cal Memory	0x0F	7	CALSTATQ	1: Calibration of Q DAC complete
		6	CALSTATI	1: Calibration of I DAC complete
		3:2	CALMEMQ[1:0]	Status of Q DAC calibration memory 00: Uncalibrated 01: Self-calibrated 10: User calibrated
		1:0	CALMEMI[1:0]	Status of I DAC calibration memory 00: Uncalibrated 01: Self-calibrated 10: User calibrated
Memory Address	0x10	5:0	MEMADDR[5:0]	Address of static memory to be accessed
Memory Data	0x11	5:0	MEMDATA[5:0]	Data for static memory access
Memory R/W	0x12	7	CALRSTQ	1: Clear CALSTATQ
		6	CALRSTI	1: Clear CALSTATI
		4	CALEN	1: Initiate device self-calibration
		3	SMEMWR	1: Write to static memory (calibration coefficients)
		2	SMEMRD	1: Read from static memory (calibration coefficients)
		1	UNCALQ	1: Reset Q DAC calibration coefficients to default (uncalibrated)
		0	UNCALI	1: Reset I DAC calibration coefficients to default (uncalibrated)
CLKMODE	0x14	7:6	CLKMODEQ[1:0]	Q datapath retimer clock select output (that is, readback after Q retimer acquires)
		4	SEARCHING	High indicates internal data path retimer is searching for clock relationship (device output is not usable while this bit is high)
		3	REACQUIRE	Edge triggered, 0 to 1 causes the retimer to reacquire the clock relationship
		2	CLKMODEN	0: CLKMODEI/Q values computed by the two retimers and read back in CLKMODEI[1:0] and CLKMODEQ[1:0] 1: CLKMODE values set in CLKMODEI[1:0] over-ride both I and Q retimers
		1:0	CLKMODEI[1:0]	0: CLKMODEN, read only; clock phase chosen by retimer 1: CLKMODEN, read/write; value in this register sets I and Q clock phases
Version	0x1F	7:0	VERSION[7:0]	Hardware version of the device

DIGITAL INTERFACE OPERATION

Digital data for the I and Q DACs is supplied over a single parallel bus (DB[MSB:0]) accompanied by a qualifying clock (DCLKIO). The I and Q data is provided to the chip in an interleaved double data rate (DDR) format. The maximum guaranteed data rate is 250 MSPS with a 125 MHz clock. The order of data pairing and the sampling edge selection is user programmable using the IFIRST and IRISING configuration bits, resulting in four possible timing diagrams. These are shown in Figure 77, Figure 78, Figure 79, and Figure 80.

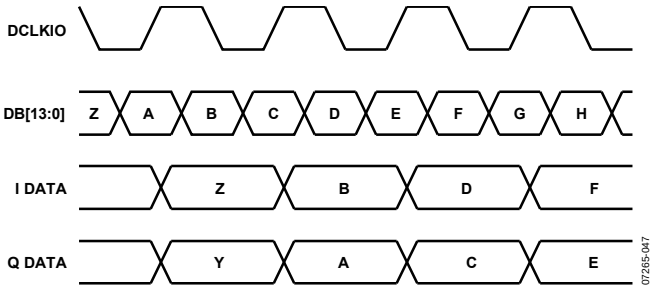

Figure 77. Timing Diagram with IFIRST = 0, IRISING = 0

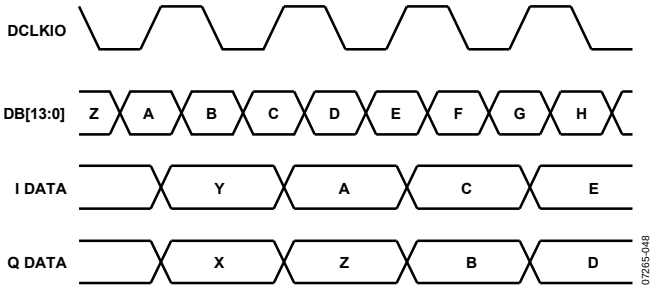

Figure 78. Timing Diagram with IFIRST = 0, IRISING = 1

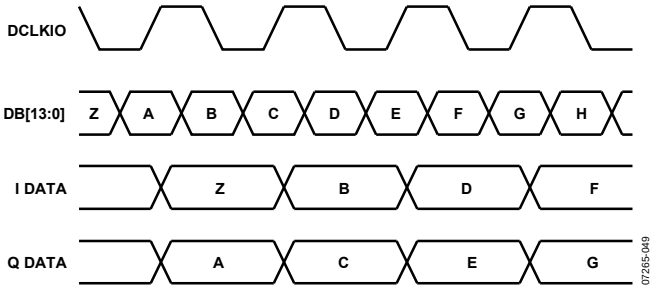

Figure 79. Timing Diagram with IFIRST = 1, IRISING = 0

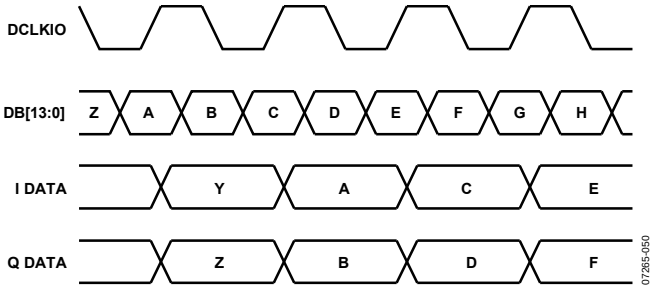

Figure 80. Timing Diagram with IFIRST = 1, IRISING = 1

Ideally, the rising and falling edges of the clock fall in the center of the keep-in-window formed by the set-up and hold times, t_S and t_H. A detailed timing diagram is shown in Figure 81.

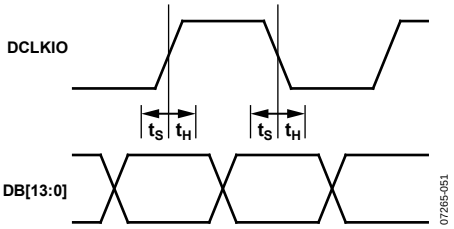

Figure 81. Set-Up and Hold Times for All Input Modes

In addition to the different timing modes listed in Table 2, the input data can also be presented to the device in either unsigned binary or twos complement format. The format type is chosen via the TWOS configuration bit.

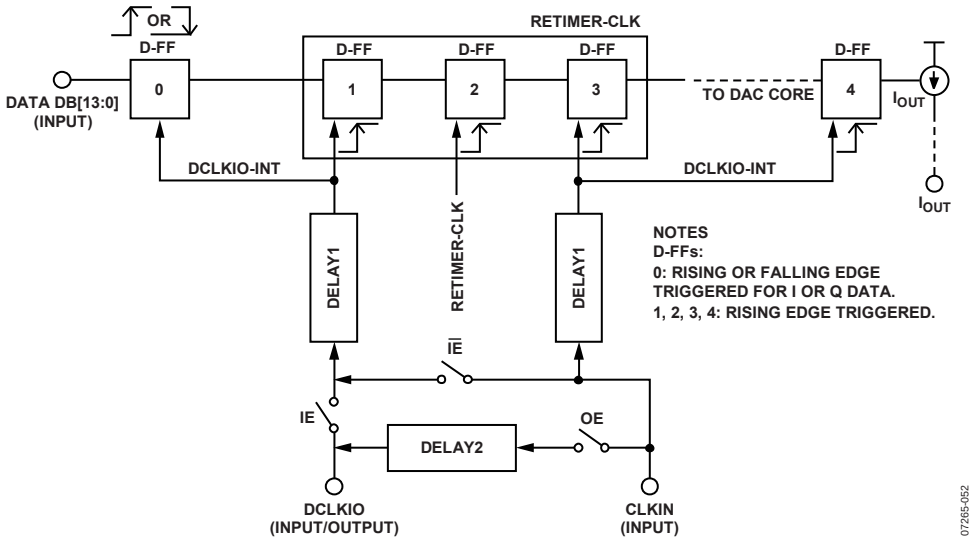

Figure 82. Simplified Diagram of AD9714/AD9715/AD9716/AD9717 Timing

DIGITAL DATA LATCHING AND RETIMER SECTION

The AD9714/AD9715/AD9716/AD9717 have two clock inputs, DCLKIO and CLKIN. The CLKIN is the analog clock whose jitter affects DAC performance and the DCLKIO is a digital clock, probably from an FPGA that needs to have a fixed relationship with the input data to ensure that the data is picked up correctly by the flip-flops on the pads.

Figure 82 is a simplified diagram of the entire data capture system in the AD9714/AD9715/AD9716/AD9717. The double data rate input data, DB[13:0], is latched at the pads/pins either on the rising edge or the falling edge of the DCLKIO-INT clock, as determined by IRISING, the SPI bit. IFIRST, the SPI bit determines which channel data is latched first (that is, I or Q). The captured data is then retimed to the internal clock (CLKIN-INT) in the retimer block before being sent to the final analog DAC core (D-FF (4)), which controls the current steering output switches. All delay blocks depicted in Figure 82 are noninverting, and any wires without an explicit delay block can be assumed to have no delay for the purpose of understanding.

Only one channel is shown in Figure 82 with the data pads (DB[13:0]) serving as double data rate pads for both channels.

The default PINMD and SPI settings are IE = high (closed) and OE = low (open). These settings are enabled when RESET/PINMD (Pin 35) is held high. In this mode, the user has to supply both DCLKIO and CLKIN. In PINMD, it is also recommended that the DCLKIO and the CLKIN be in-phase for proper functioning of the DAC, which can easily be ensured by tying the pins together on the PCB. If the user can access the SPI, settling IE low (that is, $\overline{IE}$ is high) causes the CLKIN to be used as the DCLKIO also.

Settling OE high in the SPI allows the user to get a DCLKIO output from the CLKIN input for use in the user's PCB system. It is strongly recommended that IE = OE = high not be used even though the device may appear to function correctly.

Retimer

The AD9714/AD9715/AD9716/AD9717 have an internal data retimer circuit that compares the CLKIN-INT and DCLKIO-INT clocks and, depending on their phase relationship, selects a retimer clock (RETIMER-CLK) to safely transfer data from the DCLKIO used at the chip's input interface to the CLKIN used to clock the analog DAC cores (D-FF (4)).

The retimer selects one of the three phases shown in Figure 83. The retimer is controlled by the SPI bits is shown in Table 15.

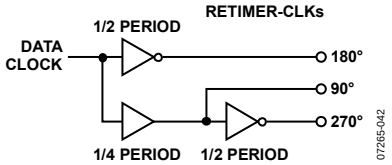

Figure 83. RETIMER-CLK Phases

Note that in most cases, more than one retimer phase works, and in such cases, the retimer arbitrarily picks one phase that works. The retimer cannot pick the best or safest phase. If the user has a working knowledge of the exact phase relationship between DCLKIO and CLKIN (and thus DCLKIO-INT and CLKIN-INT, because the delay is approximately the same for both clocks and equal to DELAY1), then the retimer can be forced to this phase with CLKMODEN = 1 as described in Table 15 and the following paragraphs.

Table 15. Timer Register List

Bit Name	Description
CLKMODEQ[1:0]	Q datapath retimer clock selected output. Valid after SEARCHING goes low.
Searching	High indicates the internal data path retimer is searching for clock relationship (DAC is not usable until it is low again).
Reacquire	Changing this bit from 0 to 1 causes the data path retimer circuit to reacquire the clock relationship.
CLKMODEN	0: Uses CLKMODEI/CLKMODEQ values (as computed by the two internal retimers) for I and Q clocking. 1: Uses CLKMODE value set in CLKMODEI[1:0] for both I and Q retimers (that is, force the retimer).
CLKMODEI[1:0]	I datapath retimer clock selected output. Valid after searching goes low. If CLKMODEN = 1, a value written to this register overrides both I and Q automatic retimer values.

Table 16. CLKMODE Details

CLKMODEI[1:0]/CLKMODEQ[1:0]	DCLKIO-to-CLKIN Phase Relationship	RETIMER-CLK Selected
00	0° to 90°	Phase 2
01	90° to 180°	Phase 3
10	180° to 270°	Phase 3
11	270° to 360°	Phase 1

When reset is pulsed high and then returns low (the part is in SPI mode), the retimer runs and automatically selects a suitable clock phase for the RETIMER-CLK within 128 clock cycles. The SPI searching bit returns to low, indicating that the retimer has locked and the part is ready for use. The reacquire bit can be used to reinitiate phase detection in the I and Q retimers at any time. CLKMODEQ[1:0] and CLKMODEI[1:0] provide readback for the values picked by the internal phase detectors in the retimer (see Table 16).

To force the two retimers (I and Q) to pick a particular phase for the retimer clock (they must both be forced to the same value), CLKMODEN should be set high and the required phase value is written into CLKMODEI[1:0] and CLKMODEQ[1:0]. For example, if the DCLKIO and the CLKIN are in phase to first order, the user could safely force the retimers to pick Phase 2 for the RETIMER-CLK. This forcing function may be useful for synchronizing multiple devices.

In pin mode, it is expected that the user tie CLKIN and DCLKIO together. The device has a small amount of programmable functionality using the now unused SPI pins (SCLK, SDIO, and $\overline{CS}$). If the two chip clocks are tied together, the SCLK pin can be tied to ground and the chip uses a clock for the retimer that is 180° out of phase with the two input clocks (that is, Phase 2, which is the safest or best option). The chip has an additional option in pin mode when the redefined SCLK pin is high. Use this mode if utilizing pin mode, but CLKIN and DCLKIO are not tied together (that is, not in phase). Holding SCLK high causes the internal clock detector to use the phase detector output to determine which clock to use in the retimer (that is, select a suitable RETIMER-CLK phase). The action of taking SCLK high causes the internal phase detector to reexamine the two clocks and determine the relative phase. Whenever the user wants to reevaluate the relative phase of the two clocks, the SCLK pin can be taken low and then high again.

ESTIMATING THE OVERALL DAC PIPELINE DELAY

DAC pipeline latency is affected by the phase of the RETIMER-CLK that is selected. If latency is critical to the system and needs to be constant, the retimer should be forced to a particular phase and not be allowed to automatically select a phase each time.

Consider the case when DCLKIO = CLKIN (that is, in phase), and the RETIMER-CLK is forced to Phase 2. Assume that IRISING is 1 (that is, I data is latched on the rising edge and Q data on the falling edge). Then the latency to the output for the I-channel is 3 clock cycles (D-FF (1), D-FF (3), and D-FF (4), but not D-FF (2) because it is latched on the half clock cycle or 180°). The latency to the output for the Q-channel

from the time the falling edge latches it at the pads in D-FF (0) is 2.5 clock cycles (½ clock cycle to D-FF (1), 1 clock cycle to D-FF (3), and 1 clock cycle to D-FF (4)). This latency for the AD9714/AD9715/ AD9716/AD9717 is case specific and needs to be calculated based on the RETIMER-CLK phase that is automatically selected or manually forced.

SELF-CALIBRATION

The AD9714/AD9715/AD9716/AD9717 have a self-calibration feature that improves the DNL of the device. Performing a self-calibration on the device improves device performance in low frequency applications. The device performance in applications where the analog output frequencies are above 5 MHz are generally influenced more by dynamic device behavior than by DNL, and in these cases, self-calibration is unlikely to provide much benefit. The calibration clock frequency is equal to the DAC clock divided by the division factor chosen by the DIVSEL value. Each calibration clock cycle is between 32 and 2048 DAC input clock cycles, depending on the value of DIVSEL[2:0] (Register 0x0E, Bits[2:0]). The frequency of the calibration clock should be between 0.5 MHz and 4 MHz for reliable calibrations. Best results are obtained by setting DIVSEL[2:0] (Register 0x0E, Bits[2:0]) to produce a calibration clock frequency between these values. Separate self-calibration hardware is included for each DAC. The DACs can be self-calibrated individually or simultaneously.

To perform a device self-calibration, the following procedure can be used:

1. Write 0x00 to Register 0x12. This ensures that the UNCALI and UNCALQ bits are reset.
2. Set up a calibration clock between 0.5 MHz and 4 MHz using DIVSEL[2:0] and then enable the calibration clock by setting the CALCLK bit (Register 0x0E, Bit 3).
3. Select the DAC(s) to self-calibrate by setting either Bit 4 (CALSELI) for the I DAC and/or Bit 5 (CALSELQ) for the Q DAC in Register 0x0E. Note that each DAC contains independent calibration hardware so they can be calibrated simultaneously.
4. Start self-calibration by setting Bit 4 in Register 0x12. Wait approximately 300 calibration clock cycles.
5. Check if the self-calibration has completed by reading the CALSTATI bit (Bit 6) and CALSTATQ bit (Bit 7) in Register 0x0F. Logic 1 indicates the calibration has completed.
6. When the self-calibration has completed, write 0x00 to Register 0x12.
7. Disable the calibration clock by clearing the CALCLK bit (Register 0x0E, Bit 3).

The AD9714/AD9715/AD9716/AD9717 allow reading and writing of the calibration coefficients. There are 32 coefficients in total. The read/write feature of the coefficients can be useful for improving the results of the self-calibration routine by averaging the results of several self-calibration cycles and loading the averaged results back into the device.

To read the calibration coefficients, use the following steps:

1. Select which DAC core to read by setting either Bit 4 (CALSELI) for the I DAC or Bit 5 (CALSELQ) for the Q DAC in Register 0x0E. Write the address of the first coefficient (0x01) to Register 0x10.
2. Set the SMEMRD bit (Register 0x12, Bit 2) by writing 0x04 to Register 0x12.
3. Read the 6-bit value of the first coefficient by reading the contents of Register 0x11.
4. Clear the SMEMRD bit by writing 0x00 to Register 0x12.
5. Repeat Step 2 through Step 4 for each of the remaining 31 coefficients by incrementing the address by one for each read.
6. Deselect the DAC core by clearing either Bit 4 (CALSELI) for the I DAC or Bit 5 (CALSELQ) for the Q DAC in Register 0x0E.

To write the calibration coefficients to the device, use the following steps:

1. Select which DAC core to write by setting either Bit 4 (CALSELI) for the I DAC or Bit 5 (CALSELQ) for the Q DAC in Register 0x0E.
2. Set the SMEMWR bit (Register 0x12, Bit 3) by writing 0x08 to Register 0x12.
3. Write the address of the first coefficient (0x01) to Register 0x10.
4. Write the value of the first coefficient to Register 0x11.
5. Repeat Step 2 through Step 4 for each of the remaining 31 coefficients by incrementing the address by one for each write.
6. Clear the SMEMWR bit by writing 0x00 to Register 0x12.
7. Deselect the DAC core by clearing either Bit 4 (CALSELI) for the I DAC or Bit 5 (CALSELQ) for the Q DAC in Register 0x0E.

COARSE GAIN ADJUSTMENT

Option 1

A coarse full-scale output current adjustment can be achieved using the lower six bits in Register 0x0D. This adds or subtracts up to 20% from the band gap voltage on Pin 34 (REFIO), and the voltage on the FSADJx resistors tracks this change. As a result, the DAC full-scale current varies the same amount. A secondary effect to changing the REFIO voltage is that the full-scale voltage in the AUXDAC also changes by the same magnitude. The register uses twos complement format, in which 011111 maximizes the voltage on the REFIO node and 100000 minimizes the voltage.

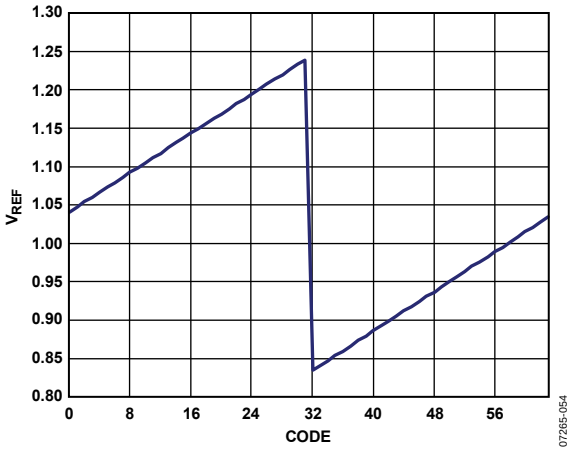

Figure 84. Typical V_{REF} Voltage vs. Code

Option 2

While utilizing the internal FSADJx resistors, each main DAC can achieve independently controlled coarse gain using the lower six bits of Register 0x04 (IRSET[5:0]) and Register 0x07 (QRSET[5:0]). Unlike Coarse Gain Option 1, this impacts only the main DAC full-scale output current. The register uses twos complement format and allows the output current to be changed in approximately 0.25 dB steps.

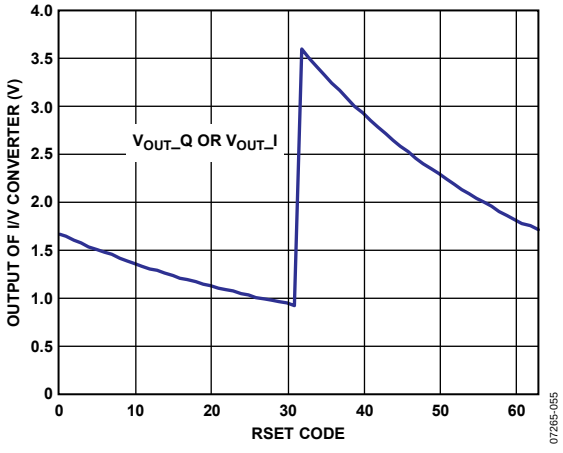

Figure 85. Effect of R_{SET} Code

Option 3

Even when the device is in pin mode, full-scale values can be adjusted by sourcing or sinking current from the FSADJ pins. Any noise injected here appears as amplitude modulation of the output. Thus, a portion of the required series resistance (at least 20 kΩ) must be installed right at the pin. A range of ±10% is quite practical using this method.

Option 4

As in Option 3, when the device is in pin mode both full-scale values can be adjusted by sourcing or sinking current from the REFIO pin. Noise injected here appears as amplitude modulation of the output, so a portion of the required series resistance (at least 10 kΩ) must be installed at the pin. A range of ±25% is quite practical when using this method.

Fine Gain

Each main DAC has independent fine gain control using the lower six bits in Register 0x03 (I DAC gain) and Register 0x06 (Q DAC gain). Unlike Coarse Gain Option 1, this impacts only the main DAC full-scale output current. This register uses straight binary format. One application where this straight binary format is critical is for side-band suppression while using a quadrature modulator. This is described in more detail in the Applications Information section.

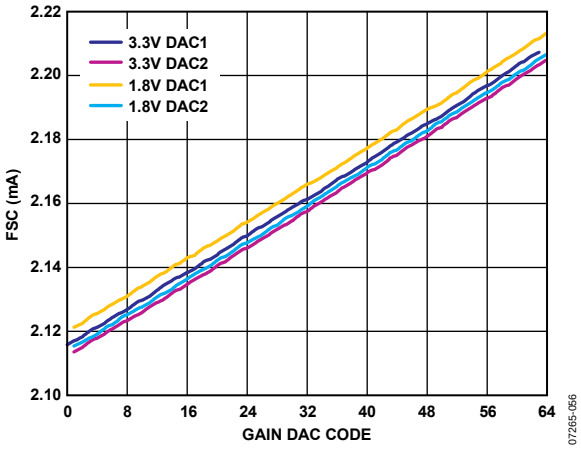

Figure 86. Typical DAC Gain Characteristics

USING THE INTERNAL TERMINATION RESISTORS

The AD9717/AD9716/AD9715/AD9714 have four 500 Ω termination internal resistors (two for each DAC output). To use these resistors to convert the DAC output current to a voltage, connect each DAC output pin to the adjacent load pin. For example, on the I DAC, IOUTP must be shorted to RLIP and IOUTN must be shorted to RLIN. In addition, the CMLI or CMLQ pin must be connected to ground directly or through a resistor. If the output current is at the nominal 2 mA and the CMLI or CMLQ pin is tied directly to ground, this produces a dc common-mode bias voltage on the DAC output equal to 0.5 V. If the DAC dc bias needs to be higher than 0.5 V, an external resistor can be connected between the CMLI or CMLQ pin and ground. This part also has an internal common-mode resistor that can be enabled. This is explained in the Using the Internal Common-Mode Resistor section.

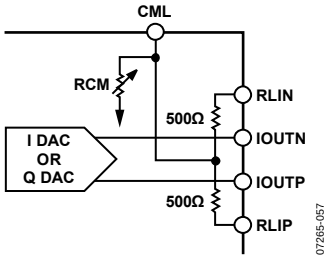

Figure 87. Simplified Internal Load Options

Using the Internal Common-Mode Resistor

These devices contain an adjustable internal common-mode resistor that can be used to increase the dc bias of the DAC outputs. By default, the common-mode resistor is not connected. When enabled, it can be adjusted from ~250 Ω to ~1 kΩ. Each main DAC has an independent adjustment using the lower six bits in Register 0x05 (IRCML[5:0]) and Register 0x08 (QRCML[5:0]).

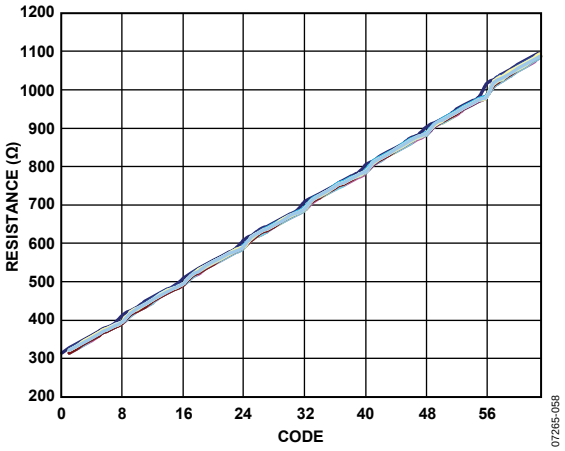

Figure 88. Typical CML Resistor Value vs. Register Code

Using the CMLx Pins for Optimal Performance

The CMLx pins also serve to change the DAC bias voltages in the parts allowing them to run at higher dc output bias voltages. When running the bias voltage below 0.9 V and an AVDD of 3.3 V, the parts perform optimally when the CMLx pins are tied to ground. When the dc bias increases above 0.9 V, set the CMLx pins at 0.5 V for optimal performance. The maximum dc bias on the DAC output should be kept at or below 1.2 V when the supply is 3.3 V. When the supply is 1.8 V, keep the dc bias close to 0 V and connect the CMLx pins directly to ground.

APPLICATIONS INFORMATION

OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD9714/AD9715/AD9716/AD9717. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 2 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration can consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application that allows ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, signal gain, and/or a low output impedance.

A single-ended output is suitable for applications where low cost and low power consumption are primary concerns.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion, as shown in Figure 89. The distortion performance of a transformer typically exceeds that available from standard op amps, particularly at higher frequencies. Transformer coupling provides excellent rejection of common-mode distortion (that is, even-order harmonics) over a wide frequency range. It also provides electrical isolation and can deliver voltage gain without adding noise. Transformers with different impedance ratios can also be used for impedance matching purposes. The main disadvantages of transformer coupling are low frequency roll-off, lack-of-power gain, and high output impedance.

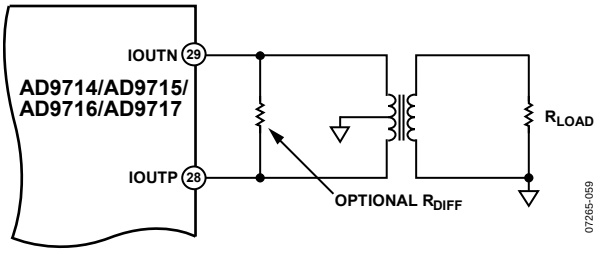

Figure 89. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to a voltage that keeps the voltages on IOUTP and IOUTN within the output common-mode voltage range of the device. Note that the dc component of the DAC output current is equal to I_{OUTFS} and flows out of both IOUTP and IOUTN. The center tap of the transformer should provide a path for this dc current. In most applications, AGND provides the most convenient voltage for the transformer center tap. The complementary voltages appearing at IOUTP and IOUTN (that is, V_{IOUTP} and V_{IOUTN}) swing symmetrically around AGND and should be maintained with the specified output compliance range of the AD9714/AD9715/AD9716/AD9717.

A differential resistor, R_{DIFF}, can be inserted in applications where the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF}, as reflected by the transformer, is chosen to provide a source termination that results in a low VSWR. Note that approximately half the signal power is dissipated across R_{DIFF}.

SINGLE-ENDED BUFFERED OUTPUT USING AN OP AMP

An op amp such as the ADA4899-1 can be used to perform a single-ended current-to-voltage conversion, as shown in Figure 90. The AD9714/AD9715/AD9716/AD9717 are configured with a pair of series resistors, R_S, off each output. For best distortion performance, R_S should be set to 0 Ω. The feedback resistor, R_{FB}, determines the peak-to-peak signal swing by the formula

$$V_{OUT} = R_{FB} \times I_{FS}$$

The common-mode voltage of the output is determined by the formula

$$V_{CM} = V_{REF} \times \left(1 + \frac{R_{FB}}{R_B}\right) - \frac{R_{FB} \times I_{FS}}{2}$$

The maximum and minimum voltages out of the amplifier are, respectively,

$$V_{MAX} = V_{REF} \times \left(1 + \frac{R_{FB}}{R_B}\right)$$

$$V_{MIN} = V_{MAX} - I_{FS} \times R_{FB}$$

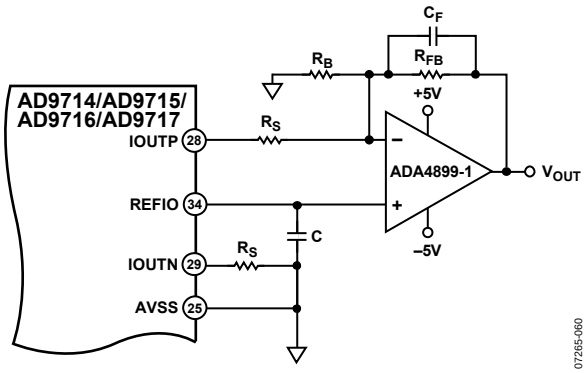

Figure 90. Single-Supply Single-Ended Buffer

DIFFERENTIAL BUFFERED OUTPUT USING AN OP AMP

A dual op amp (see the circuit shown in Figure 91) can be used in a differential version of the single-ended buffer shown in Figure 90. The same R-C network is used to form a one-pole differential, low-pass filter to isolate the op amp inputs from the high frequency images produced by the DAC outputs. The feedback resistors, R_{FB}, determine the differential peak-to-peak signal swing by the formula

$$V_{OUT} = 2 \times R_{FB} \times I_{FS}$$

The maximum and minimum single-ended voltages out of the amplifier are, respectively,

$$V_{MAX} = V_{REF} \times \left(1 + \frac{R_{FB}}{R_B}\right)$$

$$V_{MIN} = V_{MAX} - R_{FB} \times I_{FS}$$

The common-mode voltage of the differential output is determined by the formula

$$V_{CM} = V_{MAX} - R_{FB} \times I_{FS}$$

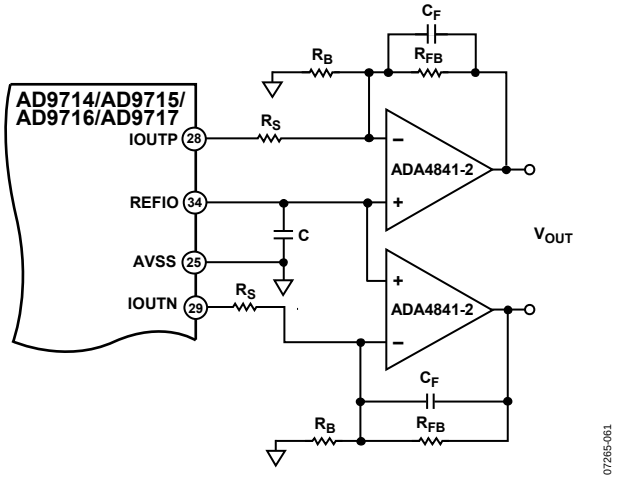

Figure 91. Single-Supply Differential Buffer

AUXILIARY DACs

The DACs of the AD9714/AD9715/AD9716/AD9717 feature two versatile and independent 10-bit auxiliary DACs suitable for dc offset correction and similar tasks.

Because the AUXDACs are driven through the SPI port, they should never be used in timing-critical applications, such as inside analog feedback loops.

To keep the pin count reasonable, these auxiliary DACs each share a pin with the corresponding FSADJx resistor. They are, therefore, usable only when enabled and when that DAC is operated on its internal full-scale resistors. A simple I-to-V converter is implemented on chip with selectable shunt resistors (3.2 kΩ to 16 kΩ) such that if REFIO is set to exactly 1 V, REFIO/2 equals 0.5 V and the following equation describes the no load output voltage:

$$V_{OUT} = 0.5\ \text{V} - \left(I_{DAC} - \frac{1.5}{R_S}\right)16\ \text{k}\Omega$$

Figure 92 illustrates the function of all the SPI bits controlling these DACs with the exception of the QAUXEN and IAUXEN bits and gating to prohibit R_S < 3.2 kΩ.

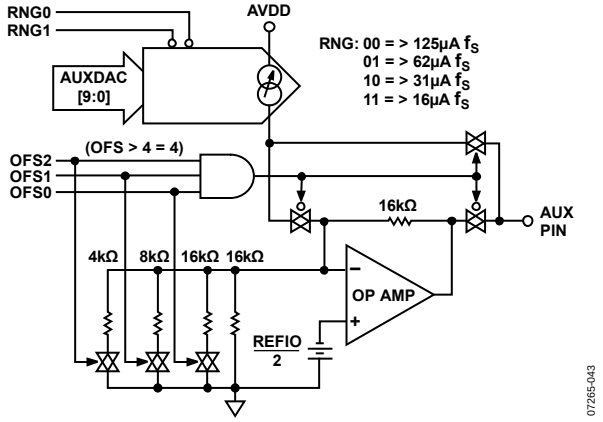

Figure 92. AUXDAC Simplified Circuit Diagram

The SPI speed limits the update rate of the auxiliary DACs. The data is inverted such that I_{AUXDAC} is full scale at 0x000 and zero at 0x1FF, as shown in Figure 93.

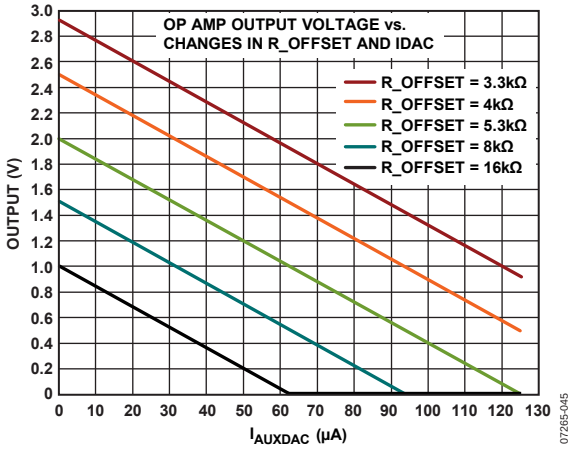

Figure 93. AUXDAC Op Amp Output vs. Current, AVDD = 3.3 V No Load, AUXDAC 0x1FF to 0x000

Two registers are assigned to each DAC with 10 bits for the actual DAC current to be generated, a 3-bit offset (and gain) adjustment, a 2-bit current range adjustment, and an enable/disable bit. Setting the QAUXOFS and IAUXOFS bits to all 1s disables the respective op amp and routes the DAC current directly to their respective FSADJI/ AUXI or FSADJQ/AUXQ pins. This is especially useful where the loads to be driven are beyond the limited capability of the on-chip amplifier. The DAC output will open circuit when not enabled (QAUXEN or IAUXEN = 0).

DAC-TO-MODULATOR INTERFACING

The auxiliary DACs can be used for local oscillator (LO) cancellation when the DAC output is followed by a quadrature modulator. This LO feedthrough is caused by the input referred dc offset voltage of the quadrature modulator (and the DAC output offset voltage mismatch) and can degrade system performance. Typical DAC-to-quadrature modulator interfaces are shown in Figure 94 and Figure 95. Often, the input common-mode voltage for the modulator is much higher than the output compliance range of the DAC, so that ac coupling or a dc level shift is necessary. If the required common-mode input voltage on the quadrature modulator matches that of the DAC, the dc blocking capacitors in Figure 94 can be removed. A low-pass or band-pass passive filter is recommended when spurious signals from the DAC (distortion and DAC images) at the quadrature modulator inputs can affect the system performance. Placing the filter at the location shown in Figure 94 and Figure 95 allows easy design of the filter, because the source and load impedances can easily be designed close to 500 Ω for a 2 mA full-scale output.

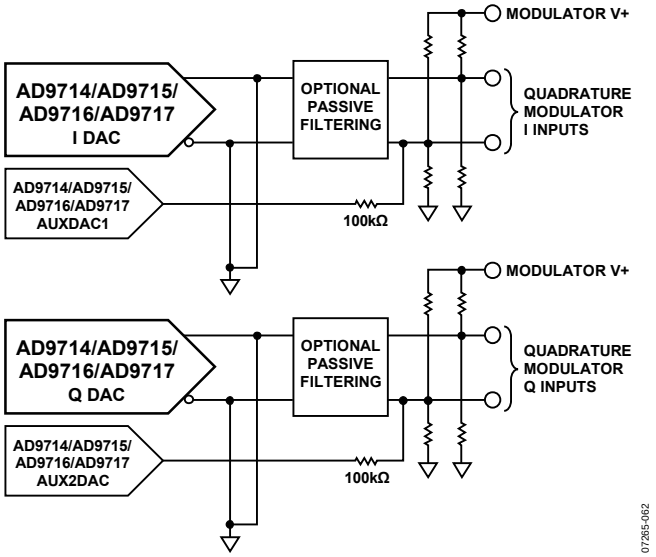

Figure 94. Typical Use of Auxiliary DACs and On-Chip Resistors for Direct Coupling to Quadrature Modulators

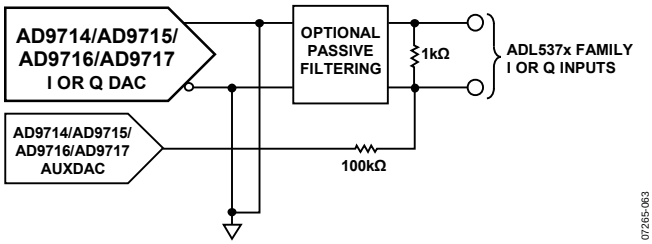

Figure 95. Typical Use of Auxiliary DACs When DC Coupling to Quadrature Modulator ADL537x Family

CORRECTING FOR NONIDEAL PERFORMANCE OF QUADRATURE MODULATORS ON THE IF-TO-RF CONVERSION

Analog quadrature modulators make it very easy to realize single sideband radios. However, there are several nonideal aspects of quadrature modulator performance. Among these analog degradations are gain mismatch and LO feedthrough.

Gain Mismatch

The gain in the real and imaginary signal paths of the quadrature modulator may not be matched perfectly. This leads to less than optimal image rejection because the cancellation of the negative frequency image is less than perfect.

LO Feedthrough

The quadrature modulator has a finite dc referred offset, as well as coupling from its LO port to the signal inputs. These can lead to a significant spectral spur at the frequency of the Quadrature Modulator LO.

The AD9714/AD9715/AD9716/AD9717 have the capability to correct for both of these analog degradations. However, understand that these degradations drift over temperature; therefore, if close to optimal single sideband performance is desired, a scheme for sensing these degradations over temperature and correcting them may be necessary.

I/Q CHANNEL GAIN MATCHING

Fine gain matching is achieved by adjusting the values in the DAC fine gain adjustment registers. For the I DAC, these values are in the I DAC gain register (Register 0x03). For the Q DAC, these values are in the Q DAC gain register (Register 0x06). These are 6-bit values that cover ±2% of full scale. To perform gain compensation starting from the default values of zero, raise the value of one of these registers a few steps until it can be determined if the amplitude of the unwanted image is increased or decreased. If the unwanted image increased in amplitude, remove the step and try the same adjustment on the other DAC control register. Iterate register changes until the rejection cannot be improved further. If the fine gain adjustment range is not sufficient to find a null (that is, the register goes full scale with no null apparent) adjust the course gain settings of the two DACs accordingly and try again. Variations on this simple method are possible.

Note that LO feedthrough compensation is independent of phase compensation. However, gain compensation can affect the LO compensation because the gain compensation may change the common-mode level of the signal. The dc offset of some modulators is common-mode level dependent. Therefore, it is recommended that the gain adjustment be performed prior to LO compensation.

LO FEEDTHROUGH COMPENSATION

To achieve LO feedthrough compensation in a circuit, each output of the two AUXDACs must be connected through a 100 kΩ resistor to one side of the differential DAC output. See the Auxiliary DACs section for details of how to use AUXDACs. The purpose of these connections is to drive a very small amount of current into the nodes at the quadrature modulator inputs, therefore adding a slight dc bias to one or the other of the quadrature modulator signal inputs.

To achieve LO feedthrough compensation, the user should start with the default conditions of the AUXDAC registers, then increment the magnitude of one or the other AUXDAC output voltages. While this is being done, the amplitude of the LO feedthrough at the quadrature modulator output should be sensed. If the LO feedthrough amplitude increases, try either decreasing the output voltage of the AUXDAC being adjusted, or try adjusting the output voltage of the other AUXDAC. It may take practice before an effective algorithm is achieved. Using the AD9714/AD9715/AD9716/AD9717 evaluation board, the LO feedthrough can typically be adjusted down to the noise floor, although this is not stable over temperature.

RESULTS OF GAIN AND OFFSET CORRECTION

The results of gain and offset correction can be seen in Figure 96 and Figure 97. Figure 96 shows the output spectrum of the quadrature demodulator before gain and offset correction. Figure 97 shows the output spectrum after correction. The LO feedthrough spur at 450 MHz has been suppressed to the noise level. This result can be achieved by applying the correction, but the correction needs to be repeated after a large change in temperature.

Note that gain matching improves the negative frequency image rejection, but it is also related to the phase mismatch in the quadrature modulator. It can be improved by adjusting the relative phase between the two quadrature signals at the digital side or properly designing the low-pass filter between the DACs and quadrature modulators. Phase mismatch is frequency dependent, so routines have to be developed to adjust it if wideband signals are desired.

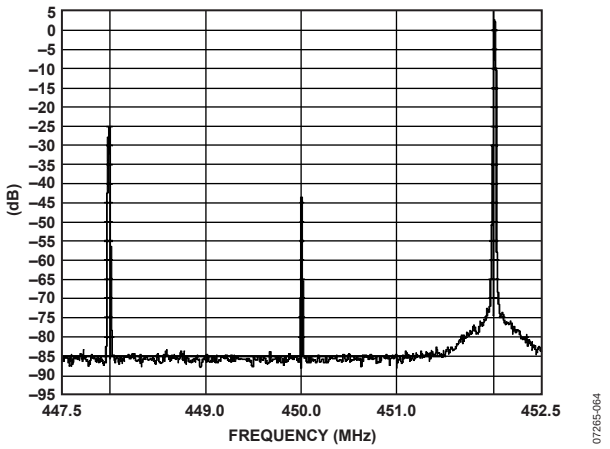

Figure 96. AD9714/AD9715/AD9716/AD9717 and ADL5370 with a Single-Tone Signal at 450 MHz, No Gain or LO Compensation

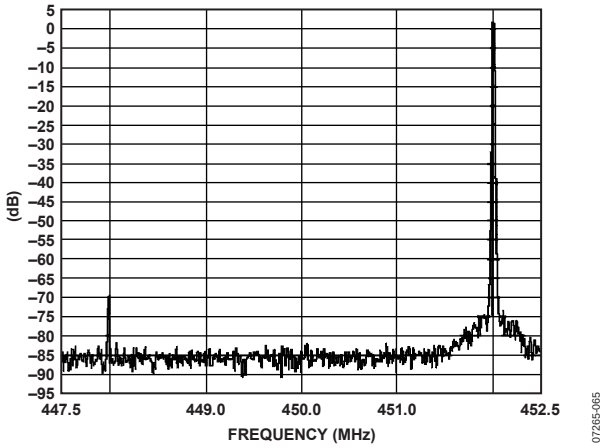

Figure 97. AD9714/AD9715/AD9716/AD9717 and ADL5370 with a Single-Tone Signal at 450 MHz, Gain and LO Compensation Optimized

MODIFYING THE EVALUATION BOARD TO USE THE ADL5370 ON-BOARD QUADRATURE MODULATOR

The evaluation board contains an Analog Devices, Inc., ADL5370 quadrature modulator. The AD9714/AD9715/AD9716/AD9717 and the ADL5370 provide an easy-to-interface DAC/modulator combination that can be easily characterized on the evaluation board. Solderable jumpers can be configured to evaluate the single-ended or differential outputs of the AD9714/ AD9715/AD9716/AD9717. This is the default configuration from the factory and consists of the following population of the components:

- JP55, JP56, JP76, JP82—unsoldered
- R13, R14, R52, R53—unpopulated
- R50, R57, T1, T2—populated

To evaluate the ADL5370 on this board, the population of these same components should be reversed so that they are in the following positions:

- JP55, JP56, JP76, JP82—soldered
- R13, R14, R52, R53—populated
- R50, R57, T1, T2—unpopulated

The AUXDAC outputs can be connected to Test Point TP44 and Test Point TP45 if LO feedthrough compensation is necessary.

OUTLINE DIMENSIONS

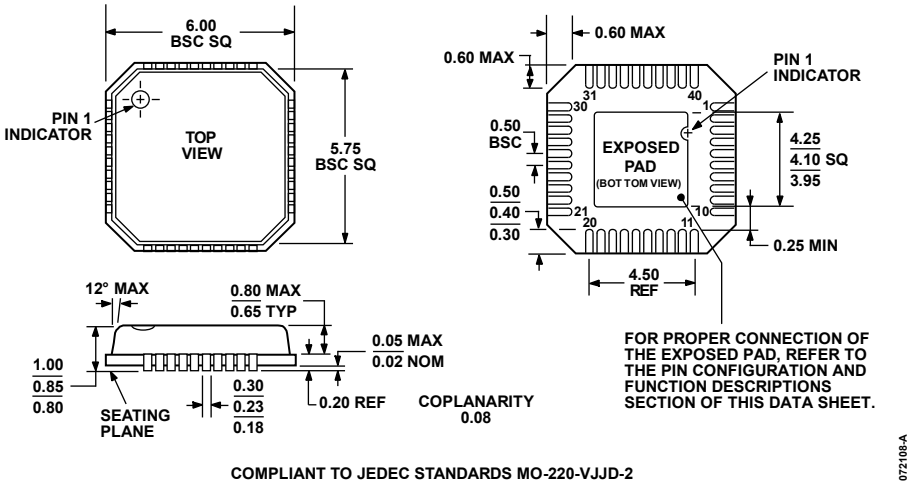

Figure 98. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm, Very Thin Quad
(CP-40-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9714BCPZ[1]	−40°C to +85°C	40-Lead LFCSP_VQ	CP-40-1
AD9714BCPZRL7[1]	−40°C to +85°C	40-Lead LFCSP_VQ	CP-40-1
AD9715BCPZ[1]	−40°C to +85°C	40-Lead LFCSP_VQ	CP-40-1
AD9715BCPZRL7[1]	−40°C to +85°C	40-Lead LFCSP_VQ	CP-40-1
AD9716BCPZ[1]	−40°C to +85°C	40-Lead LFCSP_VQ	CP-40-1
AD9716BCPZRL7[1]	−40°C to +85°C	40-Lead LFCSP_VQ	CP-40-1
AD9717BCPZ[1]	−40°C to +85°C	40-Lead LFCSP_VQ	CP-40-1
AD9717BCPZRL7[1]	−40°C to +85°C	40-Lead LFCSP_VQ	CP-40-1
AD9714-EBZ[1]		Evaluation Board	
AD9715-EBZ[1]		Evaluation Board	
AD9716-EBZ[1]		Evaluation Board	
AD9717-EBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.