Murata Power Solutions

ADC-301, ADC-302
8-Bit Video
Flash A/D Converter

PRODUCT DATA SHEET

OBSOLETE PRODUCT

Contact Factory for Replacement Model

FEATURES

ADC-301

- 8-Bit resolution
- Non-linearity ±½ LSB
- Conversion rate 30 MHz
- 15 MHz bandwidth
- 35 pF input capacitance
- Power dissipation 420 mW

ADC-302

- 8-Bit resolution
- Non-linearity ±½ LSB
- Conversion rate 50 MHz
- 25 MHz bandwidth
- 35 pF input capacitance
- Power dissipation 550 mW

GENERAL DESCRIPTION

These ADC's are video speed 8-bit flashes capable of digitizing analog signals at conversion rates of 30 MHz (ADC-301) and 50 MHz (ADC-302) with a power consumption of 420 mW and 550 mW respectively.

The 256 clocked comparators have the analog voltage applied to one input and a voltage derived from the reference voltage and reference resistors applied to the other comparator input.

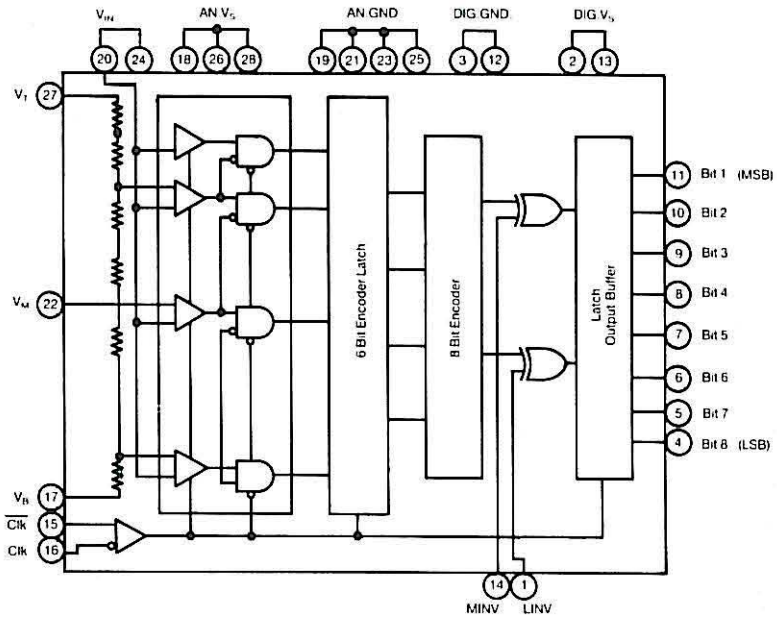
The comparator outputs are 'anded' with adjacent outputs and these outputs latched into a 6-bit encoder. These 6-bit codes are further encoded to 8-bit codes and latched. The final ECL output buffer stage requires external pull down resistors, the output being delayed from the sampling point by the time of one clock cycle.

Output polarity of the MSB and LSB's respectively can be controlled on two digital input lines.

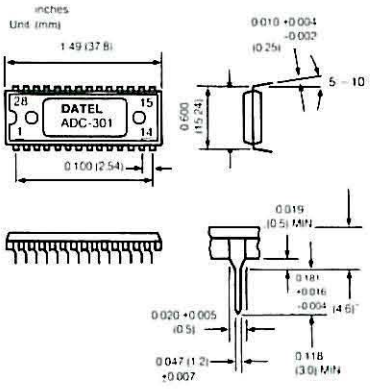
With a reference of -2V the analog input range will be 0 to -2V.

APPLICATIONS

- High speed data acquisition
- Radar pulse analysis
- TV video encoding
- High energy physics
- Transient analysis
- Medical electronics
- Fluid flow analysis
- Sonar systems



MECHANICAL DIMENSIONS



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT POLARITY (LINV)	28	ANALOG Vs (−5.2V)
2	DIGITAL Vs (−5.2V)	27	REFERENCE INPUT Vt (−0V)
3	DIGITAL GROUND	26	ANALOG Vs (−5.2V)
4	BIT 8 (LSB)	25	ANALOG GROUND
5	BIT 7	24	ANALOG INPUT
6	BIT 6	23	ANALOG GROUND
7	BIT 5	22	REFERENCE Vm
8	BIT 4	21	ANALOG GROUND
9	BIT 3	20	ANALOG INPUT
10	BIT 2	19	ANALOG GROUND
11	BIT 1 (MSB)	18	ANALOG Vs (−5.2V)
12	DIGITAL GROUND	17	REFERENCE INPUT Vb (−2V)
13	DIGITAL Vs (−5.2V)	16	CLOCK INPUT
14	OUTPUT POLARITY (MINV)	15	$\overline{\text{CLOCK}}$ INPUT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_S	0 to -7V
Input Voltage (V_{IN})	0.5V to V_S
Reference Voltage V_t, V_b, V_m	0.5V to V_S
Reference Voltage ($V_b - V_t$)	-2.5V
Digital Inputs	0.5V to -4V
Vm Input Current	-3 mA to +3 mA
Digital Outputs	0 to -10 mA
Operating Temperature	-20°C to +100°C
Storage Temperature	-55°C to +150°C
Allowable Power Dissipation	1.48 W

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, V_S = -5.2V dc, V_B = -2.0V unless otherwise stated.

PERFORMANCE	ADC-301	ADC-302
Resolution	8 Bits	8 Bits
Conversion Rate (Min)	30 MHz	50 MHz
Non-Linearity (Max)	+½ LSB	+½ LSB
Diff. Non-Linearity (Max)	+½ LSB	+½ LSB
Diff. Gain (Max)	1.5%	1.5%
Diff. Phase (Max)	0.5 Deg.	0.5 Deg.
Aperture Jitter (Typ)	45 psec.	30 psec.
Input Bandwidth (Typ)	15 MHz	25 MHz
Power Dissipation (Typ)	420 mW	550 mW

INPUTS	MIN.	TYP.	MAX.	UNITS
Reference Input Voltage	-1.8	-2.0	-2.2	V
Reference Resistance	70	80	100	Ohms
Analog Input Voltage	0.1	—	-2.2	V
Analog Input Capacitance	—	35	40	pF
Analog Input Bias Current				
(ADC-301)	—	60	90	µA
(ADC-302)	—	75	115	µA
Offset Voltage V_t	7	9	11	mV
V_b	15	17	19	mV
Digital Input Voltage				
V_h	-0.7	-0.9	-1.0	V
V_l	-1.6	-1.75	-1.9	V
Digital Input Current				
(V_h = -0.9V)	0	—	0.4	mA
(V_l = -1.75V)	-0.05	—	0.35	mA
OUTPUTS				
Digital Output Voltage				
V_h (R_L = 620 Ω)	-1.0	—	—	V
V_l (R_L = 620 Ω)	—	—	-1.6	V
Output Data Delay (R_L = 620 Ω)	—	4.0	5.0	nsec.
POWER				
Supply Voltage, V_S	-5.0	-5.2	-5.7	V
Supply Current				
(ADC-301)	—	-75	-100	mA
(ADC-302)	—	-95	-120	mA

TECHNICAL NOTES

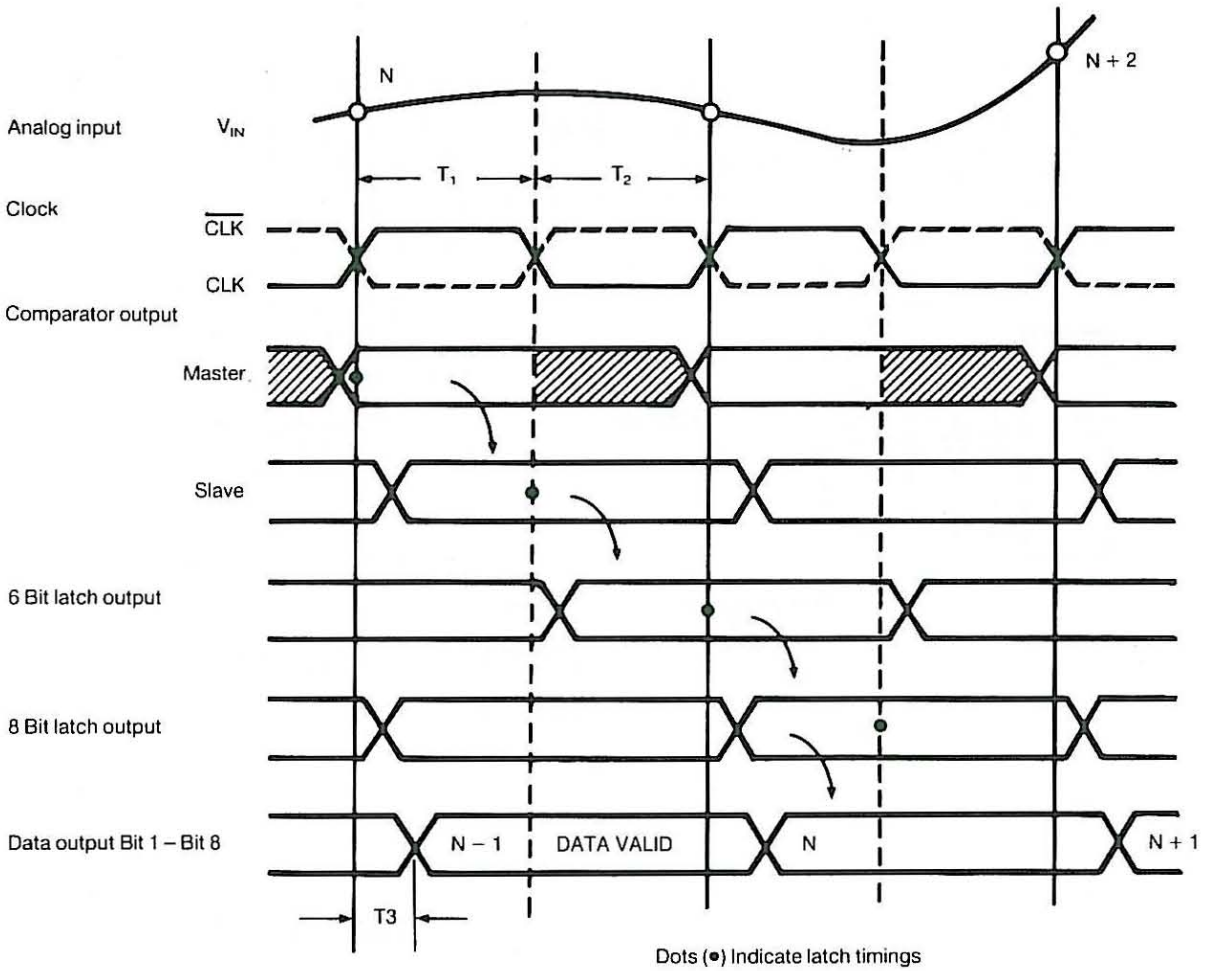
1. Even with the input capacitance down to 35 pF, or less, the converter still requires an input amplifier with good drive capability. The amplifier will require wide bandwidth and a high slew rate (250V/ µS typical) to take full advantage of the input bandwidth of the converter.
2. The input impedance of the A/D's are capacitive which may result in the input amplifier becoming unstable and cause oscillations. A resistor with a value between 2 and 10 Ohms between the amplifier and the input to the converter will stop any oscillations.
3. Clock and Clock (ECL) are usually differentially supplied to pins 16 and 15.
4. The polarity of the output data is controlled by two polarity inversion inputs, MINV (pin 14) which controls the MSB alone and LINV (pin 1) which controls Bit 2 to Bit 8 (LSB). The combination of '0's and '1' on these inputs offer the user various code options. Detailed coding is shown in Table 1. Logic level '0' is obtained by leaving inputs open, logic level '1' is obtained by connecting a 3.9K Ohm resistor to digital ground.
5. The digital outputs Bits 1 to 8 require pull down resistors, in the range 500 to 1000 Ohms, connected to the negative supply rail to prevent waveform distortions by reflection.
6. The reference voltage range (-2.0V to 0V typical) determines the dynamic range of the input voltage.

   Adjustments to this range can be made within the range V_B = 2V ± 0.2V and V_T = 0V ±0.1V. The reference input V_B (pin 17) should be decoupled to analog ground using 1 µF and 0.01 µF capacitors. Improvement in the high frequency stability can be achieved by decoupling terminal V_M (pin 22) using a 0.01 µF.
7. Terminal V_M is used to achieve less than a ± ½ LSB nonlinearity error. The external circuit to achieve this is shown in the application drawing.
8. All pins not being used should be grounded.
9. Substantial analog and digital ground planes must be provided. It is recommended that these ground planes are taken to a common point, the power ground line, as close to the converter as possible.
10. The power supplies to analog and digital inputs (-5.2V) should be supplied from separate, isolated power supplies. If one of the power supplies fails or is shorted to ground for more than 1 second there is a possibility the device may be destroyed. Both -5.2V lines should be decoupled using 1 µF and 0.01 µF capacitors located as close to the pins as possible.

TABLE 1. DIGITAL OUTPUT CODES

MINV / LINV	0 / 0	0 / 1	1 / 0	1 / 1
0.0000V	1111 1111	1000 0000	0111 1111	0000 0000
-0.0078V	1111 1110	1000 0001	0111 1110	0000 0001
-0.9961V	1000 0000	1111 1111	0000 0000	0111 1111
-1.0039V	0111 1111	0000 0000	1111 1111	1000 0000
-1.9922V	0000 0001	0111 1110	1000 0001	1111 1110
-2.0000V	0000 0000	0111 1111	1000 0000	1111 1111

TIMING DIAGRAM



Dots (•) Indicate latch timings

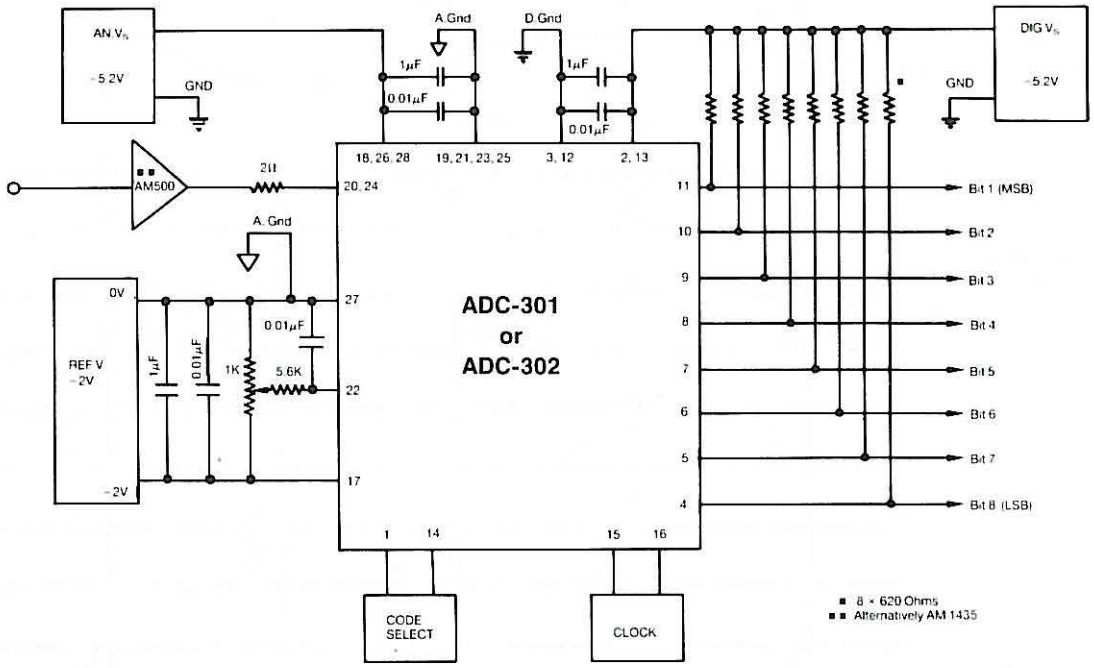
TIMING NOTES

1. Both Clock and $\overline{Clock}$ are required and the input levels are ECL. The timing T_1 and T_2 should be:

	T_1 (MIN)	T_2 (MIN)
ADC-301	25 nsec.	8 nsec.
ADC-302	15 nsec.	5 nsec.

2. The positive transition of the clock latches the comparator outputs into the 'and' gates.
3. The negative transition latches the 'anded' outputs into the 6-bit encoder.
4. The next positive transition will latch the 6-bit encoder output as well as starting the next conversion cycle.
5. The 8-bit encoder output will appear at the output pins 4.0 nsec. (typical) T_3 after 6-bit encoder output has been latched on the next negative transition of the clock.

CONNECTION AND APPLICATION



ORDERING INFORMATION

MODEL NO.	OPERATING TEMPERATURE RANGE
ADC-301	-20°C to + 100°C
ADC-302	-20°C to + 100°C

ACCESSORIES

Part Number	Description
TP 1K	Trimming Potentiometer

Note: For units with high-reliability processing, contact the factory.