

## AGR18090E 90 W, 1.805 GHz—1.880 GHz, LDMOS RF Power Transistor

### Introduction

The AGR18090E is a high-voltage, gold-metalized, laterally diffused metal oxide semiconductor (LDMOS) RF power transistor suitable for global system for mobile communication (GSM), enhanced data for global evolution (EDGE), and multicarrier class AB power amplifier applications. This device is manufactured using advanced LDMOS technology offering state-of-the-art performance and reliability. It is packaged in an industry-standard package and is capable of delivering a typical output power of 90 W, which makes it ideally suited for today's wireless base station RF power amplifier applications.

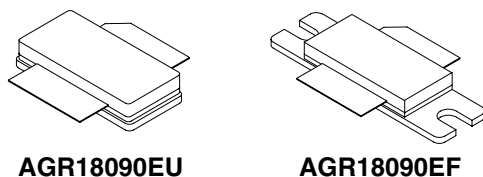


Figure 1. Available Packages

### Features

Typical performance ratings for GSM EDGE ( $f = 1.840$  GHz,  $P_{OUT} = 30$  W):

- Modulation spectrum:  
@  $\pm 400$  kHz =  $-63$  dBc.  
@  $\pm 600$  kHz =  $-73$  dBc.
- Error vector magnitude (EVM) = 1.7%.
- Gain = 15 dB.
- Drain Efficiency = 31%.

Typical continuous wave (CW) performance over entire digital communication system (DCS) band:

- $P_{1dB}$ : 90 W typ.
- Power gain: @  $P_{1dB} = 14$  dB.
- Efficiency @  $P_{1dB} = 50\%$  typ.
- Return loss:  $-10$  dB.

High-reliability gold-metalization process.

Low hot carrier injection (HCI) induced bias drift over 20 years.

Internally matched.

High gain, efficiency, and linearity.

Integrated ESD protection.

90 W minimum output power.

Device can withstand 10:1 voltage standing wave ratio (VSWR) at 26 Vdc, 1.840 GHz, 90 W CW output power.

Large signal impedance parameters available.

Table 1. Thermal Characteristics

| Parameter                                | Sym             | Value | Unit                 |
|------------------------------------------|-----------------|-------|----------------------|
| Thermal Resistance,<br>Junction to Case: |                 |       |                      |
| AGR18090EU                               | $R_{\theta JC}$ | 0.75  | $^{\circ}\text{C/W}$ |
| AGR18090EF                               | $R_{\theta JC}$ | 0.75  | $^{\circ}\text{C/W}$ |

Table 2. Absolute Maximum Ratings\*

| Parameter                                         | Sym       | Value      | Unit                        |
|---------------------------------------------------|-----------|------------|-----------------------------|
| Drain-source Voltage                              | $V_{DS}$  | 65         | Vdc                         |
| Gate-source Voltage                               | $V_{GS}$  | $-0.5, 15$ | Vdc                         |
| Drain Current—Continuous                          | $I_D$     | 8.5        | Adc                         |
| Total Dissipation at $T_c = 25^{\circ}\text{C}$ : |           |            |                             |
| AGR18090EU                                        | $P_D$     | 230        | W                           |
| AGR18090EF                                        | $P_D$     | 230        | W                           |
| Derate Above $25^{\circ}\text{C}$ :               |           |            |                             |
| AGR18090EU                                        | —         | 1.31       | $\text{W}/^{\circ}\text{C}$ |
| AGR18090EF                                        | —         | 1.31       | $\text{W}/^{\circ}\text{C}$ |
| Operating Junction Temperature                    | $T_J$     | 200        | $^{\circ}\text{C}$          |
| Storage Temperature Range                         | $T_{STG}$ | $-65, 150$ | $^{\circ}\text{C}$          |

\* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating\*

| AGR18090E | Minimum (V) | Class |
|-----------|-------------|-------|
| HBM       | 500         | 1B    |
| MM        | 50          | A     |
| CDM       | 1500        | 4     |

\* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs both a human-body model (HBM) and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114 (HBM) and JESD22-C101 (CDM) standards.

**Caution:** MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

## Electrical Characteristics

Recommended operating conditions apply unless otherwise specified:  $T_C = 30\text{ }^{\circ}\text{C}$ .

**Table 4. dc Characteristics**

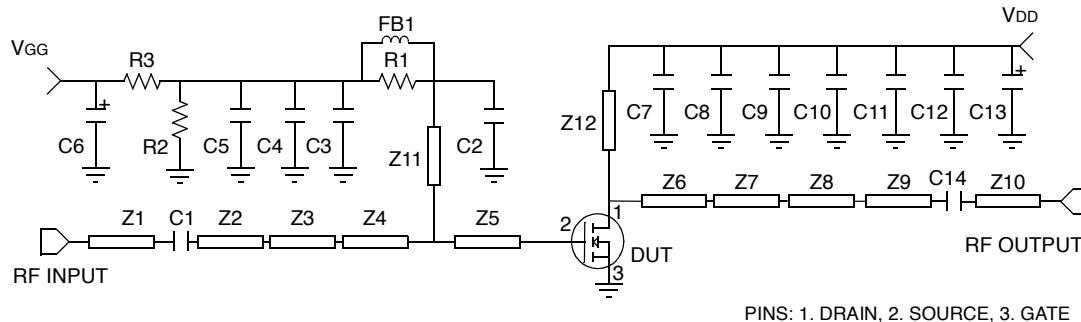
| Parameter                                                                                  | Symbol        | Min | Typ  | Max | Unit            |
|--------------------------------------------------------------------------------------------|---------------|-----|------|-----|-----------------|
| <b>Off Characteristics</b>                                                                 |               |     |      |     |                 |
| Drain-source Breakdown Voltage ( $V_{GS} = 0$ , $I_D = 300\text{ }\mu\text{A}$ )           | $V_{(BR)DSS}$ | 65  | —    | —   | Vdc             |
| Gate-source Leakage Current ( $V_{GS} = 5\text{ V}$ , $V_{DS} = 0\text{ V}$ )              | $I_{GSS}$     | —   | —    | 3.0 | $\mu\text{Adc}$ |
| Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ V}$ , $V_{GS} = 0\text{ V}$ ) | $I_{DSS}$     | —   | —    | 150 | $\mu\text{Adc}$ |
| <b>On Characteristics</b>                                                                  |               |     |      |     |                 |
| Forward Transconductance ( $V_{DS} = 10\text{ V}$ , $I_D = 1\text{ A}$ )                   | $G_{FS}$      | —   | 6.4  | —   | S               |
| Gate Threshold Voltage ( $V_{DS} = 10\text{ V}$ , $I_D = 300\text{ }\mu\text{A}$ )         | $V_{GS(TH)}$  | —   | —    | 4.8 | Vdc             |
| Gate Quiescent Voltage ( $V_{DS} = 28\text{ V}$ , $I_{DQ} = 800\text{ mA}$ )               | $V_{GS(Q)}$   | —   | 3.8  | —   | Vdc             |
| Drain-source On-voltage ( $V_{GS} = 10\text{ V}$ , $I_D = 1\text{ A}$ )                    | $V_{DS(ON)}$  | —   | 0.11 | —   | Vdc             |

**Table 5. RF Characteristics**

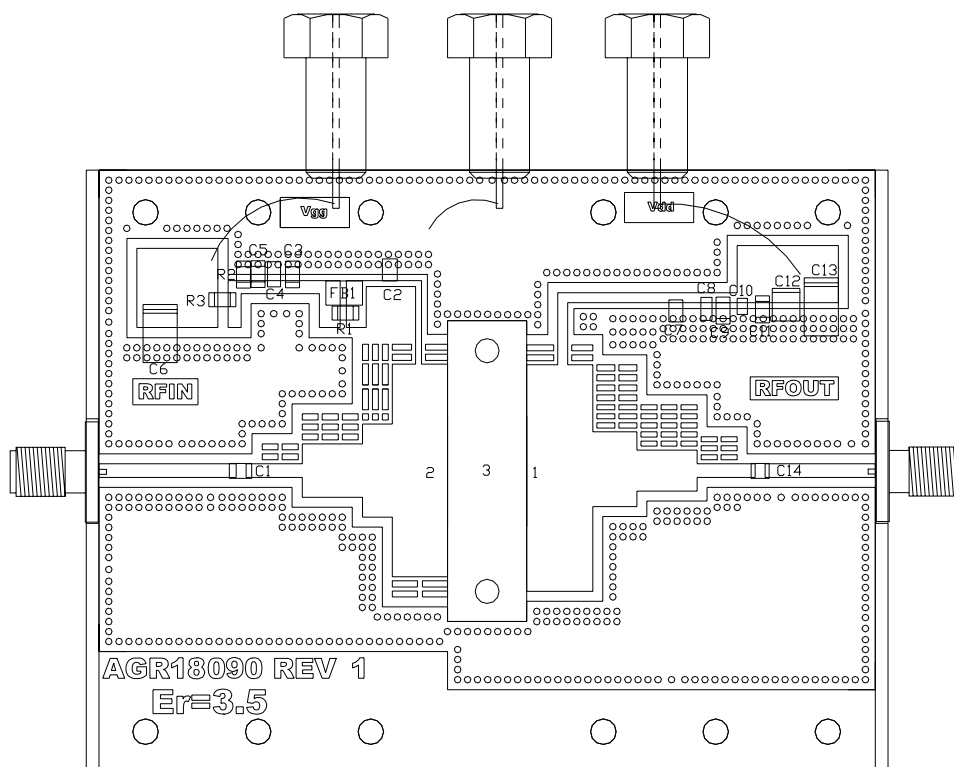
| Parameter                                                                                                                                   | Symbol    | Min                             | Typ | Max | Unit |
|---------------------------------------------------------------------------------------------------------------------------------------------|-----------|---------------------------------|-----|-----|------|
| <b>Dynamic Characteristics</b>                                                                                                              |           |                                 |     |     |      |
| Drain-to-gate Capacitance<br>( $V_{DS} = 26\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )                                               | $C_{RSS}$ | —                               | 2.1 | —   | pF   |
| Drain-to-source Capacitance<br>( $V_{DS} = 26\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )                                             | $C_{OSS}$ | —                               | 48  | —   | pF   |
| <b>Functional Tests (in Supplied Test Fixture)</b>                                                                                          |           |                                 |     |     |      |
| Power Gain<br>( $V_{DS} = 26\text{ V}$ , $P_{OUT} = 90\text{ W}$ , $I_{DQ} = 800\text{ mA}$ )                                               | $G_L$     | —                               | 14  | —   | dB   |
| Drain Efficiency<br>( $V_{DS} = 26\text{ V}$ , $P_{OUT} = 90\text{ W}$ , $I_{DQ} = 800\text{ mA}$ )                                         | $\eta$    | —                               | 50  | —   | %    |
| EDGE Linearity Characterization<br>( $P_{OUT} = 30\text{ W}$ , $f = 1.840\text{ GHz}$ , $V_{DS} = 26\text{ V}$ , $I_{DQ} = 800\text{ mA}$ ) |           |                                 |     |     |      |
| Modulation spectrum @ $\pm 400\text{ kHz}$                                                                                                  |           | —                               | −63 | —   | dBc  |
| Modulation spectrum @ $\pm 600\text{ kHz}$                                                                                                  |           | —                               | −73 | —   | dBc  |
| Output Power<br>( $V_{DS} = 26\text{ V}$ , 1 dB gain compression, $I_{DQ} = 800\text{ mA}$ )                                                | $P_{1dB}$ | —                               | 90  | —   | W    |
| Input Return Loss                                                                                                                           | $IRL$     | —                               | −12 | −8  | dB   |
| Ruggedness<br>( $V_{DS} = 26\text{ V}$ , $P_{OUT} = 90\text{ W}$ , $I_{DQ} = 800\text{ mA}$ , $V_{SWR} = 10:1$ , all angles)                | $\psi$    | No degradation in output power. |     |     |      |

1. Across full DCS band, 1.805 GHz—1.880 GHz.

## Test Circuit Illustrations for AGR18090E



### A. Schematic



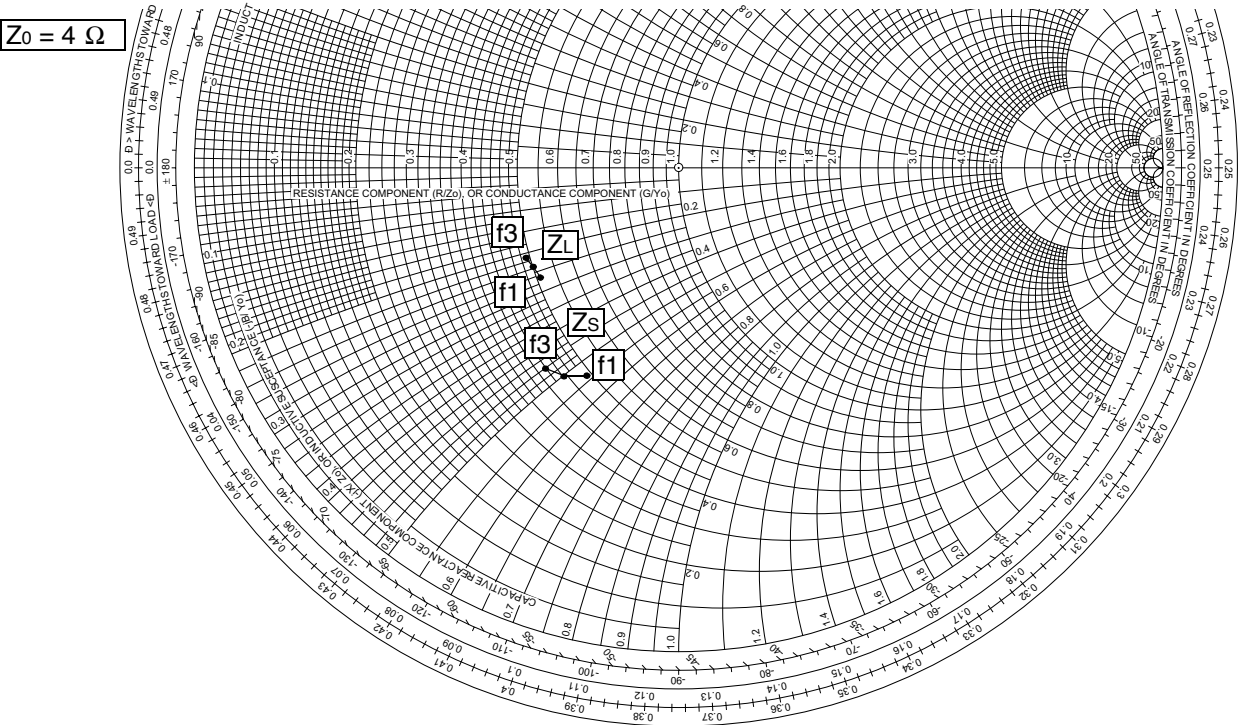
#### Parts List:

- Microstrip line: Z1 0.685 in. x 0.067 in.; Z2 0.280 in. x 0.067 in.; Z3 0.300 in. x 0.265 in.; Z4 0.150 in. x 0.465 in.; Z5 0.275 in. x 1.060 in.; Z6 0.330 in. x 1.130 in.; Z7 0.220 in. x 0.375 in.; Z8 0.300 in. x 0.205 in.; Z9 0.290 in. x 0.067 in.; Z10 0.550 in. x 0.067 in.; Z11 0.545 in. x 0.030 in.; Z12 0.800 in. x 0.050 in.
- ATC<sup>®</sup> chip capacitors: C1, C14, 12 pF 100B120JW500X; C2, C7, 10 pF 100B100JW500X.
- Sprague<sup>®</sup> tantalum surface-mount chip capacitors: C6, C13, 22  $\mu$ F, 35 V.
- Kemet<sup>®</sup> 0603 size chip capacitor: C8, 220 pF; 1206 size chip capacitors: C5, C11, 0.1  $\mu$ F C1206104K5RAC7800; 1812 size chip capacitor: C12, 1.0  $\mu$ F C1812C105K5RACTR.
- Murata<sup>®</sup> 0805 size chip capacitors: C4, C10, 0.01  $\mu$ F GRM40X7R103K100AL.
- 1206 size chip resistors: R1 4.7 k $\Omega$ , R2 560 k $\Omega$ , R3 1.02 k $\Omega$ .
- Vitramor<sup>®</sup> 1206 size chip capacitors: C3, C9, 22000 pF.
- Fair-rite<sup>®</sup> ferrite bead FB1 2743019447.
- Taconic<sup>®</sup> ORCER RF-35: board material, 1 oz. copper, 30 mil thickness,  $\epsilon_r = 3.5$ .

### B. Component Layout

**Figure 2. AGR18090E Test Circuit**

Typical Performance Characteristics



| GHz (f)     | $Z_s\ \Omega$<br>(Complex Source Impedance) | $Z_L\ \Omega$<br>(Complex Optimum Load Impedance) |
|-------------|---------------------------------------------|---------------------------------------------------|
| 1.805 (f1)  | $1.90 - j2.16$                              | $2.05 - j1.27$                                    |
| 1.8425 (f2) | $1.77 - j1.97$                              | $2.00 - j1.14$                                    |
| 1.880 (f3)  | $1.69 - j1.82$                              | $1.97 - j1.06$                                    |

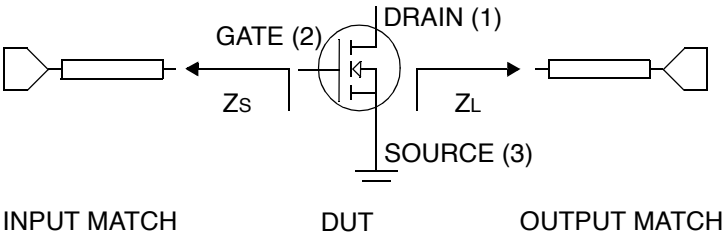
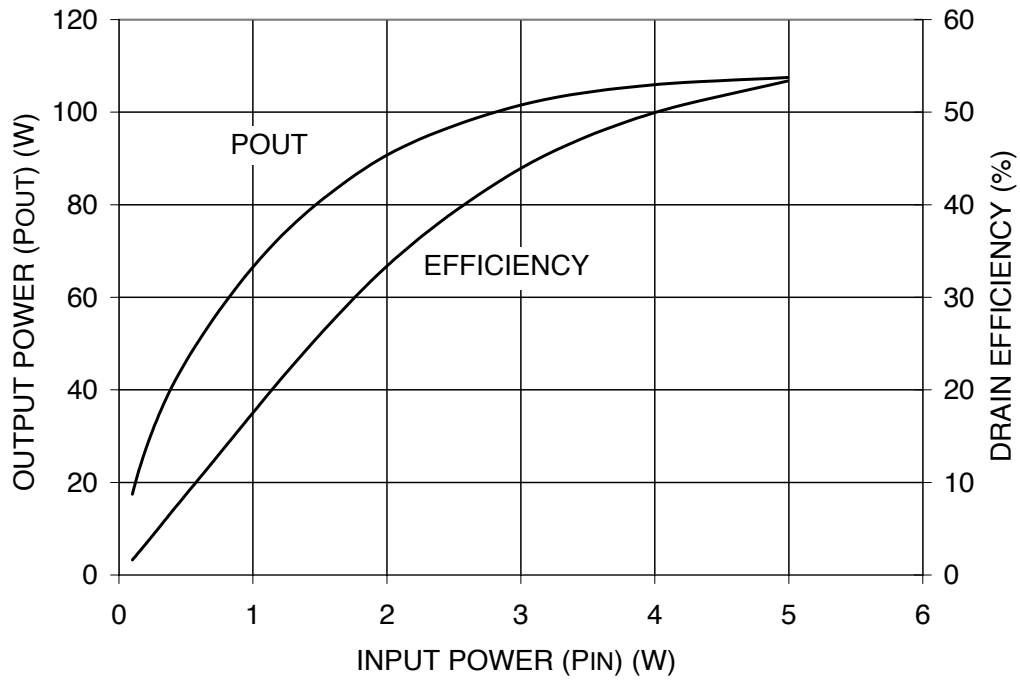


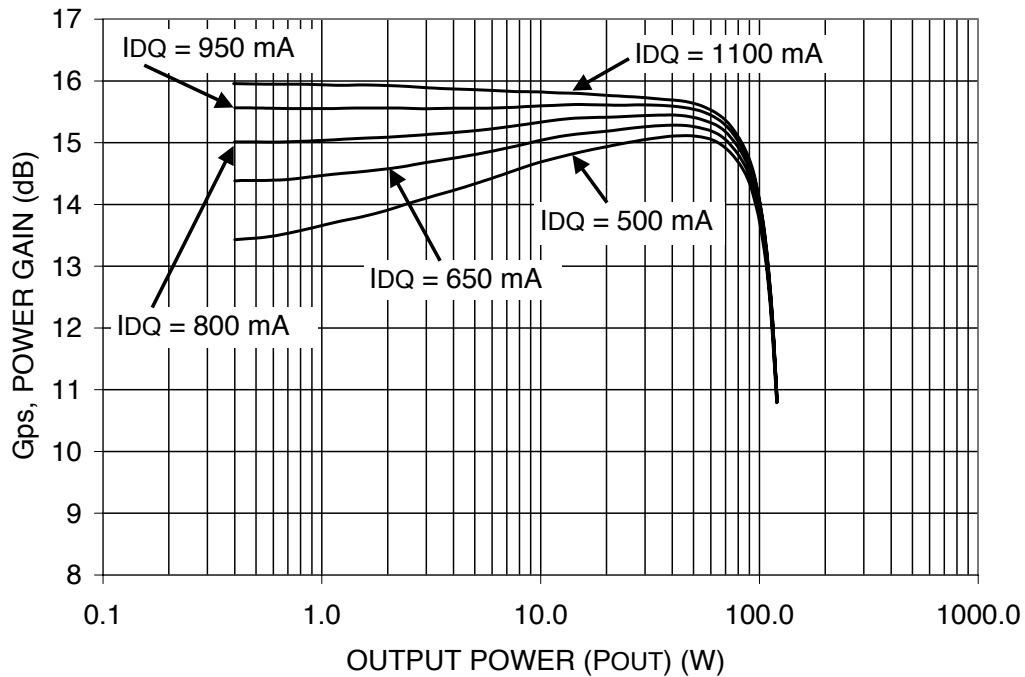
Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)



$V_{DD} = 26$  V,  $I_{DQ} = 800$  mA,  $f = 1842.5$  MHz, CW Measurement

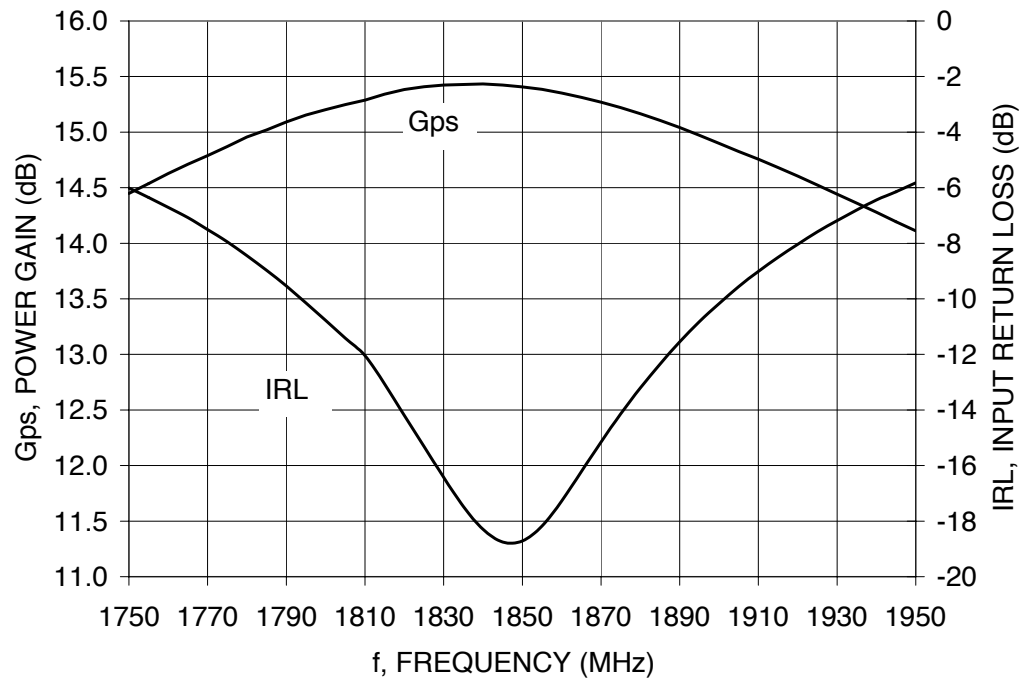
Figure 4. Output Power and Efficiency vs. Input Power



$V_{DD} = 26$  V,  $f = 1842.5$  MHz, CW Measurement

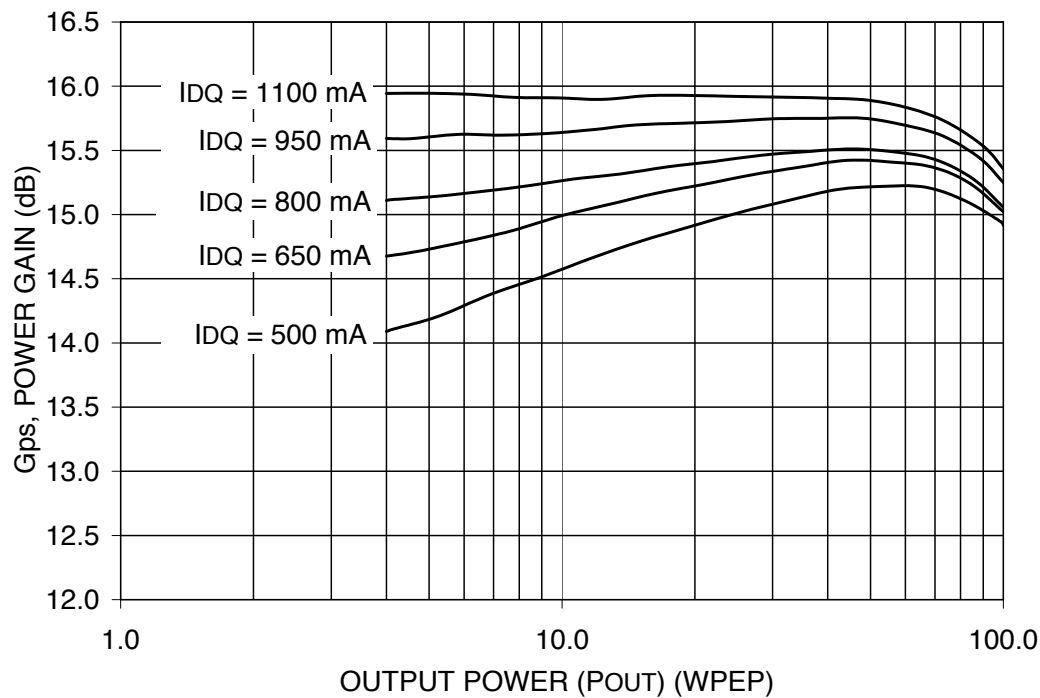
Figure 5. CW Power Gain vs. Output Power

Typical Performance Characteristics (continued)



$V_{DD} = 26\text{ V}$ ,  $I_{DQ} = 800\text{ mA}$ ,  $P_{IN} = 25\text{ dBm}$ , CW Measurement

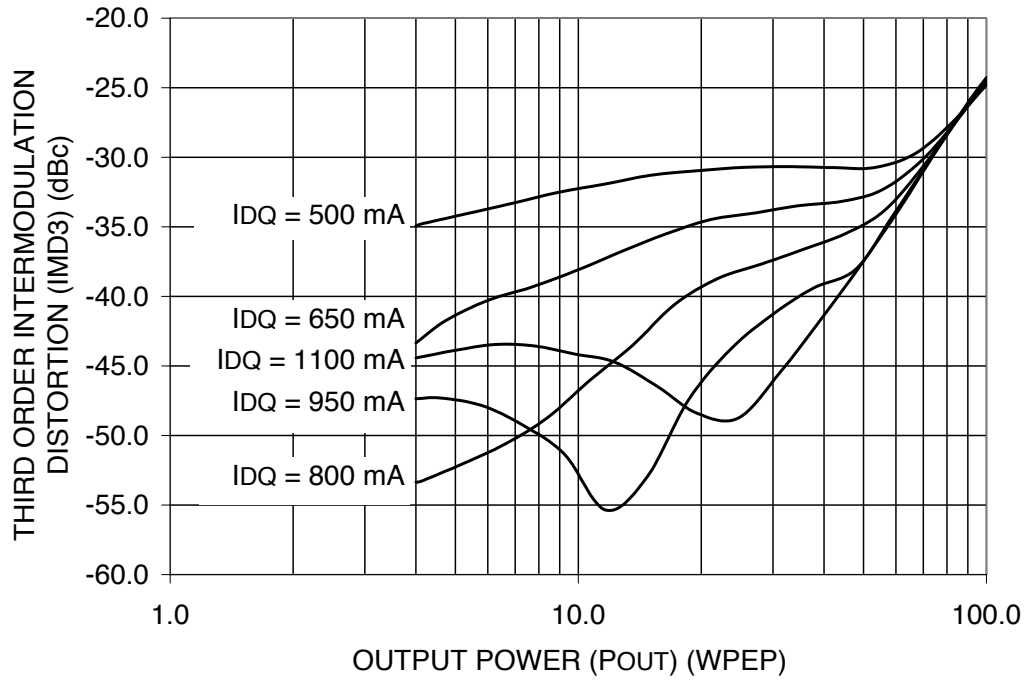
Figure 6. Wideband Gain and Return Loss



$V_{DD} = 26\text{ V}$ ,  $f_c = 1842.5\text{ MHz}$ , Two Tone Measurement, 100 kHz Spacing

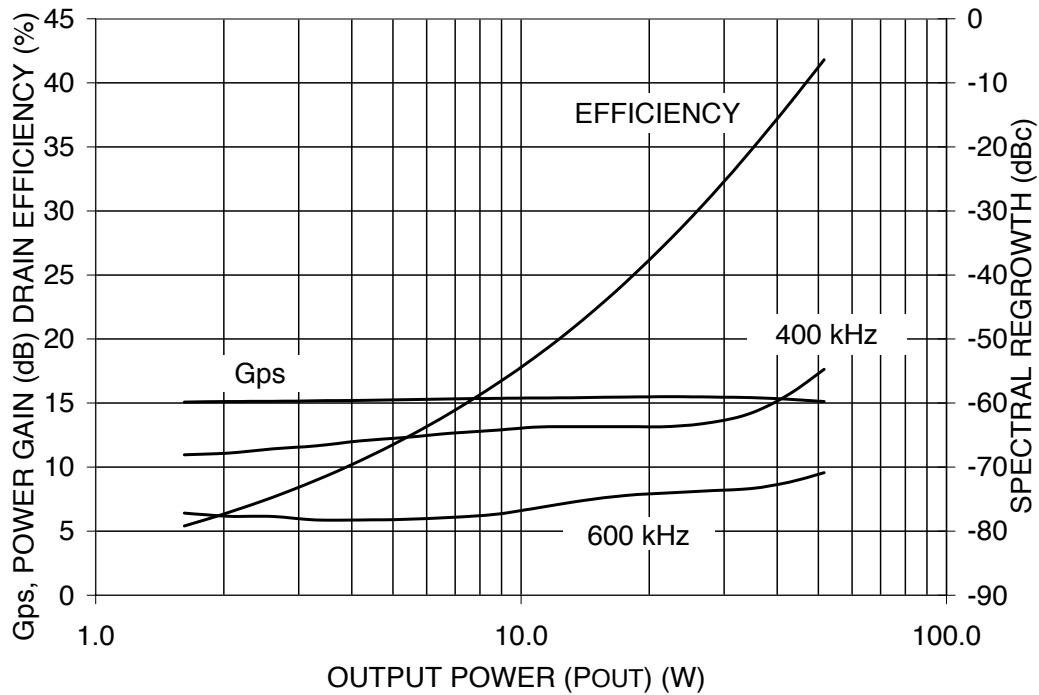
Figure 7. Two Tone Power Gain vs. Output Power

## Typical Performance Characteristics (continued)



$V_{DD} = 26 \text{ V}$ ,  $f_c = 1842.5 \text{ MHz}$ , Two Tone Measurement, 100 kHz Spacing

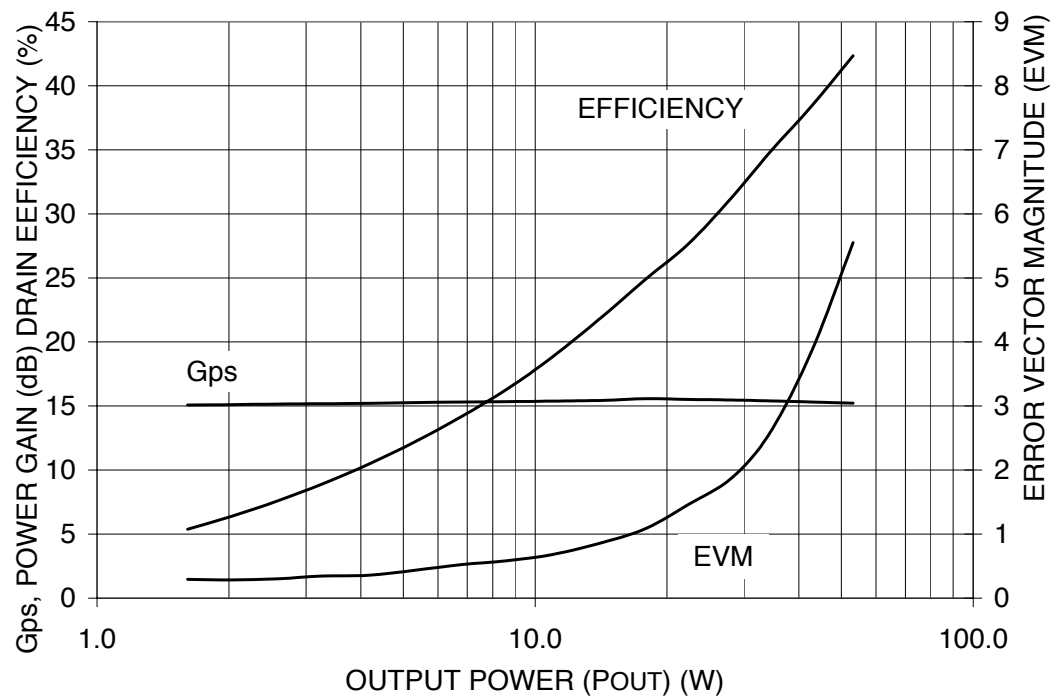
**Figure 8. Intermodulation Distortion vs. Output Power**



$V_{DD} = 26 \text{ V}$ ,  $I_{DQ} = 800 \text{ mA}$ ,  $f_c = 1842.5 \text{ MHz}$ , EDGE Modulation

**Figure 9. Power Gain, Efficiency, and Spectral Regrowth vs. Output Power**

Typical Performance Characteristics (continued)



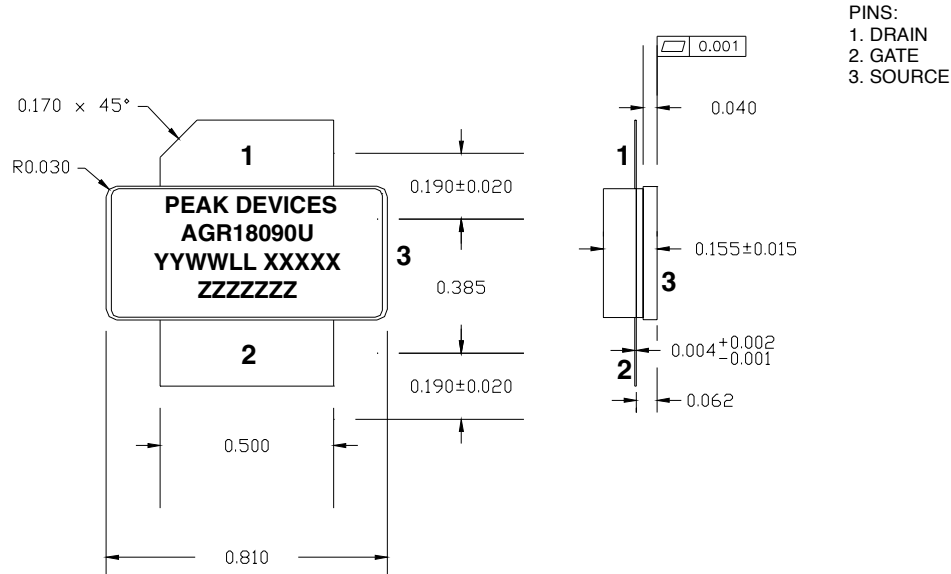
$V_{DD} = 26\text{ V}$ ,  $I_{DQ} = 800\text{ mA}$ ,  $f_c = 1842.5\text{ MHz}$ , EDGE Modulation

Figure 10. Power Gain, Efficiency, and EVM vs. Output Power

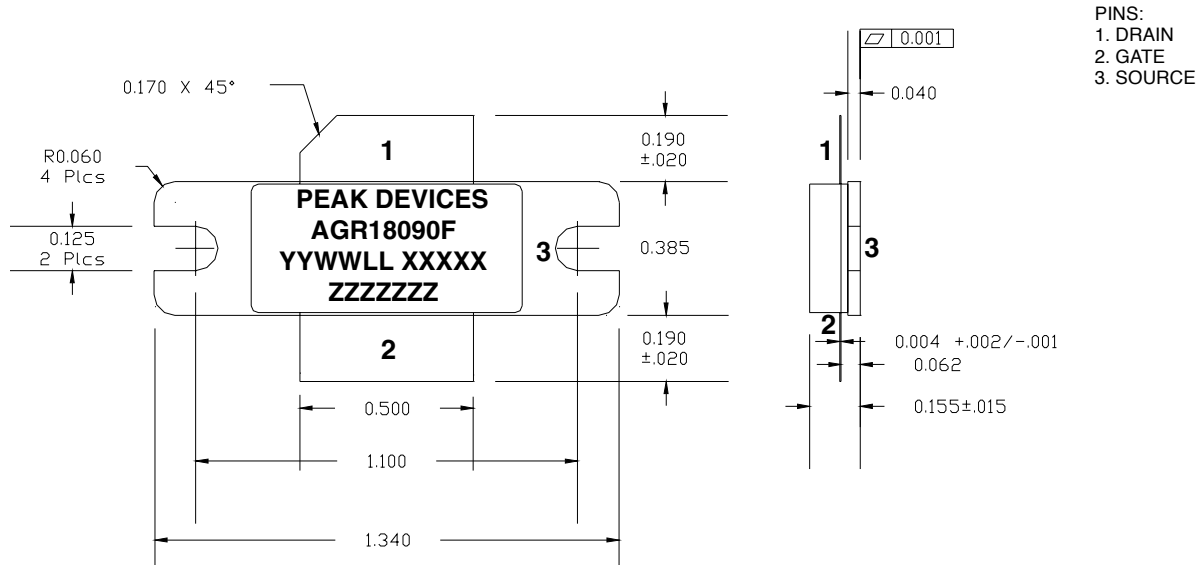
## Package Dimensions

All dimensions are in inches. Tolerances are  $\pm 0.005$  in. unless specified.

### AGR18090EU



### AGR18090EF



#### Label Notes:

- M before the part number denotes model program. X before the part number denotes engineering prototype.
- YYWWLL is the date code including place of manufacture: year year work week (YYWW), LL = location (AL = Allentown, PA; BK = Bangkok, Thailand). XXXXX = five-digit wafer lot number.
- ZZZZZZZ = seven-digit assembly lot number on production parts.
- ZZZZZZZZZZZZ = 12-digit (five-digit lot, two-digit wafer, and five-digit serial number) on models and engineering prototypes.