

AOT412
N-Channel SDMOS™ Power Transistor
General Description

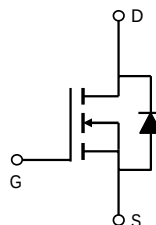
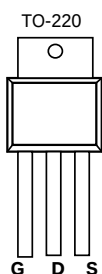
The AOT412 and AOT412L is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

- RoHS Compliant
- AOT412L is Halogen Free

Features

V_{DS} (V) = 100V
 I_D = 60A (V_{GS} = 10V)
 $R_{DS(ON)} < 15.8m\Omega$ (V_{GS} = 10V)
 $R_{DS(ON)} < 19.4m\Omega$ (V_{GS} = 7V)

100% UIS Tested!
100% R_g Tested!


Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current	I_D	60	A
$T_C=25^\circ\text{C}$		44	
$T_C=100^\circ\text{C}$			
Pulsed Drain Current ^C	I_{DM}	140	
Continuous Drain Current	I_{DSM}	8.2	A
$T_A=25^\circ\text{C}$		6.6	
$T_A=70^\circ\text{C}$			
Avalanche Current ^C	I_{AR}	47	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	110	mJ
Power Dissipation ^B	P_D	150	W
$T_C=25^\circ\text{C}$		75	
$T_C=100^\circ\text{C}$			
Power Dissipation ^A	P_{DSM}	2.6	W
$T_A=25^\circ\text{C}$		1.7	
$T_A=70^\circ\text{C}$			
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	15	18	$^\circ\text{C/W}$
$t \leq 10\text{s}$		40	48	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A D}				
Steady-State	$R_{\theta JC}$	0.7	1	$^\circ\text{C/W}$
Maximum Junction-to-Case				
Steady-State				

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	100			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^{\circ}\text{C}$			10 50	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 25\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.6	3.2	3.8	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	140			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=20\text{A}$ $T_J=125^{\circ}\text{C}$		13.2 25	15.8 30	$\text{m}\Omega$
		$V_{GS}=7\text{V}$, $I_D=20\text{A}$		15.5	19.4	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$		30		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.65	1	V
I_S	Maximum Body-Diode Continuous Current				60	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=50\text{V}$, $f=1\text{MHz}$	2150	2680	3220	pF
C_{oss}	Output Capacitance		180	260	340	pF
C_{rss}	Reverse Transfer Capacitance		60	100	140	pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	0.5	1	1.5	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=50\text{V}$, $I_D=20\text{A}$	36	45	54	nC
$Q_g(4.5\text{V})$	Total Gate Charge		10	12	14	nC
Q_{gs}	Gate Source Charge		14	17	20	nC
Q_{gd}	Gate Drain Charge		9	15	21	nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=50\text{V}$, $R_L=5\Omega$, $R_{GEN}=3\Omega$		19		ns
t_r	Turn-On Rise Time			16		ns
$t_{D(off)}$	Turn-Off DelayTime			27		ns
t_f	Turn-Off Fall Time			10		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$	15	22	29	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$	67	96	125	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

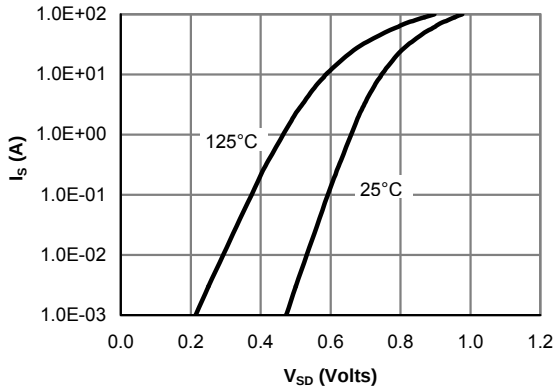
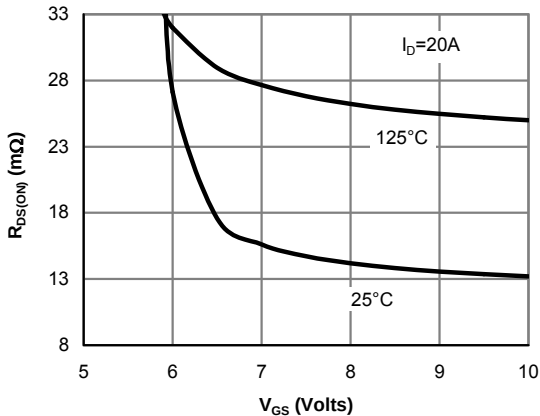
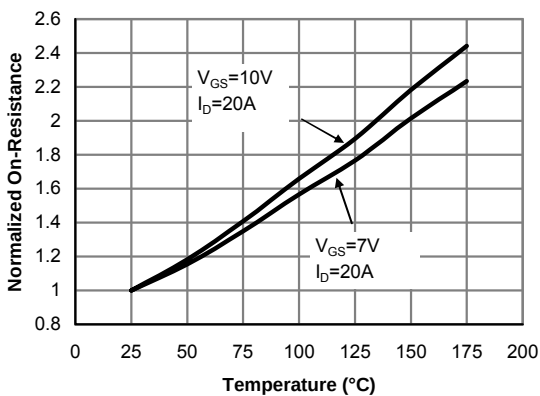
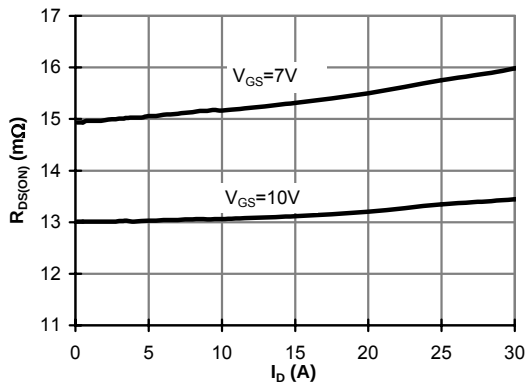
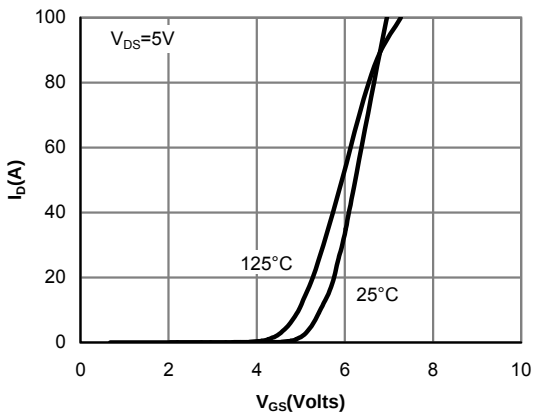
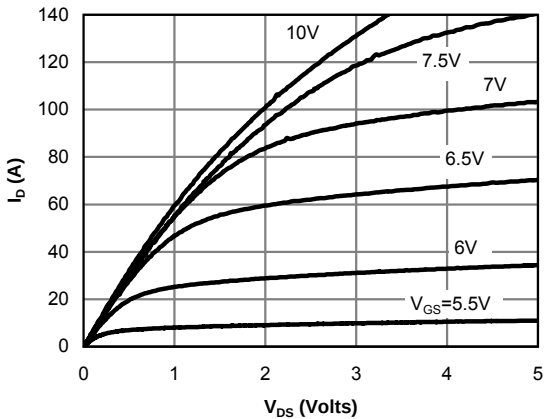
G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$.

Rev 0: Nov-08

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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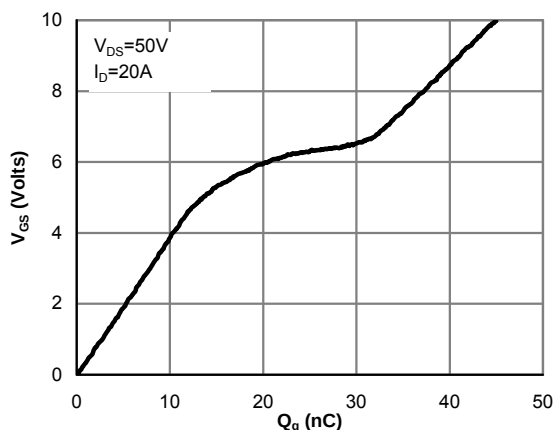


Figure 7: Gate-Charge Characteristics

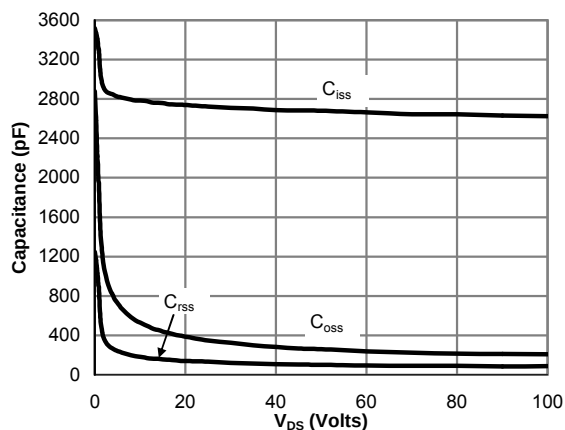


Figure 8: Capacitance Characteristics

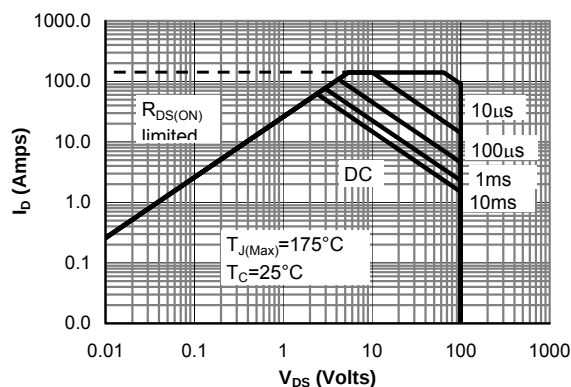


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

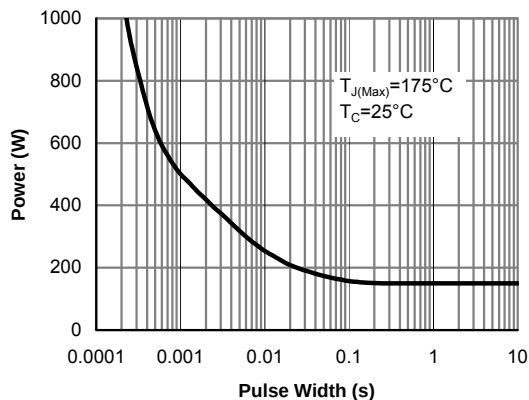


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

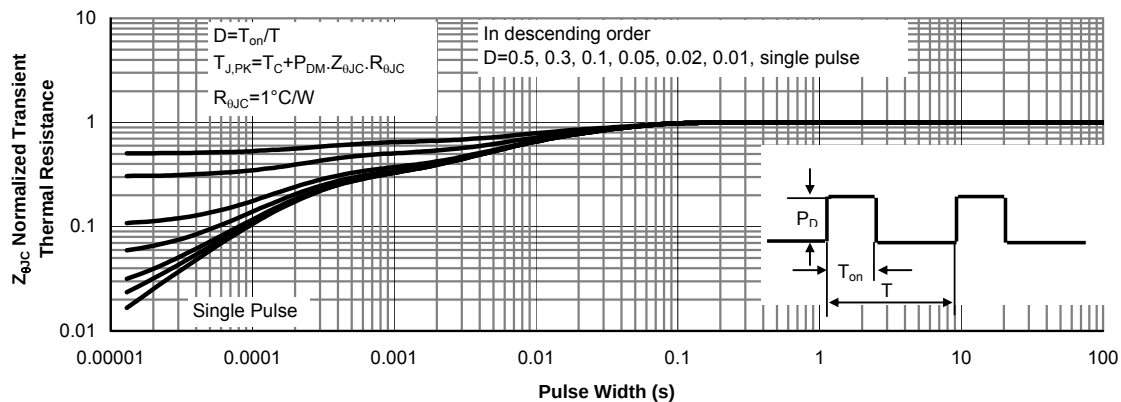


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

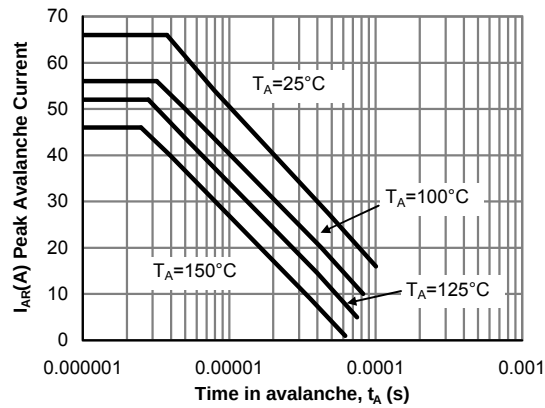


Figure 12: Single Pulse Avalanche capability (Note C)

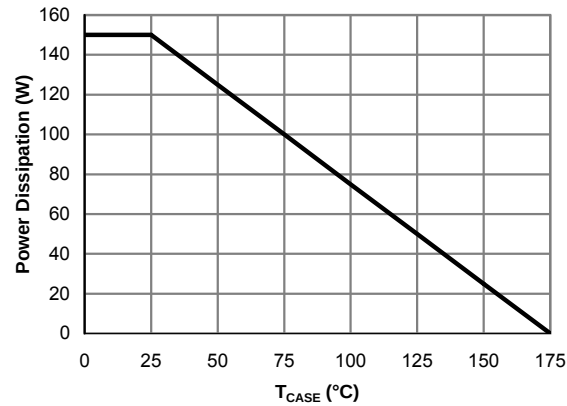


Figure 13: Power De-rating (Note F)

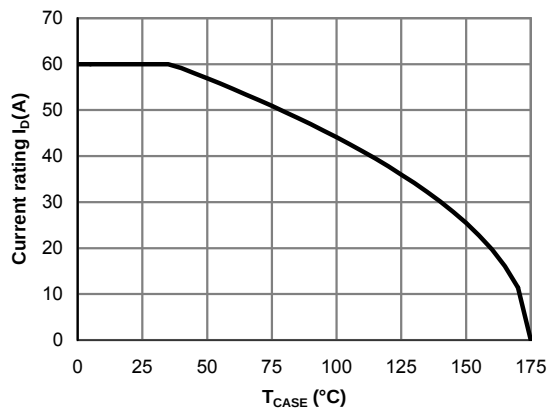


Figure 14: Current De-rating (Note F)

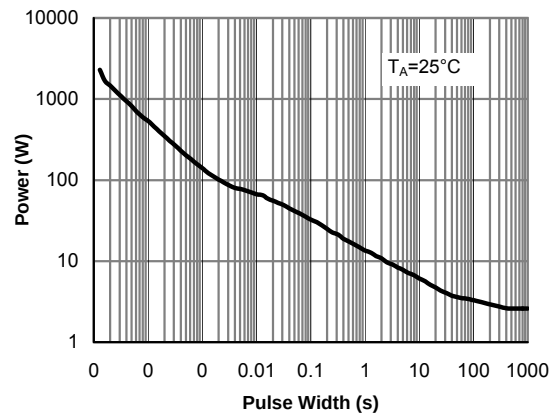


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

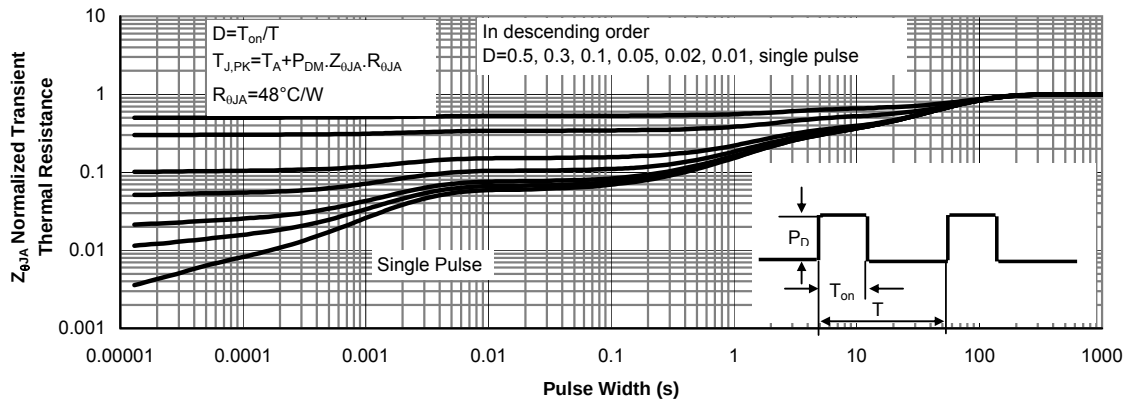


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

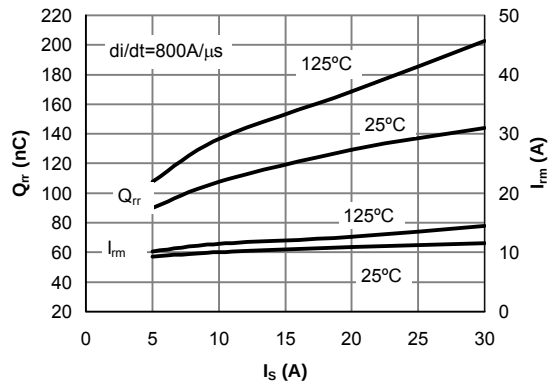


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

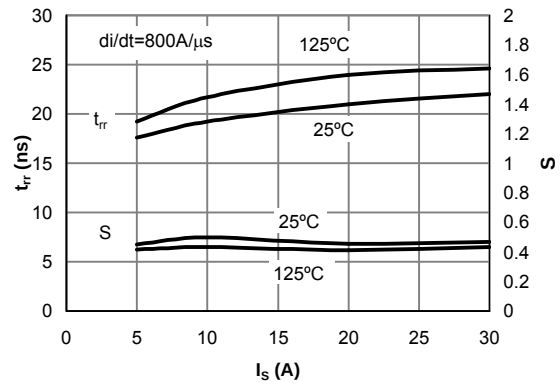


Figure 18: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

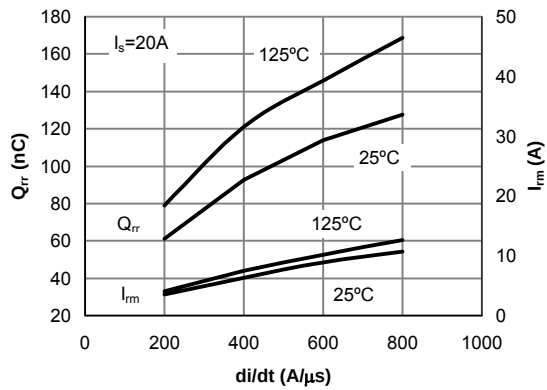


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. di/dt

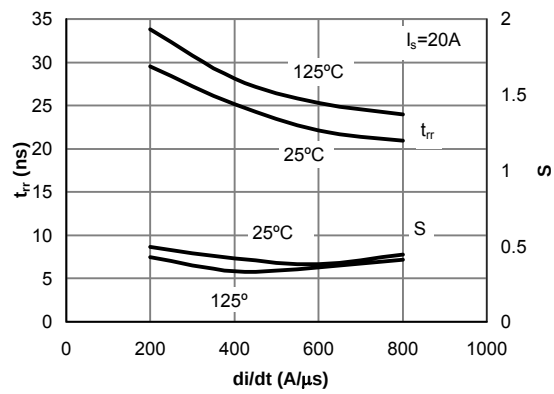
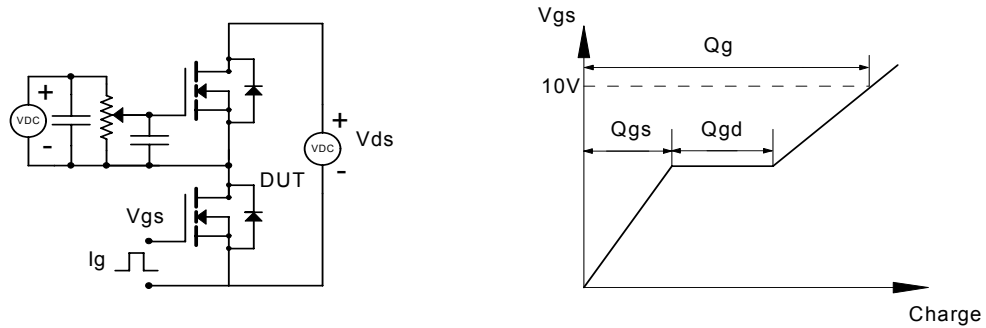
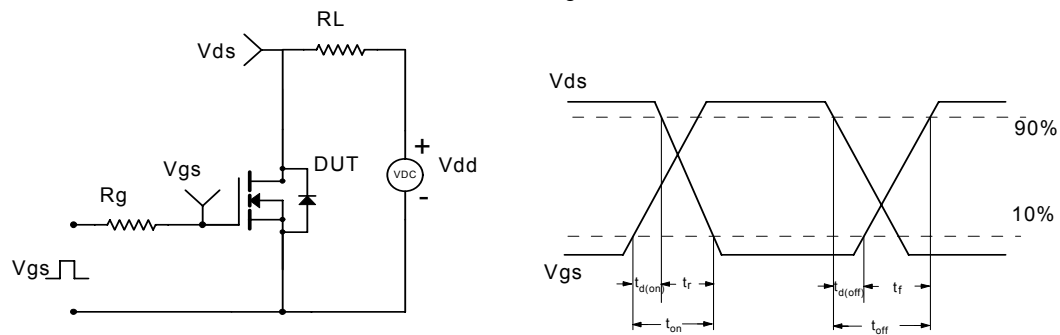


Figure 20: Diode Reverse Recovery Time and Softness Factor vs. di/dt

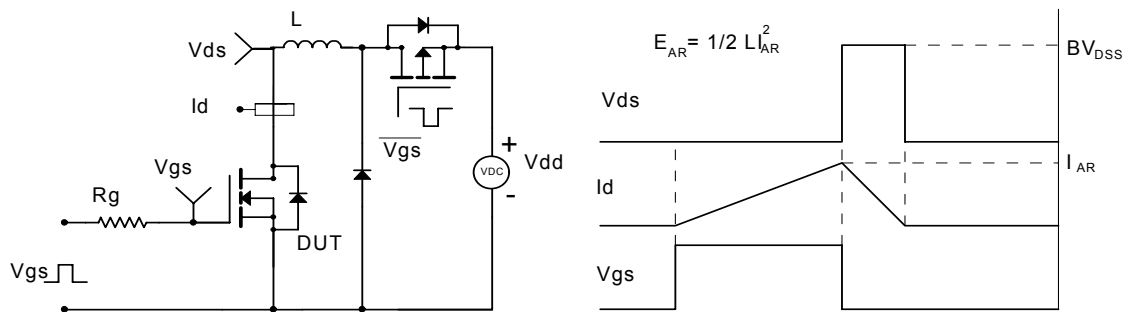
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

