Spread Spectrum Clock Generator for Mobile Applications

Features

- Generates a 4X EMI optimized clock signal at the Output.
- Input frequency   : 12.5MHz to 20MHz
- Output frequency : 50MHz to 80MHz
- SSON/PDB option
- Selectable Centre Spread : ± 0.5%, ± 1.0%
- Low power CMOS design
- Supply Voltage : 3.3V ± 0.3V
- Industrial Temperature range
- 8-pin TSSOP Package
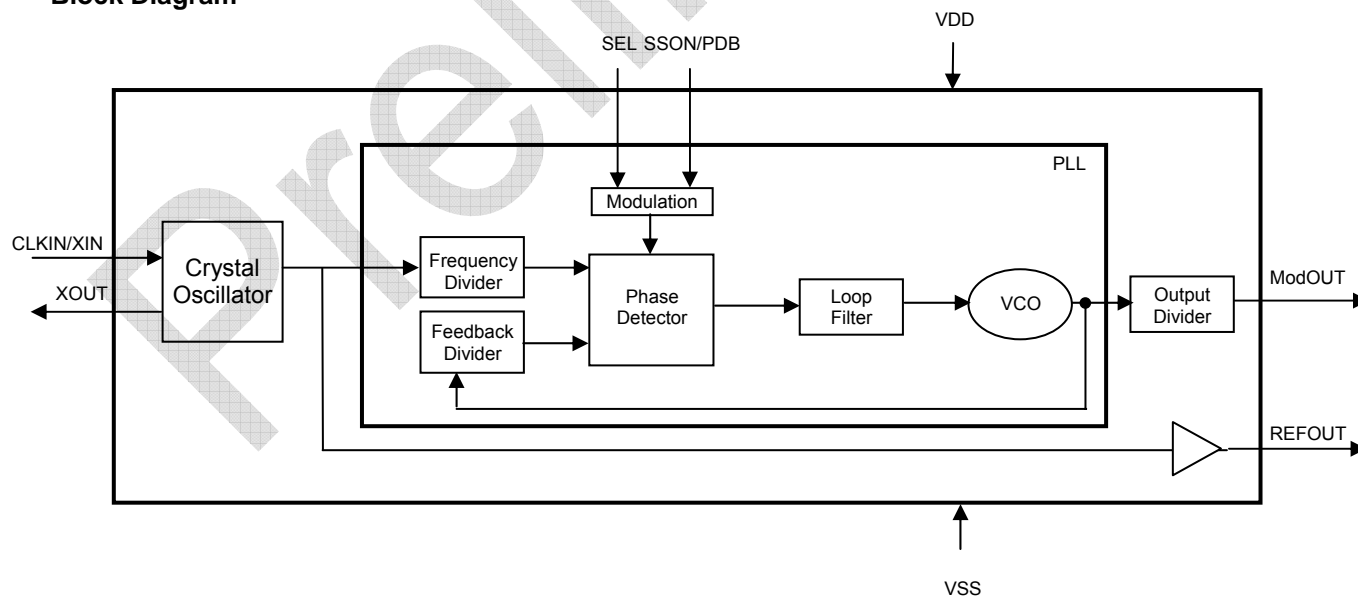- Drop-in replacement for MB88155-412 Device

Product Description

The ASM3P2187A/B is a versatile spread spectrum frequency modulator designed specifically for a wide range of clock frequencies. The ASM3P2187A/B reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. The ASM3P2187A/B allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding that are traditionally required to pass EMI regulations.
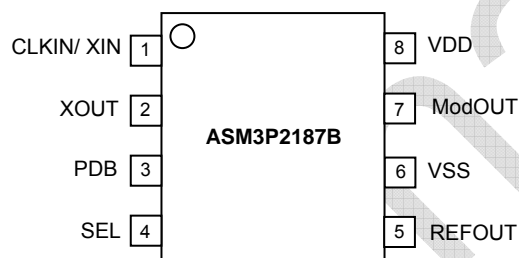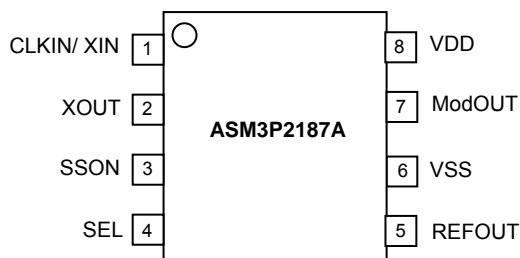ASM3P2187A device has an option of Spread ON/OFF and ASM3P2187B device has Powerdown option

Application

The ASM3P2187A/B is targeted towards mobile phones, mobile audio players and PDAs.

Block Diagram

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Pin Configurations

CLKIN/ XIN | 1   ASM3P2187A   8 | VDD
XOUT | 2   7 | ModOUT
SSON | 3   6 | VSS
SEL | 4   5 | REFOUT

CLKIN/ XIN | 1   ASM3P2187B   8 | VDD
XOUT | 2   7 | ModOUT
PDB | 3   6 | VSS
SEL | 4   5 | REFOUT

Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN/XIN	I	External reference Clock input or Crystal connection.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	SSON / PDB*	I	Modulation enable pin/ Power down pin. Has an Internal pull up resistor
4	SEL	I	Modulation rate setting pin Centre spread, SEL = "L" : Frequency Deviation ± 0.5% Centre spread, SEL = "H" : Frequency Deviation ± 1.0% Has an Internal pull up resistor.
5	REFOUT	O	Non-modulated clock output pin. The Frequency is same as input frequency. This pin becomes to "L" at power-down.
6	VSS	P	Ground Connection. Connect to system ground.
7	ModOUT	O	Modulated clock output pin This pin becomes to"L" at power-down.
8	VDD	P	Power Supply Voltage Pin. Connect to +3.3V.

* SSON Pin is available in ASM3P2187A Device and PDB Pin is available in ASM3P2187B Device

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Modulation Enable Setting Table

SSON	Modulation
L	No Modulation
H	Modulation

Power down Status Table

PDB	Status
L	Power Down Status
H	Operating Status

Spread Range Selection Table

SEL	Deviation @ 15MHz
L	± 0.50%
H	± 1.00%

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD	Supply Voltage pin with respect to Ground	-0.5 to +4.6	V
V_{IN}	Input Voltage pin with respect to Ground	VSS-0.5 to VDD+0.5	V
V_{OUT}	Output Voltage pin with respect to Ground	VSS-0.5 to VDD+0.5	V
T_{STG}	Storage temperature	-55 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.
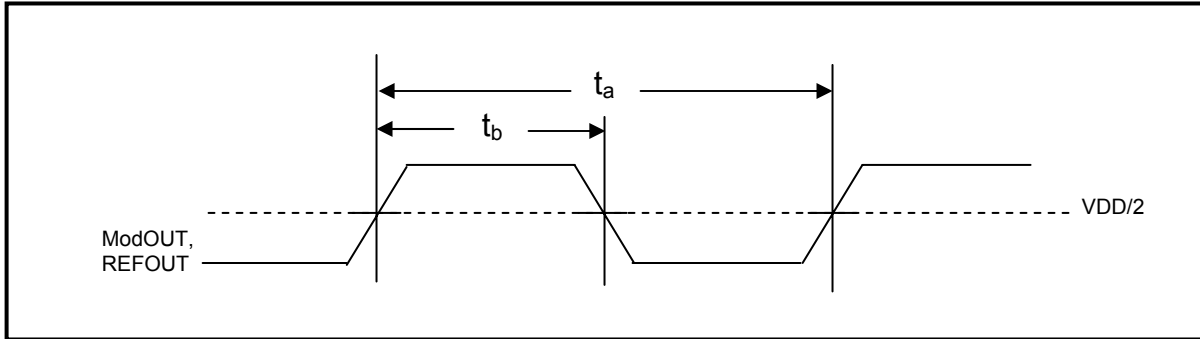
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DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
V_{IL}	Input low voltage		VSS – 0.3		0.8	V
V_{IH}	Input high voltage		2.0		VDD+ 0.3	V
I_{IL}	Input low current				-50	µA
I_{IH}	Input high current				+50	µA
V_{OL}	Output low voltage	For ModOUT, I_{OL} = 4mA	VSS		0.4	V
		For REFOUT, I_{OL} = 3mA				
V_{OH}	Output high voltage	For ModOUT, I_{OH} = -4mA	2.4		VDD	V
		For REFOUT, I_{OH} = -3mA				
I_{CC}	Dynamic supply current (Unloaded Outputs)				17	mA
I_{DD}	Static supply current standby mode (CLKIN/XIN pulled LOW)				8	mA
VDD	Operating voltage		3.3	3.3	3.6	V
t_{ON}	Power up time (first locked clock cycle after power up)			2	5	mS
Z_{OUT}	Clock output impedance			50		Ω
C_{IN}	Input Capacitance				7	pF
C_L	Load Capacitance				15	pF

AC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
CLKIN/XIN	Input Clock frequency		12.5	15	20	MHz
CLKOUT	Output Clock frequency	REFOUT	12.5	15	20	MHz
		ModOUT	50	60	80	
M_F	Modulation Frequency		32.4	39	52	KHz
t_{LH}*	Output rise time (Measured from 20% to 80%)			2	2.5	nS
t_{HL}*	Output fall time (Measured from 80% to 20%)			1.5	2	nS
t_{JC}	Cycle to Cycle Jitter			±250	±325	pS
t_{Jp}	Period Jitter (REFOUT)			±150	±200	
t_D	Output duty cycle		45	50	55	%

*t_{LH} and t_{HL} are measured with a capacitive load of 15pF

Giving you the edge

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Output Clock Duty Cycle $t_D = (t_b / t_a)$

Cycle –to- Cycle Jitter $(t_{JC} = [t_n - t_n + 1])$

Note: Cycle-cycle jitter indicates the difference between a certain cycle and the immediately
succeeding (or preceding) cycle

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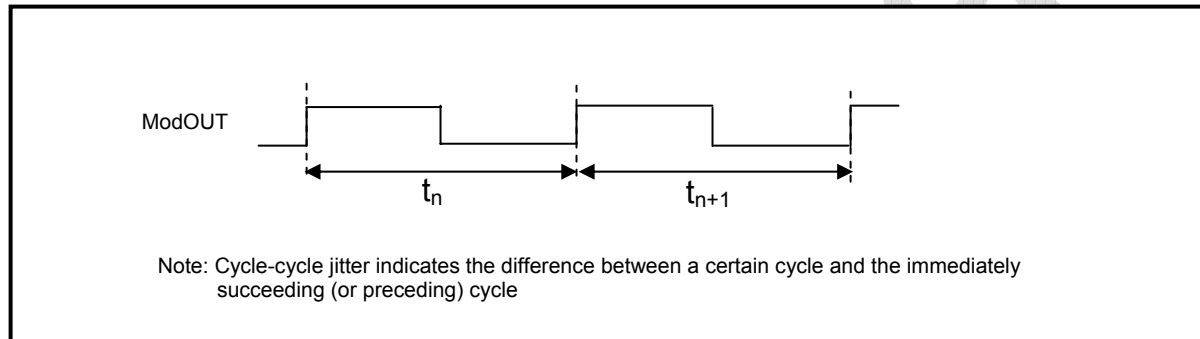
Typical Crystal Oscillator Circuit

R1 = 510Ω

C1 = 27 pF   C2 = 27 pF
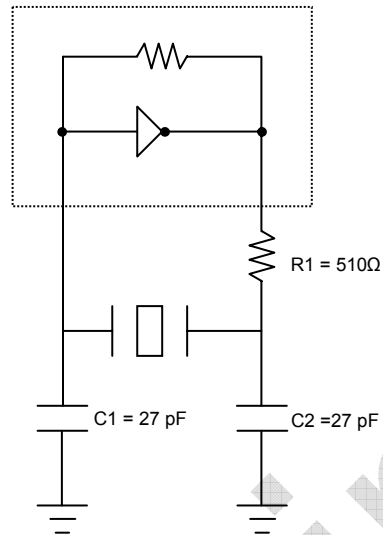
Typical Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	14.31818MHz
Frequency tolerance	± 50 ppm or better at 25°C
Operating temperature range	-25°C to +85°C
Storage temperature	-40°C to +85°C
Load capacitance	18pF
Shunt capacitance	7pF maximum
ESR	25Ω

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Package Information

Mechanical Package Outline 8-Pin TSSOP
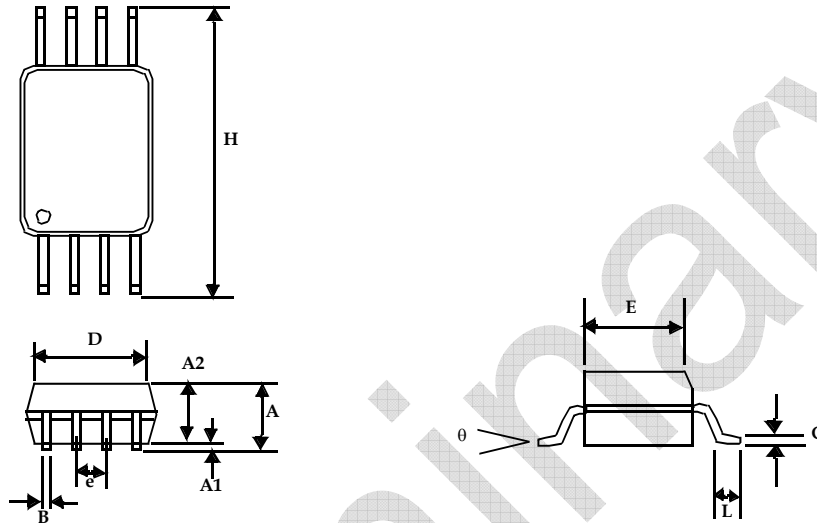
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

Note: Controlling dimensions are millimeters
      TSSOP – 0.034 grams unit weight

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Ordering Code

Part Number	Marking	Package Type	Temperature
ASM3P2187AG-08TT	3P2187AG	8-Pin TSSOP, TUBE, Green	Commercial
ASM3P2187AG-08TR	3P2187AG	8-Pin TSSOP, TAPE & REEL, Green	Commercial
ASM3I2187AG-08TT	3I2187AG	8-Pin TSSOP, TUBE, Green	Industrial
ASM3I2187AG-08TR	3I2187AG	8-Pin TSSOP, TAPE & REEL, Green	Industrial
ASM3P2187BG-08TT	3P2187BG	8-Pin TSSOP, TUBE, Green	Commercial
ASM3P2187BG-08TR	3P2187BG	8-Pin TSSOP, TAPE & REEL, Green	Commercial
ASM3I2187BG-08TT	3I2187BG	8-Pin TSSOP, TUBE, Green	Industrial
ASM3I2187BG-08TR	3I2187BG	8-Pin TSSOP, TAPE & REEL, Green	Industrial

Device Ordering Information

A S M 3 P 2 1 8 7 A G - 0 8 T R

R = Tape & Reel, T = Tube or Tray

O = SOT	U = MSOP
S = SOIC	E = TQFP
T = TSSOP	L = LQFP
A = SSOP	U = MSOP
V = TVSOP	P = PDIP
B = BGA	D = QSOP
Q = QFN	X = SC-70

DEVICE PIN COUNT

F = LEAD FREE AND RoHS COMPLIANT PART
G = GREEN PACKAGE, LEAD FREE, and RoHS

PART NUMBER

X= Automotive   I= Industrial   P or n/c = Commercial
  (-40C to +125C)   (-40C to +85C)   (0C to +70C)

1 = Clock Generator	6 = Power Management
2 = Non PLL based	7 = Power Management
3 = EMI Reduction	8 = Power Management
4 = DDR support products	9 = Hi Performance
5 = STD Zero Delay Buffer	0 = Reserved

PulseCore Semiconductor Mixed Signal Product

Licensed under U.S Patent Nos 5,488,627 and 5,631,921

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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003
Many PulseCore Semiconductor products are protected by issued patents or by applications for patent

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