



## Peak EMI Reducing Solution

### Features

- Generates an EMI optimized clock signal at output.
- Input frequency: 25MHz.
- Frequency outputs:
  - USB Clock (48MHz unmodulated)
  - 50MHz (modulated),  $\pm 1\%$  centre spread
- Modulation rate: 39KHz.
- Spread Spectrum ON/OFF control
- Supply voltage range  $2.5V \pm 5\%$ .
- Available in 8-Pin SOIC package.

### Product Description

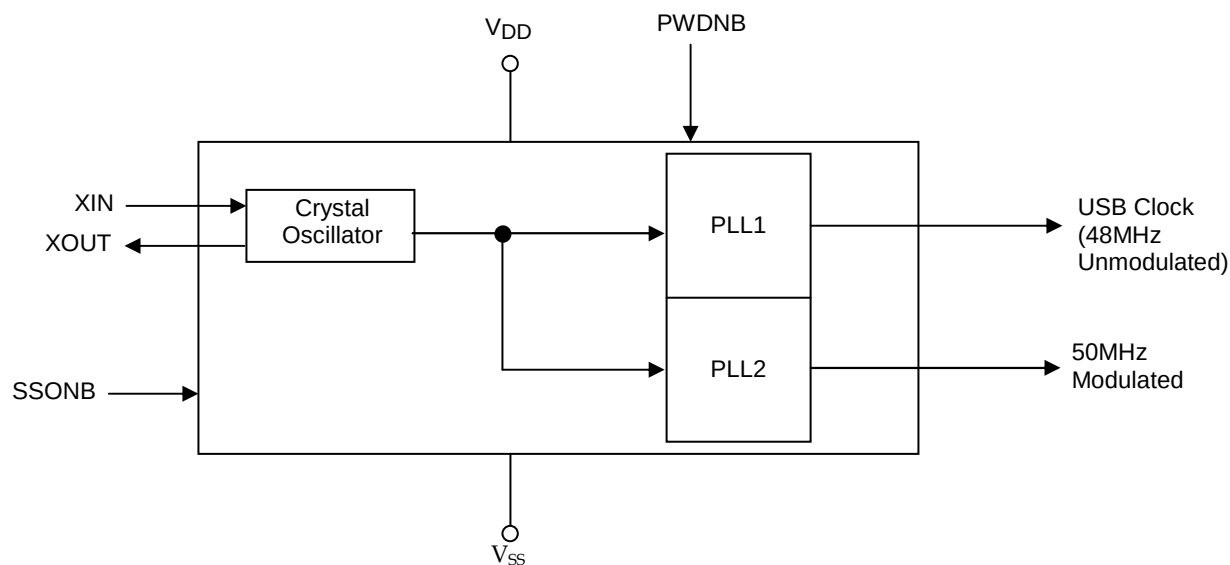
The ASM3P2853A is a versatile spread spectrum frequency modulator. The ASM3P2853A reduces electromagnetic interference (EMI) at the clock source. The ASM3P2853A allows significant system cost savings

by reducing the number of circuit board layers and shielding that are required to pass EMI regulations. The ASM3P2853A modulates the output of PLL in order to spread the bandwidth of a synthesized clock, thereby decreasing the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal's bandwidth is called spread spectrum clock generation.

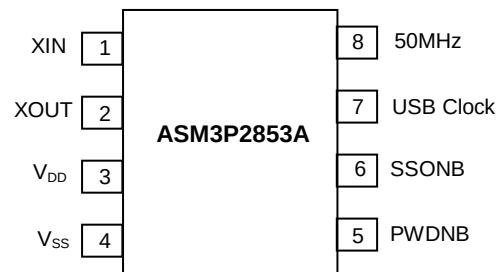
### Applications

ASM3P2853A is targeted towards EMI management for high speed digital applications such as PC peripheral devices, consumer electronics and embedded controller systems.

### Block Diagram



## Pin Configuration



## Pin Description

| Pin# | Pin Name        | Type | Description                                                                                                                                                                 |
|------|-----------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1    | XIN             | I    | Connection to crystal or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock. |
| 2    | XOUT            | O    | Connection to crystal. If using an external reference clock, this pin must be left unconnected.                                                                             |
| 3    | V <sub>DD</sub> | P    | Power supply for the analog and digital blocks.                                                                                                                             |
| 4    | V <sub>SS</sub> | P    | Ground to entire chip.                                                                                                                                                      |
| 5    | PWDNB           | I    | Power-down control pin. Pull low to enable the power-down mode. Connect to VDD, if not used.                                                                                |
| 6    | SSONB           | I    | Digital logic input used to enable spread spectrum function (Active LOW). Spread spectrum is enabled when LOW, disabled when HIGH.                                          |
| 7    | USB Clock       | O    | Clock output-1 (48MHz unmodulated).                                                                                                                                         |
| 8    | 50MHz           | O    | Clock output-2 (50MHz modulated).                                                                                                                                           |

## Absolute Maximum Ratings

| Symbol                                                                                                                                                                        | Parameter                                             | Rating       | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|--------------|------|
| VDD, VIN                                                                                                                                                                      | Voltage on any pin with respect to Ground             | -0.5 to +4.6 | V    |
| TSTG                                                                                                                                                                          | Storage temperature                                   | -65 to +125  | °C   |
| Ts                                                                                                                                                                            | Max. Soldering Temperature (10 sec)                   | 260          | °C   |
| TJ                                                                                                                                                                            | Junction Temperature                                  | 150          | °C   |
| TDV                                                                                                                                                                           | Static Discharge Voltage (As per JEDEC STD22- A114-B) | 2            | KV   |
| Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability. |                                                       |              |      |

## Operating Conditions

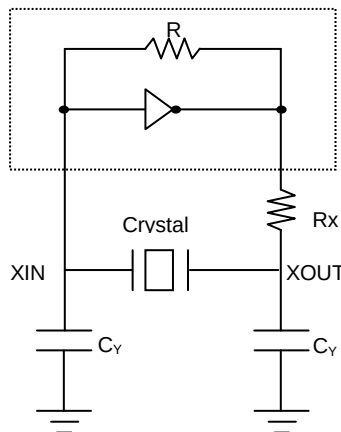
| Parameter                           | Symbol | Condition / Description | Min   | Typ | Max   | Unit |
|-------------------------------------|--------|-------------------------|-------|-----|-------|------|
| Supply Voltage                      | VDD    | 2.5V ± 5%               | 2.375 | 2.5 | 2.625 | V    |
| Ambient Operating Temperature Range | TA     |                         | -40   | -   | +85   | °C   |
| Crystal Resonator Frequency         | FXIN   |                         | 25    |     |       | MHz  |
| Output Driver Load Capacitance      | CL     |                         | -     | -   | 15    | pF   |

## Crystal Specifications

| Fundamental AT cut parallel resonant crystal |                          |
|----------------------------------------------|--------------------------|
| Nominal frequency                            | 25MHz                    |
| Frequency tolerance                          | ±50ppm or better at 25°C |
| Operating temperature range                  | -25°C to +85°C           |
| Storage temperature                          | -40°C to +85°C           |
| Load capacitance                             | 18pF                     |
| Shunt capacitance                            | 7pF maximum              |
| ESR                                          | 25Ω                      |

Note: CY is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

## Typical Crystal Interface Circuit



$$C_Y = 2 * (C_P - C_S),$$

Where CP = Load capacitance of crystal from crystal vendor datasheet

CS = Stray capacitance due to CIN, PCB, Trace etc.

## DC Electrical Characteristics

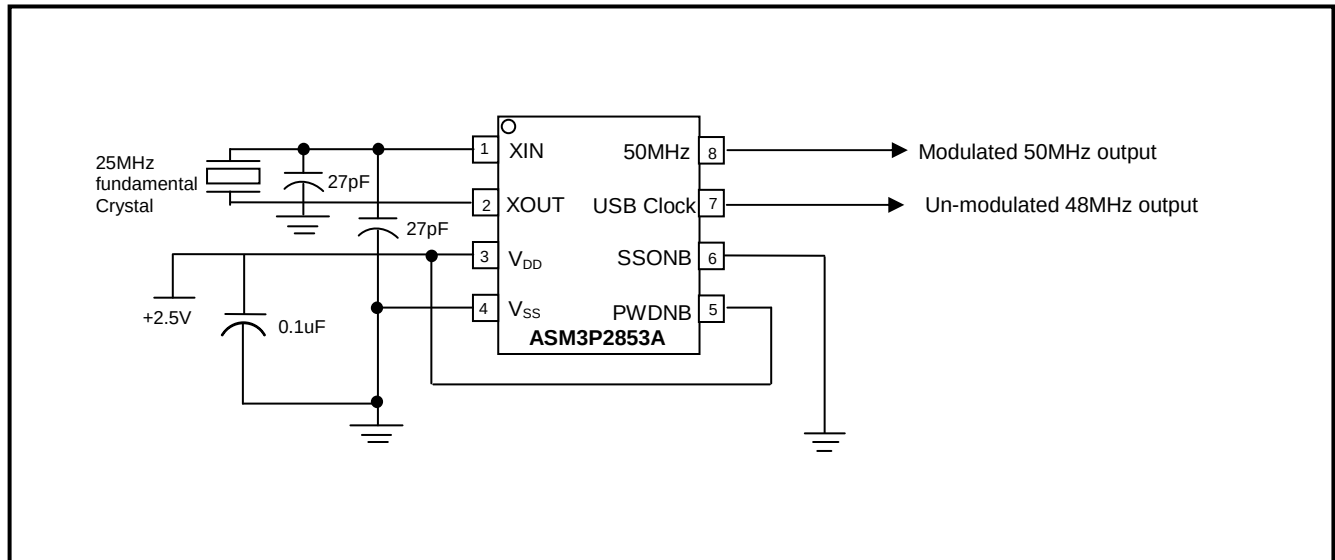
| Parameter                         | Symbol    | Conditions / Description                           | Min | Typ | Max | Unit     |
|-----------------------------------|-----------|----------------------------------------------------|-----|-----|-----|----------|
| <b>Overall</b>                    |           |                                                    |     |     |     |          |
| Supply Current, Dynamic           | $I_{DD}$  | $V_{DD} = 2.5V$ , $F_{XIN} = 25MHz$ , $C_L = 15pF$ | 7   | 13  | 20  | mA       |
| Supply Current, Static            | $I_{DDL}$ | $V_{DD} = 2.5V$ , $X_{IN} = 0$ , $PWDNB = 0$       | -   | 12  | -   | uA       |
| <b>All input pins</b>             |           |                                                    |     |     |     |          |
| High-Level Input Voltage          | $V_{IH}$  | $V_{DD} = 2.5V$                                    | 1.7 | -   | -   | V        |
| Low-Level Input Voltage           | $V_{IL}$  | $V_{DD} = 2.5V$                                    | -   | -   | 0.7 | V        |
| High-Level Input Current          | $I_{IH}$  |                                                    | -   | -   | 25  | $\mu A$  |
| Low-Level Input Current (pull-up) | $I_{IL}$  |                                                    | -   | -   | -25 | $\mu A$  |
| <b>Clock Outputs</b>              |           |                                                    |     |     |     |          |
| High-Level Output Source Current  | $I_{xOH}$ | $V_{DD} = 2.5V$ , $V(X_{IN}) = 0$ , $V_O = 2V$     | -   | -15 | -   | mA       |
| Low-Level Output Sink Current     | $I_{xOL}$ | $V_{DD} = V(X_{IN}) = 2.5V$ , $V_O = 0.4V$         | -   | 15  | -   | mA       |
| High-Level Output Source Current  | $I_{OH}$  | $V_O = 2V$                                         | -   | 8   | -   | mA       |
| Low-Level Output Sink Current     | $I_{OL}$  | $V_O = 0.4V$                                       | -   | 8   | -   | mA       |
| Output Impedance                  | $Z_O$     |                                                    | -   | 42  | -   | $\Omega$ |

## AC Electrical Characteristics

| Parameter               | Symbol   | Conditions / Description                                                                                    | Min | Typ | Max | Unit |
|-------------------------|----------|-------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| Rise Time <sup>1</sup>  | $t_r$    | Measured from 20% to 80% of the signal level                                                                | -   | 2   | -   | nS   |
| Fall Time <sup>1</sup>  | $t_f$    | Measured from 80% to 20% of the signal level                                                                | -   | 1.5 | -   | nS   |
| Jitter (Cycle-to-Cycle) | $t_{jc}$ |                                                                                                             | -   | 250 | -   | pS   |
| Jitter (Period)         | $t_p$    |                                                                                                             | -   | 175 | -   | pS   |
| Clock Duty Cycle        | $t_d$    | Ratio of pulse width (as measured from rising edge to next falling edge at $V_{DD}/2$ ) to one clock period | 45  | 50  | 55  | %    |

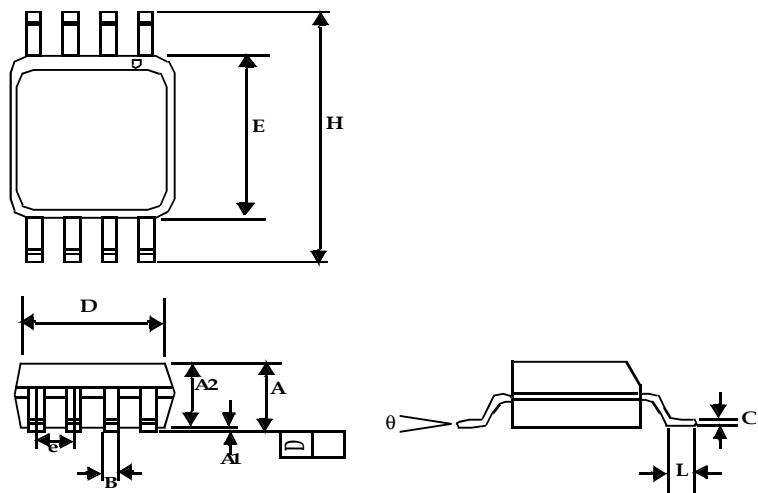
Note: 1.  $C_L = 15$  pF, Input clock frequency = 25MHz

## Typical Application Schematic using ASM3P2853A Device



Package Information

8-Pin SOIC package



| Symbol | Dimensions |       |             |      |
|--------|------------|-------|-------------|------|
|        | Inches     |       | Millimeters |      |
|        | Min        | Max   | Min         | Max  |
| A1     | 0.004      | 0.010 | 0.10        | 0.25 |
| A      | 0.053      | 0.069 | 1.35        | 1.75 |
| A2     | 0.049      | 0.059 | 1.25        | 1.50 |
| B      | 0.012      | 0.020 | 0.31        | 0.51 |
| C      | 0.007      | 0.010 | 0.18        | 0.25 |
| D      | 0.193 BSC  |       | 4.90 BSC    |      |
| E      | 0.154 BSC  |       | 3.91 BSC    |      |
| e      | 0.050 BSC  |       | 1.27 BSC    |      |
| H      | 0.236 BSC  |       | 6.00 BSC    |      |
| L      | 0.016      | 0.050 | 0.41        | 1.27 |
| θ      | 0°         | 8°    | 0°          | 8°   |

Coplanarity ≤ 4 mil

## Ordering Code

| Part number      | Marking | Package Configuration          | Temperature Range |
|------------------|---------|--------------------------------|-------------------|
| ASM3P2853AG-08SR | AEC     | 8-pin SOIC, TAPE & REEL, Green | 0°C to +70°C      |

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

Note: This product utilizes US Patent #6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003.

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