

## Multi-Output Custom Clock Generator

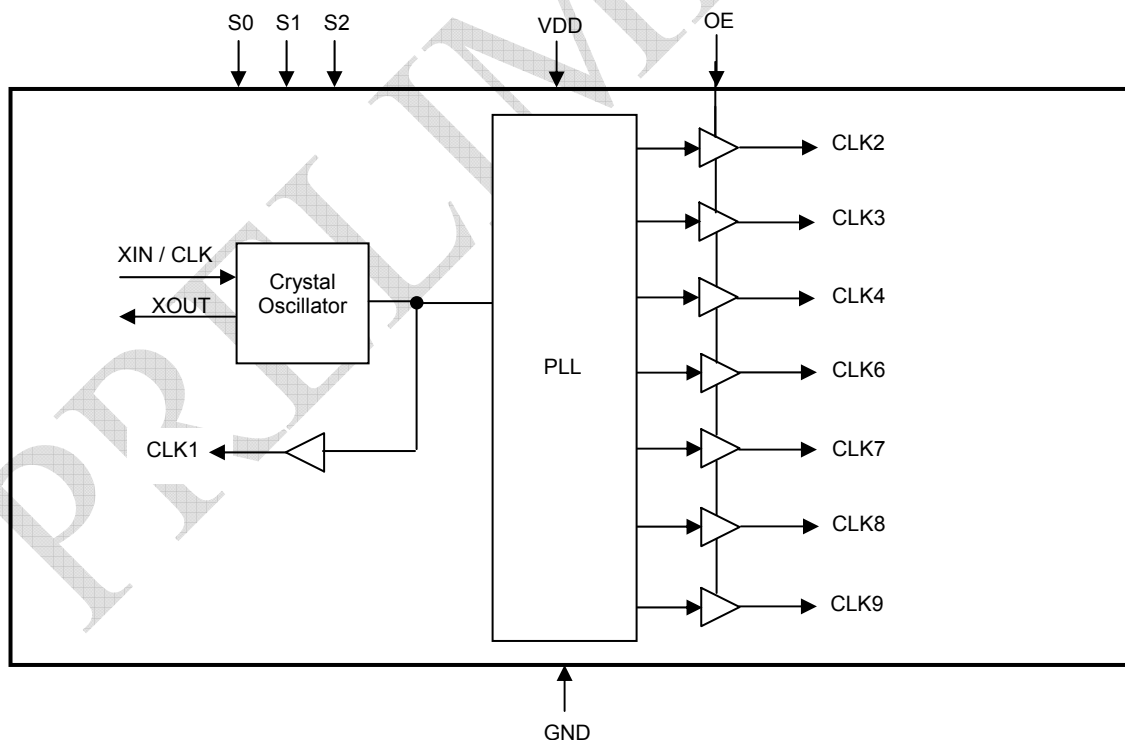
### Features

- Generates seven clock outputs from an inexpensive 20MHz crystal or external reference clock.
- Output Frequencies are selectable through select bits
- Generates an EMI optimized clock signal at the output.
- $\pm 1.5\%$  (Typ) Centre Spread for Spread Spectrum Clock Outputs
- Operates with a  $3.3V \pm 5\%$  Supply Voltage
- Available in 28-pin TSSOP.

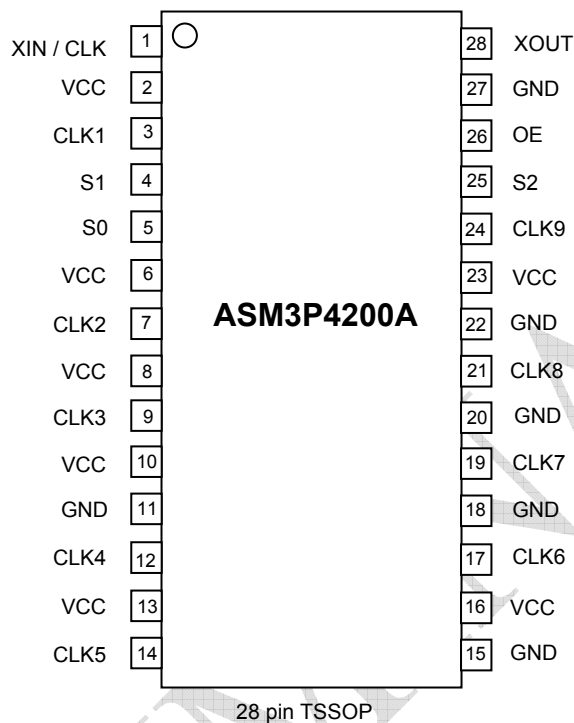
### Product Description

The ASM3P4200A is a versatile multi output custom clock generator. The seven high frequency Clock outputs are generated using an inexpensive 20MHz Crystal or external reference clock. The accuracy of the 20MHz Input Clock should be within  $\pm 50\text{ppm}$ . The output clocks consist of a low EMI spread spectrum clock and other non-spread clocks. Three Select bits choose the combination of Output Clock Frequency. Refer to the Output Frequency Selection Table for the values. The device operates from a Supply Voltage of  $3.3V \pm 5\%$  with a tolerable ripple voltage of 50mV. The device is available in a 28 pin TSSOP JEDEC package.

### Block Diagram



## Pin Assignment



## Output Frequency Selection Table

Selection Bits			CLK1 (MHz)	CLK2 (MHz)	CLK3 (MHz)	CLK4 (MHz)	CLK5 (MHz)	CLK6 (MHz)	CLK7 (MHz)	CLK8* (MHz)	CLK9* (MHz)
S2	S1	S0									
0	0	0	20	36.6	31.6	39.5	OFF	84	63	50	20
0	0	1	20	36.6	31.6	39.5	OFF	84	63	60	20
0	1	0	20	36.6	31.6	39.5	OFF	36	63	50	20
0	1	1	20	36.6	31.6	39.5	OFF	84	63	75	20
1	0	0	-	-	-	-	-	-	-	-	-
1	0	1	-	-	-	-	-	-	-	-	-
1	1	0	-	-	-	-	-	-	-	-	-
1	1	1	-	-	-	-	-	-	-	-	-

\* CLK8 and CLK9 are Spread Spectrum Clocks

### Pin Description

Pin #	Pin Name	Pin Type	Pin Description
1	XIN / CLK	Input	Crystal connection or external reference frequency input. It can be connected to a 20MHz Fundamental mode crystal or to an external reference clock.
2	VCC	Power	Connect to +3.3V.
3	CLK1	Output	Clock Output. Refer to the Output Frequency Selection Table for details.
4	S1	Input	Select Bit for Desired Output Frequency at different output pins. Refer to the Output Frequency Selection Table for details. Has an internal pull down resistor
5	S0	Input	Select Bit for Desired Output Frequency at different output pins. Refer to the Output Frequency Selection Table for details. Has an internal pull down resistor
6	VCC	Power	Connect to +3.3V.
7	CLK2	Output	Clock Output. Refer to the Output Frequency Selection Table for details.
8	VCC	Power	Connect to +3.3V.
9	CLK3	Output	Clock Output. Refer to the Output Frequency Selection Table for details.
10	VCC	Power	Connect to +3.3V.
11	GND	Power	Connect to ground.
12	CLK4	Output	Clock Output. Refer to the Output Frequency Selection Table for details.
13	VCC	Power	Connect to +3.3V.
14	CLK5	Output	Clock Output. Refer to the Output Frequency Selection Table for details.
15	GND	Power	Connect to ground.
16	VCC	Power	Connect to +3.3V.
17	CLK6	Output	Clock Output. Refer to the Output Frequency Selection Table for details.
18	GND	Power	Connect to ground.
19	CLK7	Output	Clock Output. Refer to the Output Frequency Selection Table for details.
20	GND	Power	Connect to ground.
21	CLK8	Output	Spread Spectrum Clock Output. Refer to the Output Frequency Selection Table for details.
22	GND	Power	Connect to ground.
23	VCC	Power	Connect to +3.3V.
24	CLK9	Output	Spread Spectrum Clock Output. Refer to the Output Frequency Selection Table for details.
25	S2	Input	Select Bit for Desired Output Frequency at different output pins. Refer to the Output Frequency Selection Table for details. Has an internal pull down resistor
26	OE	Input	Output Enable bit. When this pin is made HIGH, the output clocks are enabled. Has an Internal pull-up resistor
27	GND	Power	Connect to ground.
28	XOUT	Output	Crystal connection. If an external reference clock is used, this pin must be left unconnected.

### Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD	Power Supply Voltage relative to Ground	-0.5 to +4.6	V
V <sub>IN</sub>	Input Voltage relative to Ground (Input Pins)	-0.5 to VDD+0.3	
T <sub>STG</sub>	Storage temperature	-65 to +150	°C
T <sub>A</sub>	Operating temperature	-20 to +85	°C
T <sub>s</sub>	Max. Soldering Temperature (10 sec)	260	°C
T <sub>J</sub>	Junction Temperature	125	°C
T <sub>DV</sub>	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

rev 0.2

### DC Electrical Characteristics

(Test condition: All parameters are measured at room temperature (+ 25°C) unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>IL</sub>	Input low voltage	GND - 0.3	-	0.8	V
V <sub>IH</sub>	Input high voltage	2.0	-	VDD + 0.3	V
I <sub>IL</sub>	Input low current	-	-	-35	μA
I <sub>IH</sub>	Input high current	-	-	35	μA
I <sub>XOL</sub>	XOUT output low current (@0.4V, VDD=3.3V)	-	3	-	mA
I <sub>XOH</sub>	XOUT output high current (@2.5V, VDD=3.3V)	-	3	-	mA
V <sub>OL</sub>	Output low voltage (VDD = 3.3 V, I <sub>OL</sub> = 12mA)	-	-	0.4	V
V <sub>OH</sub>	Output high voltage (VDD = 3.3 V, I <sub>OH</sub> = 12mA)	2.5	-	-	V
I <sub>DD</sub>	Static supply current*	-	TBD	-	mA
I <sub>CC</sub>	Dynamic supply current (3.3V, 20MHz and no load)	-	TBD	-	mA
VDD	Operating Voltage	3.135	3.3	3.465	V
t <sub>ON</sub>	Power-up time (first locked cycle after power-up)**	-	-	5	mS
Z <sub>OUT</sub>	Output impedance	-	17	-	Ω

\* XIN / CLK and OE Pins are pulled low  
 \*\* VDD and XIN / CLK inputs are stable,

### AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
XIN / CLK	Input frequency	-	20	-	MHz
f <sub>d</sub>	Spread Percentage	-	±1.5	-	%
	Output Frequency = 20MHz (Pin 24)				
	Output Frequency = 50MHz				
	Output Frequency = 60MHz				
	Output Frequency = 75MHz				
t <sub>LH</sub> *	Output rise time (Measured from 0.8V to 2.0V)	-	-	1	nS
t <sub>HL</sub> *	Output fall time ( Measured from 2.0V to 0.8V)	-	-	1	nS
t <sub>JC</sub>	Jitter (Cycle to cycle)	-	±250	-	pS
t <sub>p</sub>	Jitter( Period)	-	±150	-	pS
t <sub>D</sub>	Output duty cycle	45	50	55	%

\*t<sub>LH</sub> and t<sub>HL</sub> are measured into a capacitive load of 30pF

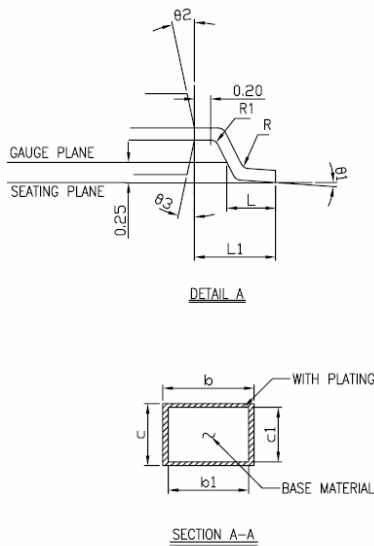
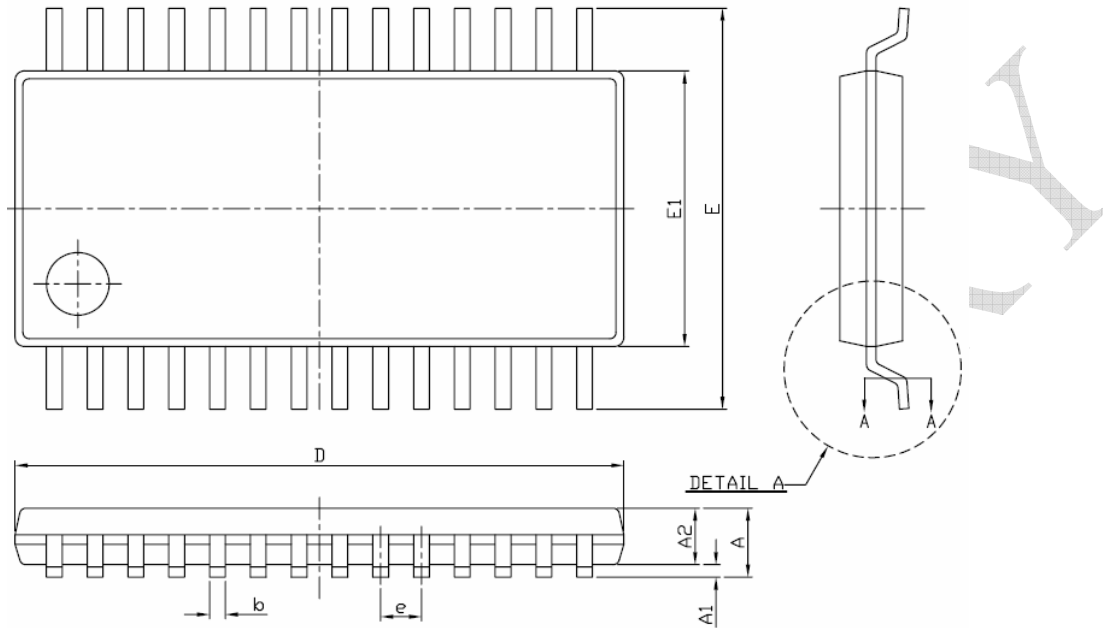
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**ASM3P4200A**

rev 0.2

**Package Information**

**28 lead Thin Shrunk Small Outline Package (4.40-MM Body) --- JEDEC Standard**



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	....	0.043	...	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.031	0.041	0.80	1.05
D	0.3779	0.3858	9.60	9.80
L	0.020	0.030	0.50	0.75
E	0.252 BSC		6.40 BSC	
E1	0.169	0.177	4.30	4.50
R	0.004	....	0.09	.....
R1	0.004	....	0.09	.....
b	0.007	0.012	0.19	0.30
b1	0.007	0.010	0.19	0.25
c	0.004	0.008	0.09	0.20
c1	0.004	0.006	0.09	0.16
L1	0.039 REF		1.0 REF	
e	0.026 BSC		0.65 BSC	
01	0°	8°	0°	8°
02	12° REF		12° REF	
03	12° REF		12° REF	

## Ordering Information

Part Number	Marking	Package	Temperature
ASM3P4200AG-28-TT	3P4200AG	28-Pin TSSOP, Tube, Green	Commercial
ASM3P4200AG-28-TR	3P4200AG	28-Pin TSSOP, Tape and Reel, Green	Commercial

## Device Ordering Information

ASM3P4200AG-28-TT

OR – TSOT23 -6, T/R  
 TT – TSSOP, TUBE  
 TR – TSSOP, T/R  
 VT – TVSOP, TUBE  
 VR – TVSOP, T/R  
 ST – SOIC, TUBE  
 AR – SSOP, T/R  
 AT – SSOP, TUBE  
 SR – SOIC, T/R  
 QR – QFN, T/R  
 QT – QFN, TRAY  
 BT – BGA, TRAY  
 BR – BGA, T/R  
 UR – SOT-23, T/R  
 DR – QSOP, T/R  
 DT – QSOP, TUBE

PIN COUNT

GREEN PACKAGE

PART NUMBER

X = Automotive (-40C to +125C)    I = Industrial (-40C to +85C)    P or n/c = Commercial (0C to +70C)

1 – reserved    6 – power management  
 2 – Non PLL based    7 – power management  
 3 – EMI Reduction    8 – power management  
 4 – DDR support products    9 – Hi performance  
 5 – STD Zero Delay Buffer    0 – reserved

PulseCore Semiconductor Mixed Signal Product



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Part Numbers: ASM3P4200A  
Document Version: 0.2

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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