

Multi-Output Custom Clock Generator

Features

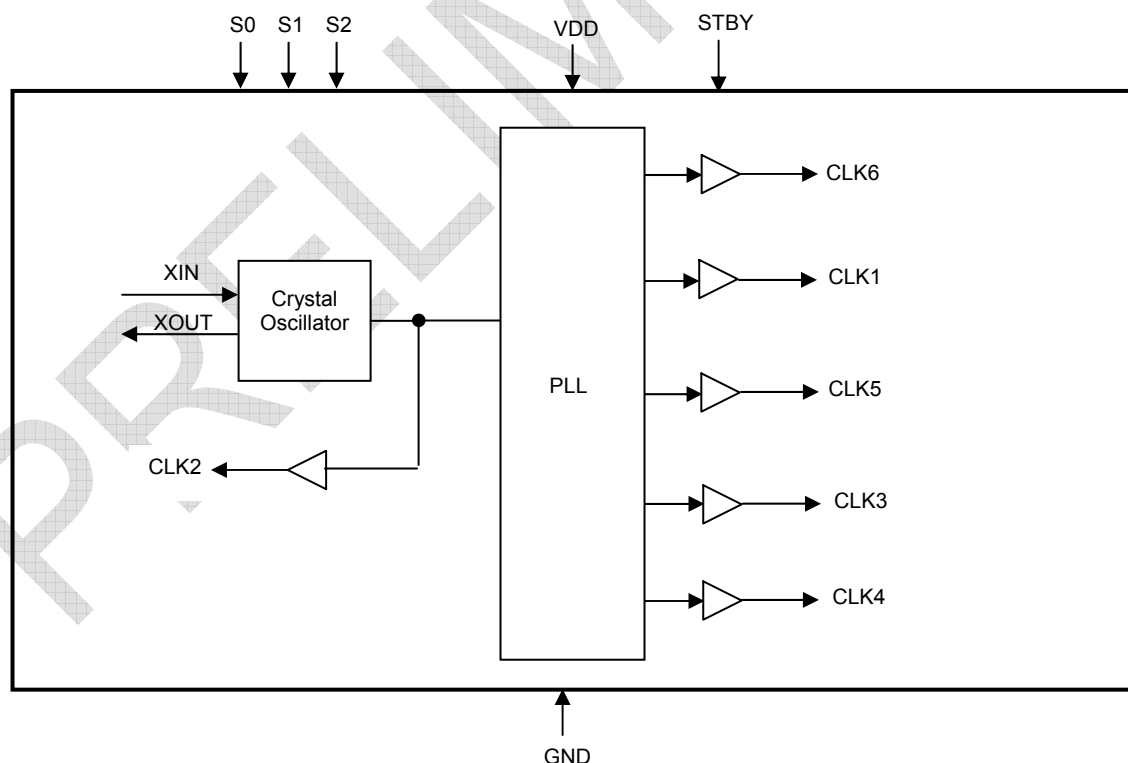
- Generates five clock outputs from an inexpensive 20MHz crystal or external reference clock.
- Output Frequencies are selectable through select bits
- Generates an EMI optimized clock signal at the output.
- $\pm 1.5\%$ (Typ) Centre Spread for Spread Spectrum Clock Outputs
- Operates with a $3.3V \pm 0.3V$ Supply Voltage
- Output Clocks disable feature using STBY pin
- Available in 20-pin TSSOP.

clock generator. The five high frequency Clock outputs are generated using an inexpensive 20MHz Crystal or external reference clock. The accuracy of the 20MHz Input Clock should be within $\pm 50\text{ppm}$. The output clocks consist of a low EMI spread spectrum clock and other non-spread clocks. Three Select bits choose the combination of Output Clock Frequency. Refer to the Output Frequency Selection Table for the values. Output clocks can be disabled using the STBY pin. The device operates from a Supply Voltage of $3.3V \pm 0.3V$ with a tolerable ripple voltage of 50mV. The device is available in a 20 pin TSSOP JEDEC package.

Product Description

The ASM3P4201A is a versatile multi output custom

Block Diagram

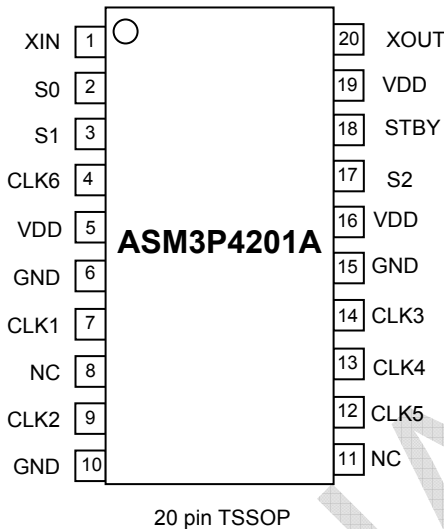


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Pin Assignment



Pin Description

| Pin # | Pin Name | Pin Type | Pin Description |
|-------|----------|----------|---|
| 1 | XIN | Input | Crystal connection or external reference frequency input. It can be connected to a 20MHz Fundamental mode crystal or to an external reference clock. |
| 2 | S0 | Input | Select Bit for Desired Output Frequency at different output pins. Refer to the Output Frequency Selection Table for details. Has an internal pull down resistor |
| 3 | S1 | Input | Select Bit for Desired Output Frequency at different output pins. Refer to the Output Frequency Selection Table for details. Has an internal pull down resistor |
| 4 | CLK6 | Output | Clock Output. Refer to the Output Frequency Selection Table for details. |
| 5 | VDD | Power | Connect to +3.3V. |
| 6 | GND | Power | Connect to ground. |
| 7 | CLK1 | Output | Clock Output. Refer to the Output Frequency Selection Table for details. |
| 8 | NC | - | No connect |
| 9 | CLK2 | Output | Clock Output. Refer to the Output Frequency Selection Table for details. |
| 10 | GND | Power | Connect to ground. |
| 11 | NC | - | No connect |
| 12 | CLK5 | Output | Clock Output. Refer to the Output Frequency Selection Table for details. |
| 13 | CLK4 | Output | Spread Spectrum Clock Output. Refer to the Output Frequency Selection Table for details. |
| 14 | CLK3 | Output | Spread Spectrum Clock Output. Refer to the Output Frequency Selection Table for details. |
| 15 | GND | Power | Connect to ground. |
| 16 | VDD | Power | Connect to +3.3V. |
| 17 | S2 | Input | Select Bit for Desired Output Frequency at different output pins. Refer to the Output Frequency Selection Table for details. Has an internal pull down resistor |
| 18 | STBY | Input | When this pin is made is HIGH, all the output clocks are enabled. |
| 19 | VDD | Power | Connect to +3.3V. |
| 20 | XOUT | Output | Crystal connection. If an external reference clock is used, this pin must be left unconnected. |

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Output Frequency Selection Table

| Selection Bits | | | CLK1 (MHz) | CLK2 (MHz) | CLK3* (MHz) | CLK4* (MHz) | CLK5 (MHz) | CLK6 (MHz) |
|----------------|----|----|------------|------------|-------------|-------------|------------|------------|
| S2 | S1 | S0 | | | | | | |
| 0 | 0 | 0 | 39.5 | 20 | 65 | 20 | 84 | 36.6 |
| 0 | 0 | 1 | 39.5 | 20 | 60 | 20 | 84 | 36.6 |
| 0 | 1 | 0 | 39.5 | 20 | 50 | 20 | 36 | 36.6 |
| 0 | 1 | 1 | 39.5 | 20 | 75 | 20 | 84 | 36.6 |

* CLK3 and CLK4 are Spread Spectrum Clocks

Absolute Maximum Ratings

| Symbol | Parameter | Rating | Unit |
|------------------|--|-----------------|------|
| VDD | Power Supply Voltage relative to Ground | -0.5 to +4.6 | V |
| V _{IN} | Input Voltage relative to Ground (Input Pins) | -0.5 to VDD+0.3 | |
| T _{STG} | Storage temperature | -65 to +150 | °C |
| T _A | Operating temperature | -20 to +85 | °C |
| T _s | Max. Soldering Temperature (10 sec) | 260 | °C |
| T _J | Junction Temperature | 125 | °C |
| T _{DV} | Static Discharge Voltage (As per JEDEC STD22- A114-B) | 2 | KV |

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

DC Electrical Characteristics

(Test condition: All parameters are measured at room temperature (+ 25°C) unless otherwise stated)

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------|---|-----------|-----|-----------|------|
| V _{IL} | Input low voltage | GND - 0.3 | - | 0.8 | V |
| V _{IH} | Input high voltage | 2.0 | - | VDD + 0.3 | V |
| I _{IL} | Input low current | - | - | -35 | μA |
| I _{IH} | Input high current | - | - | 35 | μA |
| I _{XOL} | XOUT output low current (V _{XOL} @0.4V, VDD=3.3V) | - | 3 | - | mA |
| I _{XOH} | XOUT output high current (V _{XOH} @2.5V, VDD=3.3V) | - | 3 | - | mA |
| V _{OL} | Output low voltage (VDD = 3.3V, I _{OL} =12mA) | - | - | 0.4 | V |
| V _{OH} | Output high voltage (VDD = 3.3V, I _{OH} =12mA) | 2.5 | - | - | V |
| I _{DD} | Static supply current* | - | TBD | - | mA |
| I _{CC} | Dynamic supply current (VDD =3.3V) | - | TBD | - | mA |
| VDD | Operating Voltage | 3.0 | 3.3 | 3.6 | V |
| t _{ON} | Power-up time (first locked cycle after power-up)** | - | - | 5 | mS |
| Z _{OUT} | Output impedance | - | 17 | - | Ω |

* XIN and STBY Pins are pulled low
 ** VDD and XIN input are stable,

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AC Electrical Characteristics

| Symbol | Parameter | | Min | Typ | Max | Unit |
|--|--|----------------------------------|-----|------|-----|------|
| CLKIN | Input frequency | | - | 20 | - | MHz |
| f _d | Spread Percentage | Output Frequency =20MHz (Pin 13) | - | ±1.5 | - | % |
| | | Output Frequency = 50MHz | | | | |
| | | Output Frequency = 60MHz | | | | |
| | | Output Frequency = 65MHz | | | | |
| | | Output Frequency = 75MHz | | | | |
| t _{LH} * | Output rise time (Measured from 0.8V to 2.0V) | | - | - | 1 | nS |
| t _{HL} * | Output fall time (Measured from 2.0V to 0.8V) | | - | - | 1 | nS |
| t _{JC} | Jitter (Cycle to cycle) | | - | ±250 | - | pS |
| t _p | Jitter(Period) | | - | ±150 | - | pS |
| t _D | Output duty cycle | | 45 | 50 | 55 | % |
| *t _{LH} and t _{HL} are measured into a capacitive load of 30pF | | | | | | |

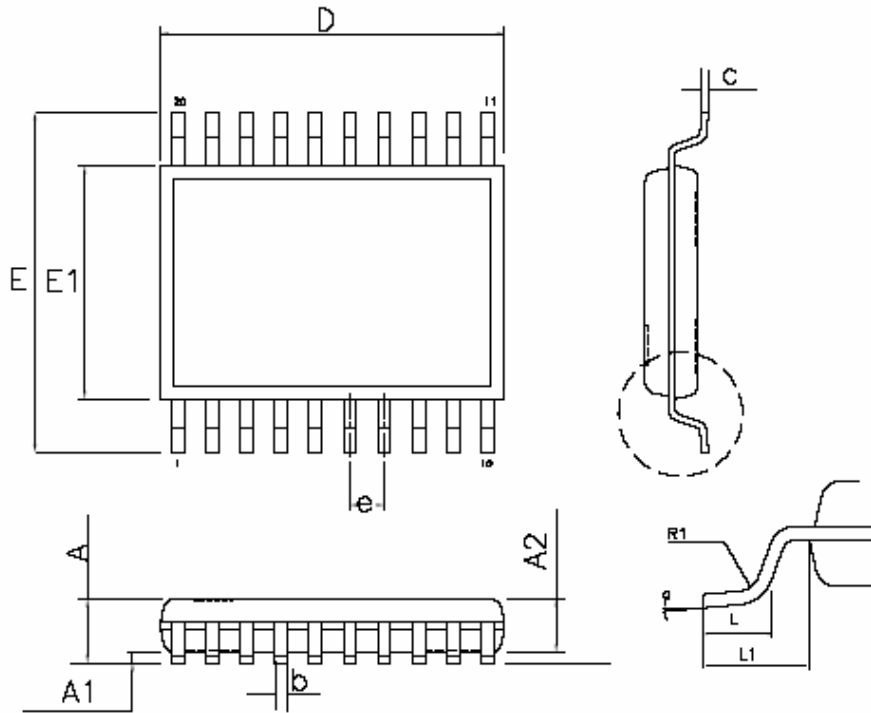
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Package Information

20-lead Thin Shrunk Small Outline Package (4.40-MM Body) – JEDEC Standard



| Symbol | Dimensions | | | |
|--------|------------|--------|-------------|-------|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | | 0.043 | ... | 1.2 |
| A1 | 0.0020 | 0.0059 | 0.05 | 0.15 |
| A2 | 0.031 | 0.041 | 0.80 | 1.05 |
| D | 0.252 | 0.26 | 6.40 | 6.60 |
| L | 0.020 | 0.030 | 0.50 | 0.75 |
| E | 0.252 BSC | | 6.40 BSC | |
| E1 | 0.169 | 0.177 | 4.30 | 4.50 |
| R1 | 0.004 | | 0.09 | |
| b | 0.007 | 0.012 | 0.19 | 0.30 |
| c | 0.004 | 0.008 | 0.09 | 0.20 |
| L1 | 0.039 REF | | 1.0 REF | |
| e | 0.026 BSC | | 0.65 BSC | |
| a | 0° | 8° | 0° | 8° |

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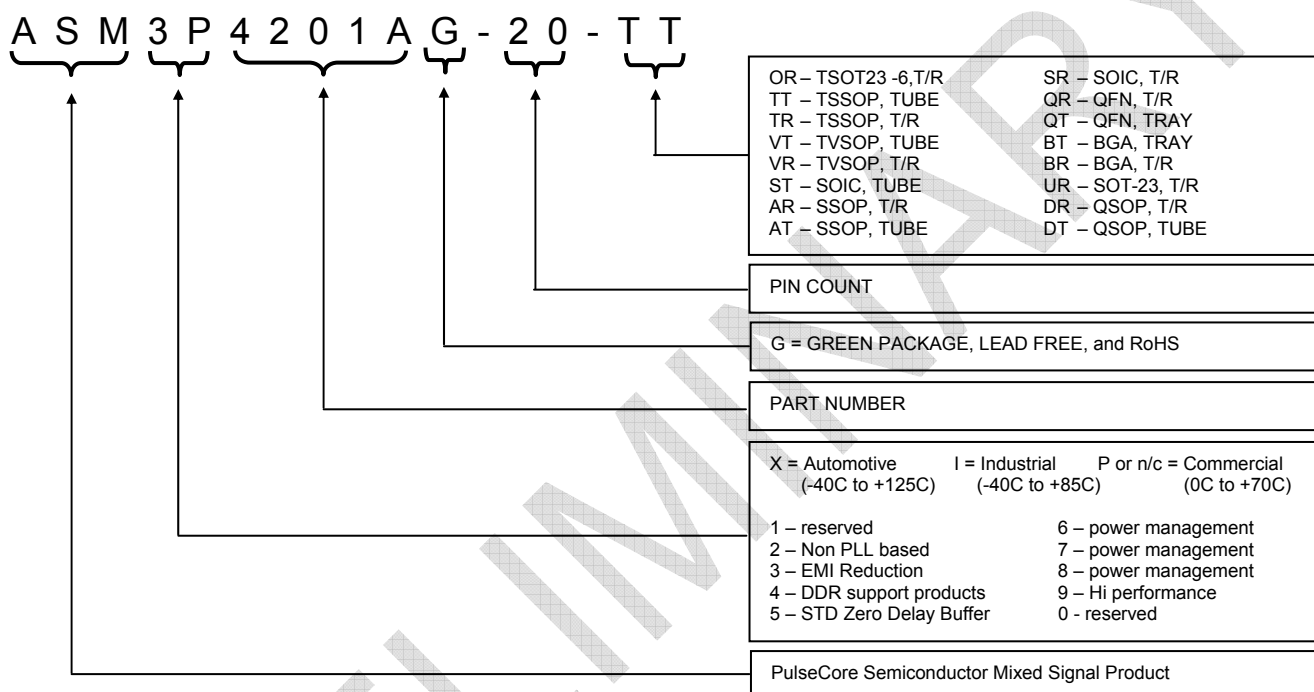
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Ordering Information

| Part Number | Marking | Package | Temperature |
|-------------------|----------|------------------------------------|-------------|
| ASM3P4201AG-28-TT | 3P4201AG | 20-Pin TSSOP, Tube, Green | Commercial |
| ASM3P4201AG-28-TR | 3P4201AG | 20-Pin TSSOP, Tape and Reel, Green | Commercial |

Device Ordering Information



Licensed under US patent Nos 5,488,627 and 5,631,920



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Part Numbers: ASM3P4201A
Document Version: 0.2

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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