Features

- **Organized as 2M x 8 bits**
- **Single 3.3V Power Supply**
- **Stacks of 16 SRAM 128K x AT65609E Die**
- **Access Time: 40 ns read, 35 ns write**
- **Very Low Power Consumption**
  - **Active: 130 mW (Typ)**
  - **Standby: 1 mW (Typ)**
- **TTL-Compatible Inputs and Outputs**
- **Die Designed on 0.35 Micron Process**
- **No Single Event Latch-up below a LET Threshold of 80 MeV/mg/cm^2**
- **Tested up to a Total Dose of 200 krads (Si) according to MIL STD 883 Method 1019**
- **Wide Temperature Range -55°C to +125°C**
- **Built by 3D+ company, using 3D+ Die Stacking Technology and Tested by Atmel**

Description

The AT61162E is a Rad Hard module, highly-integrated and very low-power CMOS static RAM organized as 2M x 8 bits. It is organized with 16 banks of 1 Mbit. Each bank has a 8-bit interface and is selected with 16 specific $\overline{CS}$: 0 - 15. Banks are selectable by pairs with 8 specific BS: 0 - 7.

This module takes full benefit of the 3D+ cube technology, and it is assembled by 3D+ and tested by Atmel, using Atmel 65609E 1-Mbit SRAM die: it is built with 8 layers, each one housing 2 dies. 10 nF decoupling capacitors are embedded for each memory die.

This module brings the solution to applications where fast computing is as mandatory as low power consumption, for example: space electronics, portable instruments, or embarked systems.

AT61162E is processed according to the methods of the latest revision of the MIL PRF 38535, QML N (QML Q counterpart for plastic).

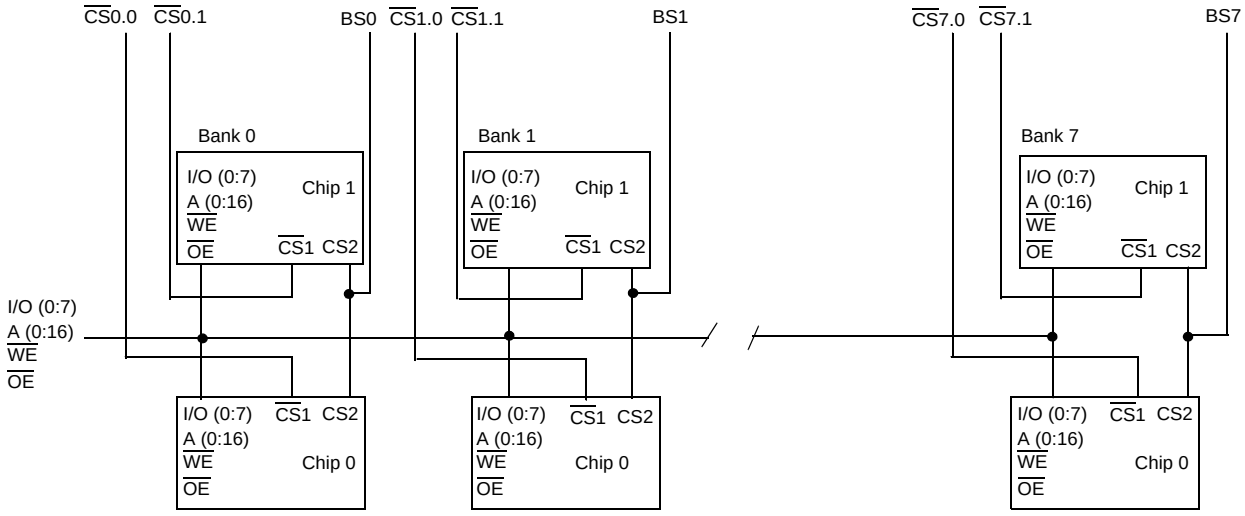
The package is a 64 gull wing pins dual in line, 11 mm wide, 28 mm long and 14.3 mm height and 0.8 mm pin pitch.

Rad Hard 2-Mbit x 8 SRAM Cube

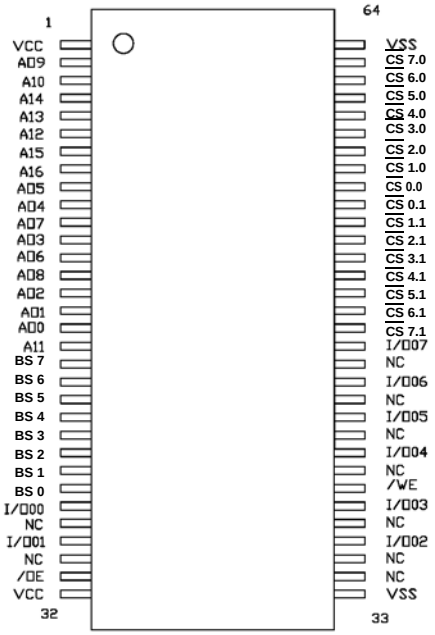
AT61162E

4157E–AERO–07/05

Block Diagram



Pin Configuration



Pin Description

Pin Name	Function
AO - A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$ 0.0 - $\overline{CS}$ 7.1	Chip Select 1
BS0 - BS7	Chip Select 2
I/O0 - I/O7	Data Inputs/Outputs
V_{CC}	3.3V Power
GND	Ground
NC	No Connection

Truth Table

$\overline{CS}_{x.x}$	BS_x	$\overline{WE}$	$\overline{OE}$	Inputs/ Outputs	Mode
All $\overline{CS}$ H	–	–	–	Z	Deselect/ Power-down
–	All BS L	–	–	Z	Deselect/ Power-down
$\overline{CS}$ y.z: L Other $\overline{CS}$: H	BSy: H Other BS: –	H	L	Data out	Read (Bank y.z selected)
$\overline{CS}$ y.z: L $\overline{CS}$ y.w: H Other $\overline{CS}$: –	BSy: H Other BS: L				
$\overline{CS}$ y.z: L Other $\overline{CS}$: H	BSy: H Other BS: –	L	–	Data in	Write (Bank y.z selected)
$\overline{CS}$ y.z: L $\overline{CS}$ y.w: H Other $\overline{CS}$: –	BSy: H Other BS: L				
$\overline{CS}$ y.z: L Other $\overline{CS}$: H	BSy: H Other BS: –	H	H	Z	Output Disable
$\overline{CS}$ y.z: L $\overline{CS}$ y.w: H Other $\overline{CS}$: –	BSy: H Other BS: L				

Electrical Characteristics

Absolute Maximum Ratings*

Supply Voltage to GND Potential	0.5 to +5V
DC Input Voltage GND	GND -0.3 to V_{CC}0.3V
DC Output Voltage high-Z-State GND	GND -0.3 to V_{CC}+0.3V
Storage Temperature	-65 to +150°C
Output Current into Outputs (Low)	20 mA
Electro Statics Discharge Voltage (MIL STD 883D method 3015.3)	>1000V

*Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

	Operating Temperature	Operating Voltage
Military	-55°C to 125°C	3.3V ± 0.3V

Recommended DC Operating Conditions

Parameter	Description	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3	3.3	3.6	V
Gnd	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	GND-0.3	0.0	0.8	V

DC Parameters

Parameter	Description	Min	Typ	Max	Unit
I_{IX} (1)	Input Leakage Current	-10	-	10	µA
I_{OZ} (1)	Output Leakage Current	-10	-	10	µA
V_{OL} (2)	Output Low Voltage	-	-	0.4	V
V_{OH} (3)	Output High Voltage	2.4	-	-	V

1. Gnd < V_{IN} < V_{CC}, Gnd < V_{OUT} < V_{CC} Output Disabled.
2. V_{CC} min. IOL = 4 mA.
3. V_{CC} min. IOH = -2 mA.

Consumption

Symbol	Description	61162E	Unit	Value
ICCSB (1)	Standby Supply Current	24	mA	max
$ICCSB_1$ (2)	Standby Supply Current	16	mA	max
ICCOP (3)	Dynamic Operating Current	60	mA	max

1. $\overline{CS}_{0.0}$ - $\overline{CS}_{7.1} \geq V_{IH}$ or BS_0 - BS7 $\leq V_{IL}$ and $\overline{CS}_{0.0}$ - $\overline{CS}_{7.1} \leq V_{IL}$.
2. $\overline{CS}_{0.0} \geq V_{CC}$ - 0.3V or, BS_0 - BS7 < Gnd + 0.3V and $\overline{CS}_{0.0}$ - $\overline{CS}_{7.1} \leq$ 0.2V
3. One bank active (F = $1/T_{AVAV}$, I_{OUT} = 0 mA, $\overline{W}$ = $\overline{OE}$ = V_{IH}, V_{IN} = Gnd/V_{CC}, V_{CC} max.), other banks stand by TTL (note 1) or CMOS (note 2).

Write Cycle

Symbol	Parameter	61162E	Unit	Value
t_{AVAW}	Write cycle time	35	ns	min
t_{AVWL}	Address set-up time	0	ns	min
t_{AVWH}	Address valid to end of write	25	ns	min
t_{DVWH}	Data set-up time	20	ns	min
t_{E1LWH}	$\overline{CS}_1$ low to write end	30	ns	min
t_{E2HWH}	CS_2 high to write end	30	ns	min
t_{WLQZ}	Write low to high-Z (1)	10	ns	max
t_{WLWH}	Write pulse width	30	ns	min
t_{WHAX}	Address hold from to end of write	+3	ns	min
t_{WHDX}	Data hold time	0	ns	min
t_{WHQX}	Write high to low-Z (1)	0	ns	min

Note: 1. Parameters guaranteed, not tested, with output loading 5 pF (see 1b in Figure: AC Test Loads Waveforms).

Read Cycle

Symbol	Parameter	61162E	Unit	Value
t_{AVAV}	Read cycle time	40	ns	min
t_{AVQV}	Address access time	40	ns	max
t_{AVQX}	Address valid to low-Z	3	ns	min
t_{E1LQV}	Chip-select$_1$ access time	40	ns	max
t_{E1LQX}	$\overline{CS}_1$ low to low-Z (1)	3	ns	min
t_{E1HQZ}	$\overline{CS}_1$ high to high-Z (1)	15	ns	max
t_{E2HQV}	Chip-select$_2$ access time	40	ns	max
t_{E2HQX}	CS_2 high to low-Z (1)	3	ns	min
t_{E2LQZ}	CS_2 low to high-Z (1)	15	ns	max
t_{GLQV}	Output Enable access time	15	ns	max
t_{GLQX}	$\overline{OE}$ low to low-Z (1)	0	ns	min
t_{GHQZ}	$\overline{OE}$ high to high-Z (1)	10	ns	max

Note: 1. Parameters guaranteed, not tested, with output loading 5 pF (see 1b in page Figure: AC Test Loads Waveforms).

AC Parameters

AC Test Conditions

Input Pulse Levels: ..... GND to 3.0V

Input Timing Reference Levels: 1.5V

Output Loading I_{OL}/I_{OH} (see figures 1a and 1b)..... +30 pF

Rise and Fall times:

Capacities, combined with current levels, impact on rise and fall times.

The following table summarizes capacitance values (in pF), determined at 50Ω.

$\overline{CS}_{x.x}$	BS_x	$\overline{WE}$ / $\overline{OE}$ / Address Inputs	Data Inputs / Outputs
12	20	130	160

AC Test Loads Waveforms

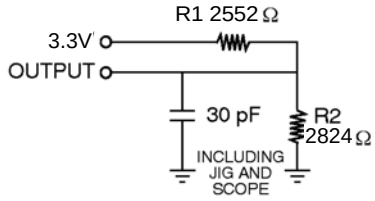


Figure 1a

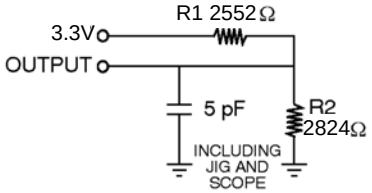


Figure 1b

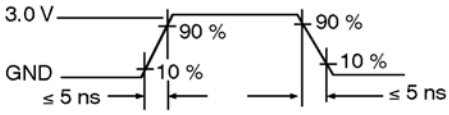
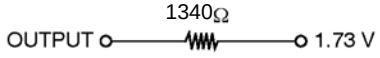


Figure 2

Equivalent to : THEVENIN EQUIVALENT

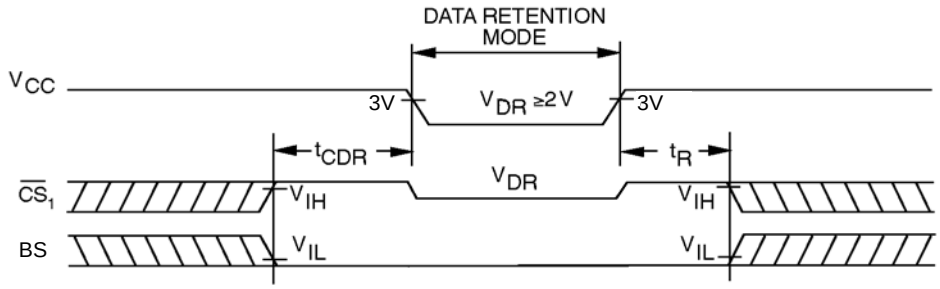


Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. During data retention $\overline{CS}$ must be held high within V_{CC} to V_{CC} -0.2V or, chip select BS must be held down within GND to GND +0.2V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power up and power down transitions $\overline{CS}$ and $\overline{OE}$ must be kept between V_{CC} + 0.3V and 70% of V_{CC}, or with BS between GND and GND -0.3V.
4. The RAM can begin operation > TR ns after V_{CC} reaches the minimum operation voltages (3V).

Timing



Data Retention Characteristics

Parameter	Description	Min	Typical T_A = 25°C	Max	Unit
V_{CCDR}	V_{CC} for data retention	2.0	–	–	V
t_{CDR}	Chip deselect to data retention time	0.0	–	–	ns
t_R	Operation recovery time	t_{AVAV}(1)	–	–	ns
I_{CCDR1}(2)	Data retention current at 2.0V	–	0.040	12	mA

Notes: 1. T_{AVAV} = Read Cycle Time

2. All $\overline{CS}$ = V_{CC} or All BS = $\overline{CS}$ = GND, V_{IN} = Gnd/V_{CC}.

Figure 1. Write Cycle 1. $\overline{W}$ Controlled, $\overline{OE}$ High During Write

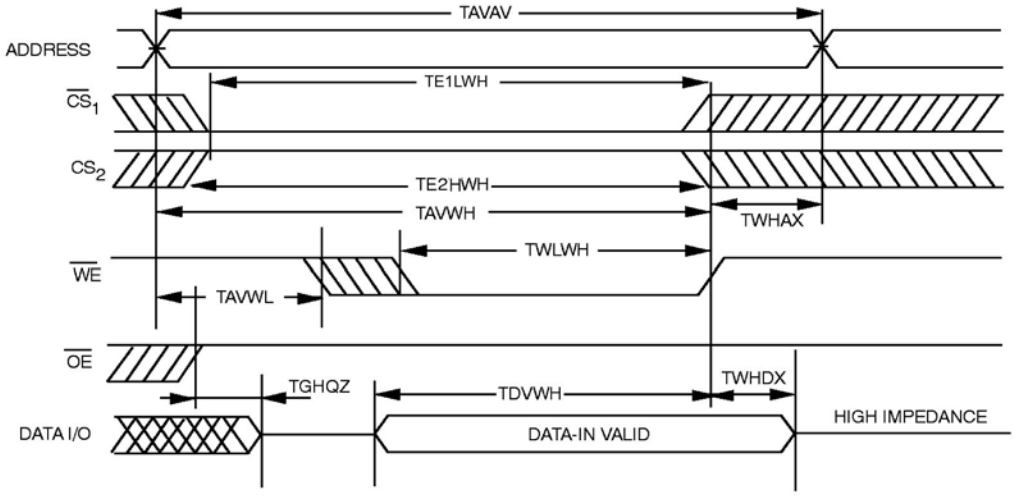


Figure 2. Write Cycle 2. $\overline{W}$ Controlled, $\overline{OE}$ Low

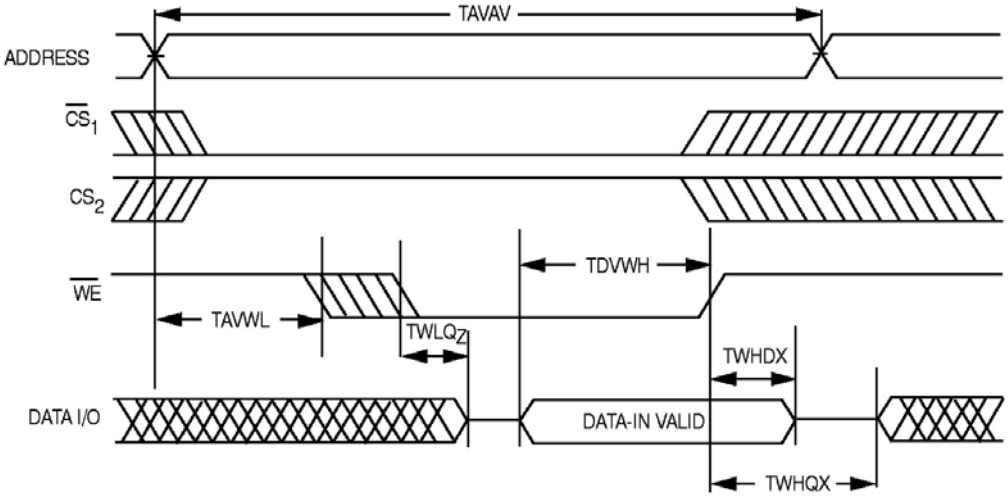
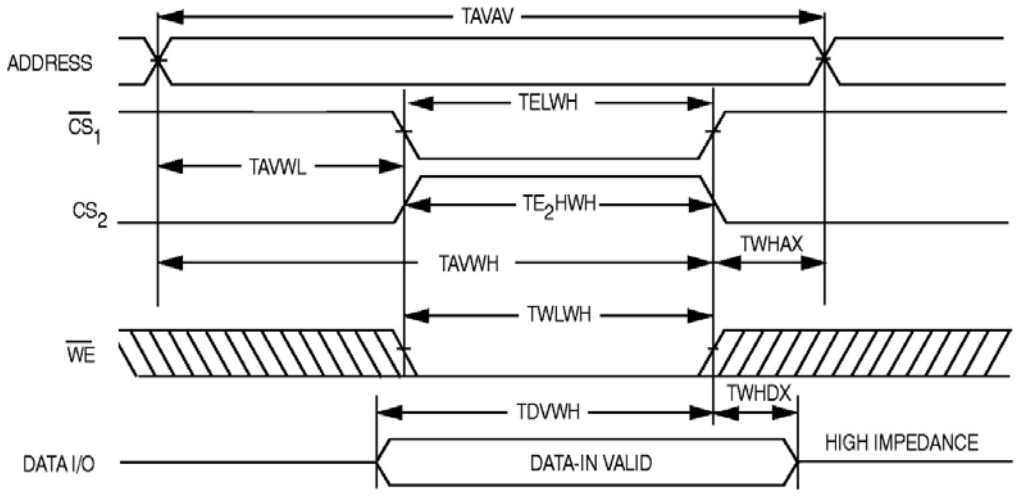


Figure 3. Write Cycle 3. $\overline{CS}$1 or CS2 Controlled



Note: The internal write time of the memory is defined by the overlap of CS_1 Low and CS_2 HIGH and $\overline{WE}$ LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in actived. The data input setup and hold timing should be referenced to the activated edge of the signal that terminates the write. Data out is high impedance if $\overline{OE}$ = V_{IH}.

Figure 4. Read Cycle nb 1

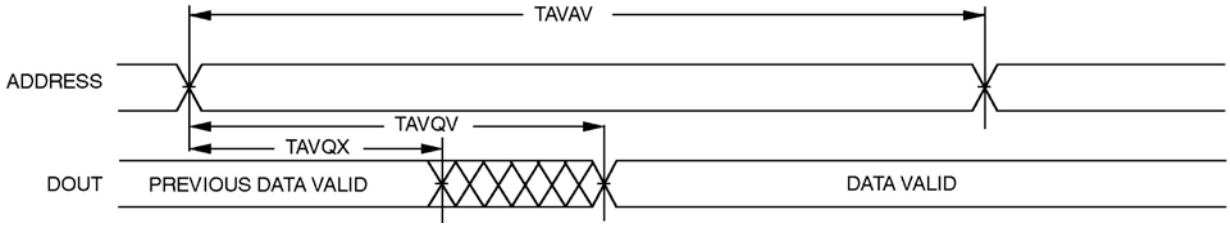


Figure 5. Read Cycle nb 2

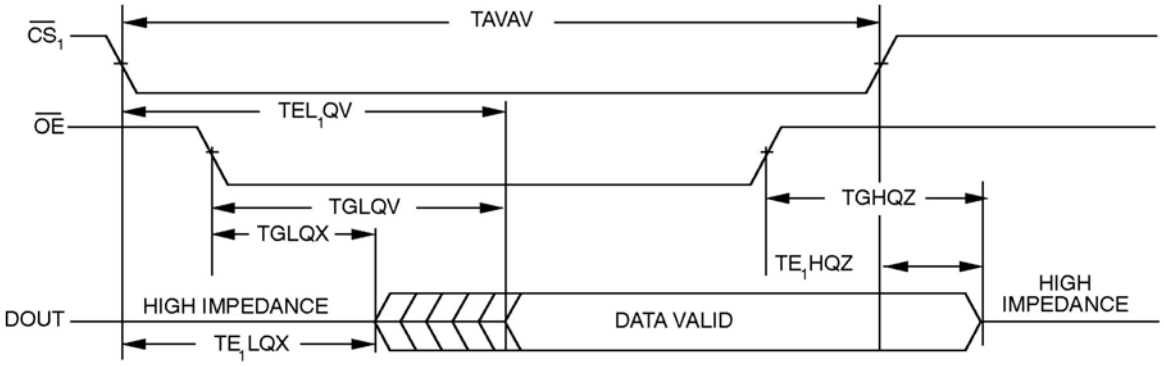
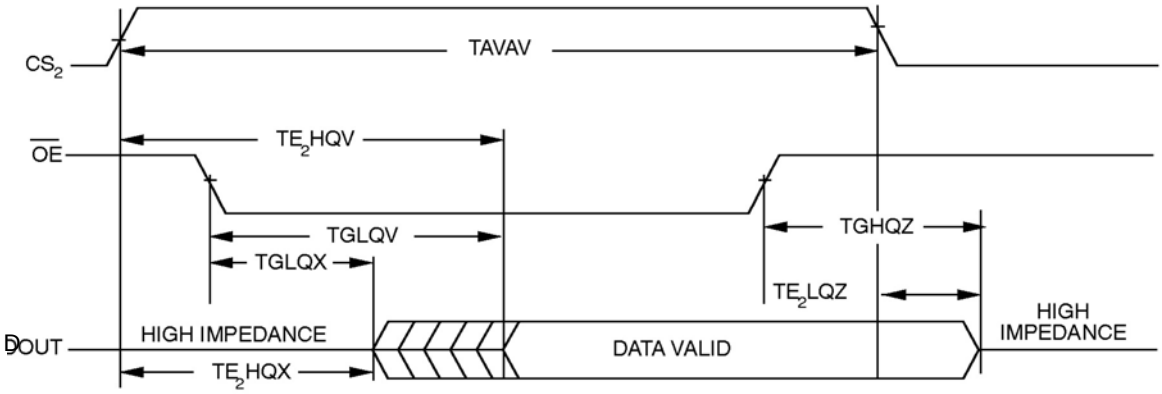


Figure 6. Read Cycle nb 3



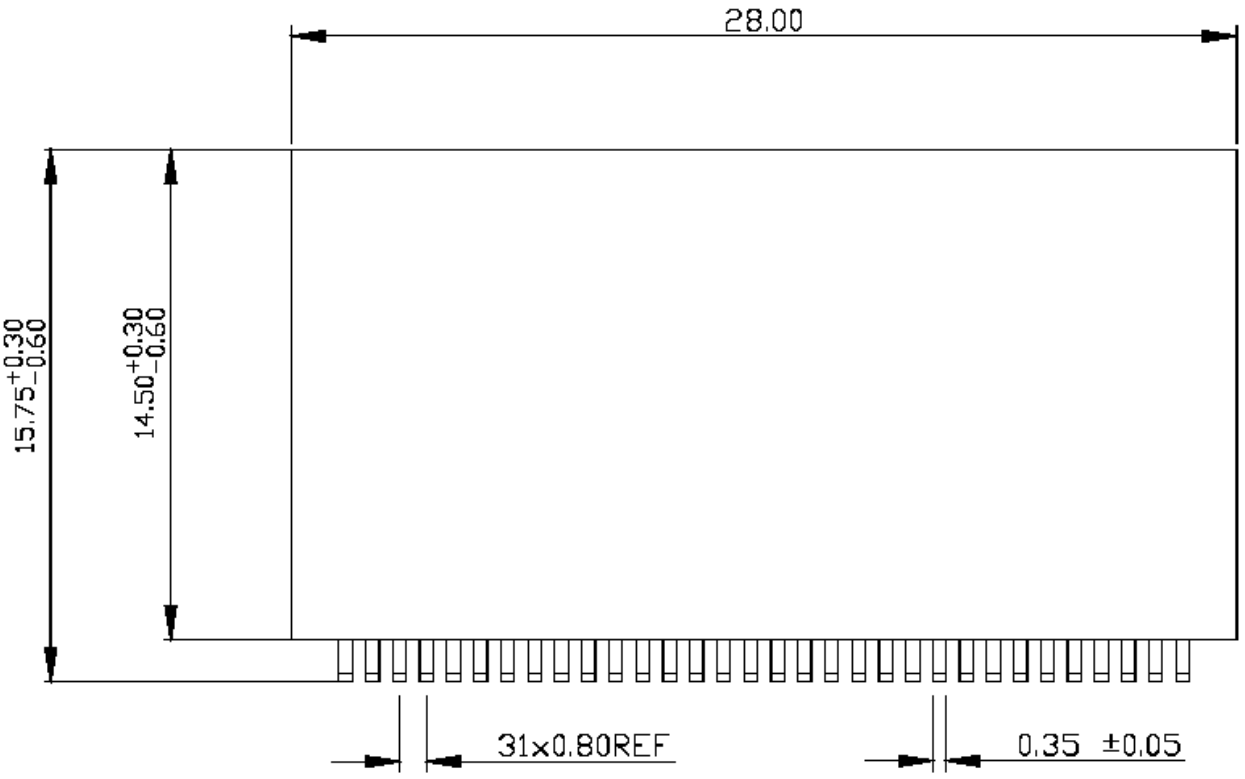
Test Tools

Supplier	Reference Number
ENPLAS	OTS - 64 - 0.8 - 04

Ordering Information

Reference Number	Temperature Range	Speed	Package	Quality Flow
AT61162E-PM40MMN	-55 to +125°C	40 ns	Cube 64 pins	Atmel flow for plastic package (equivalent to MIL-PRF-38535 QML N)
AT61162E-PM40M-E	25°C	40 ns	Cube 64 pins	Engineering Samples

Package Drawing



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