

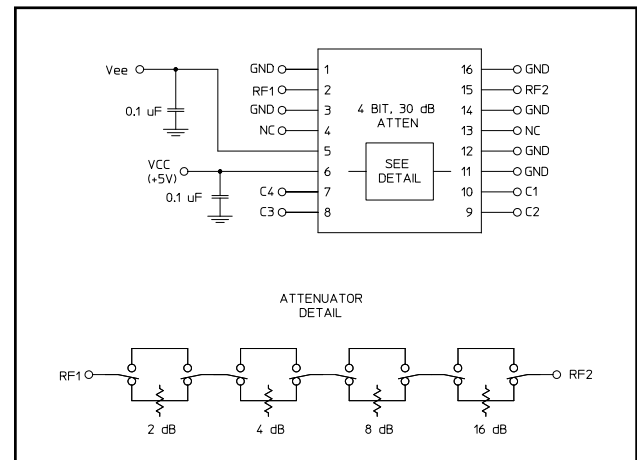
Features

- Attenuation: 2.0 dB steps to 30 dB
- Low DC Power Consumption
- Integral TTL Driver
- 50 Ohm Impedance
- Temperature Stability: ± 0.18 dB from -55°C to $+85^{\circ}\text{C}$ Typ.
- SOIC-16 Package

Description

M/A-COM's AT65-0233 is a GaAs FET 4-bit digital attenuator with a 2.0 dB minimum step size and a 30 dB total attenuation range. This device is in a SOIC-16 plastic surface mount package. The AT65-0233 is ideally suited for use where accuracy, fast speed, very low power consumption and low costs are required. Typical applications include dynamic range setting in precision receiver circuits and other gain/leveling control circuits.

Schematic with Off-Chip Components or Functional Block Diagram



Ordering Information

Part Number	Package
AT65-0233	Bulk Packaging
AT65-0233TR	1000 piece reel
AT65-0233-TB	Sample Test Board

Note: Reference Application Note M513 for reel size information.

Pin Configuration

Pin No.	Function	Pin No.	Function
1	GND	9	C2
2	RF1	10	C1
3	GND	11	GND
4	NC ¹	12	GND
5	Vcc	13	NC ¹
6	C4	14	GND
7	C3	15	RF2
8	C3	16	GND

1. NC = No Connection

Digital Attenuator
30.0 dB, 4-Bit, TTL Driver, DC-3.0 GHz

Rev. V6

Electrical Specifications: $T_A = 25^\circ\text{C}$

Parameter	Test Conditions	Frequency	Units	Min	Typ	Max
Insertion Loss	—	DC - 0.5 GHz	dB	—	1.7	2.0
		DC - 2.0 GHz	dB	—	2.3	2.7
		DC - 3.0 GHz	dB	—	2.6	3.1
Attenuation Accuracy	Any Bit or Combination of Bits	DC - 3.0 GHz	dB	$\pm (.4 + 8\% \text{ of attenuation})$	$\pm (.4 + 8\% \text{ of attenuation})$	$\pm (.4 + 8\% \text{ of attenuation})$
VSWR	Full Range	DC - 3.0 GHz	Ratio	—	—	1.7:1
Trise, Tfall Ton, Toff Transients	10% to 90% 50% Cntl to 90%/10% RF In-Band	10% to 90%	nS	—	10	50
		50% Cntl to 90%/10% RF	nS	—	30	150
		In-Band	mV	—	35	—
1 dB Compression	Input Power Input Power	0.05 GHz	dBm	—	+20	—
		0.5 - 3.0 GHz	dBm	—	+28	—
Input IP_3	Two-tone inputs up to +5 dBm	0.05 GHz	dBm	—	+40	—
		0.5 - 3.0 GHz	dBm	—	+50	—
Input IP_2	Two-tone inputs up to +5 dBm	0.05 GHz	dBm	—	+45	—
		0.5 - 3.0 GHz	dBm	—	+68	—
V_{CC}	—	—	V	4.5	5.0	5.5
V_{EE}	—	—	V	-8.0	-5.0	-4.75
V_{IL} V_{IH}	LOW-level input voltage	—	V	0.0	—	0.8
	HIGH-level input voltage	—	V	2.0	—	5.0
lin (Input Leakage Current)	$V_{in} = V_{CC}$ or GND	—	μA	-1.0	—	1.0
I_{CC} (Quiescent Supply Current)	$V_{cntrl} = V_{CC}$ or GND	—	μA	—	250	400
ΔI_{CC} (Additional Supply Current Per TTL Input Pin)	$V_{CC} = \text{Max}$, $V_{cntrl} = V_{CC} - 2.1 \text{ V}$	—	mA	—	—	1.0
IEE	V_{EE} min to max, $V_{in} = V_{IL}$ or V_{IH}	—	mA	-1.0	-0.2	—

Absolute Maximum Ratings^{2,3}

Parameter	Absolute Maximum
Max. Input Power 0.05 GHz 0.5 - 3.0 GHz	+27 dBm +34 dBm
V_{CC}	$-0.5\text{V} \leq V_{CC} \leq +7.0\text{V}$
V_{EE}	$-8.5\text{V} \leq V_{EE} \leq +0.5\text{V}$
$V_{CC} - V_{EE}$	$-0.5\text{V} \leq V_{CC} - V_{EE} \leq 14.5\text{V}$
V_{in}^4	$-0.5\text{V} \leq V_{in} \leq V_{CC} + 0.5\text{V}$
Operating Temperature	-40°C to $+85^\circ\text{C}$
Storage Temperature	-65°C to $+125^\circ\text{C}$

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Standard CMOS TTL interface, latch=up will occur if logic signal applied prior to power supply.

ADVANCED: Data Sheets contain information regarding a product M/A-COM Technology Solutions is considering for development. Performance is based on target specifications, simulated results, and/or prototype measurements. Commitment to develop is not guaranteed.

PRELIMINARY: Data Sheets contain information regarding a product M/A-COM Technology Solutions has under development. Performance is based on engineering tests. Specifications are typical. Mechanical outline has been fixed. Engineering samples and/or test data may be available. Commitment to produce in volume is not guaranteed.

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Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

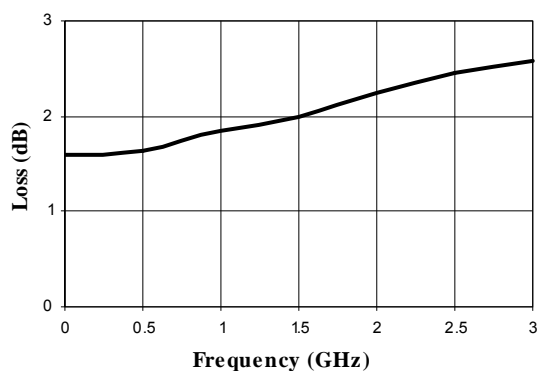
Truth Table (Digital Attenuator)

C1	C2	C3	C4	Attenuation
0	0	0	0	Loss, Reference
1	0	0	0	2.0 dB
0	1	0	0	4.0 dB
0	0	1	0	8.0 dB
0	0	0	1	16.0 dB
1	1	1	1	30.0 dB

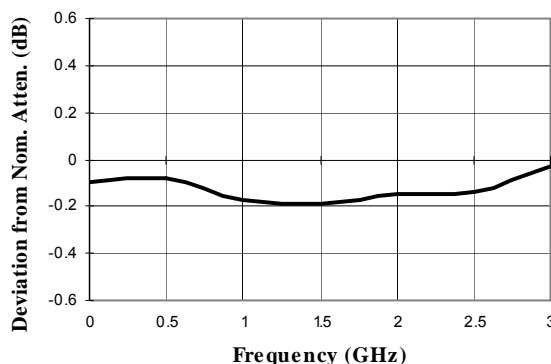
0 = TTL Low; 1 = TTL High

Typical Performance Curves

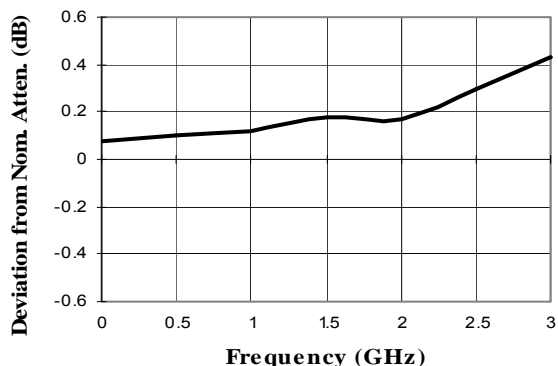
Typical Insertion Loss (dB)



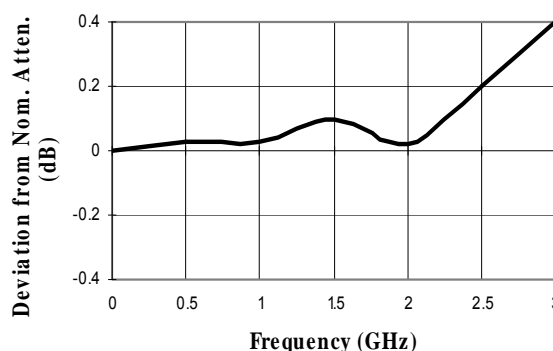
Attenuation Accuracy, 2 dB



Attenuation Accuracy, 4 dB

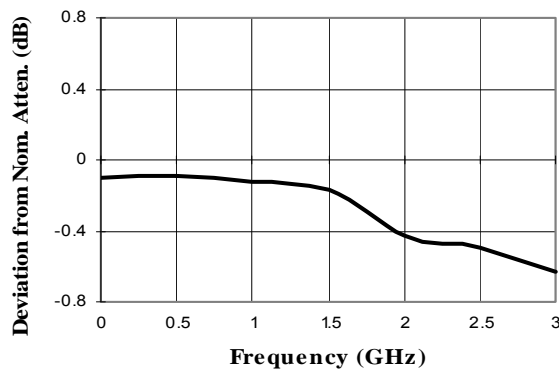


Attenuation Accuracy, 8 dB

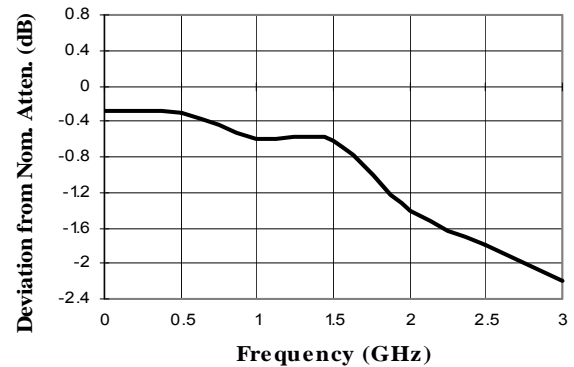


Typical Performance Curves

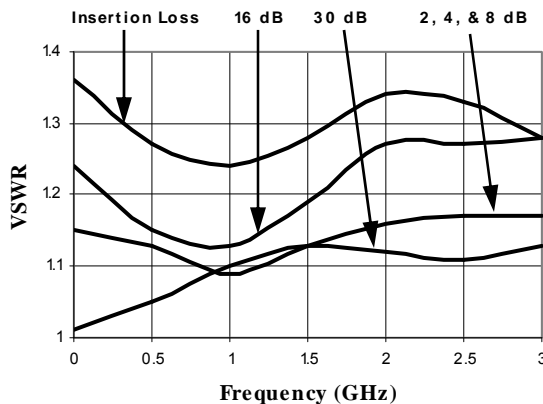
Attenuation Accuracy, 16 dB



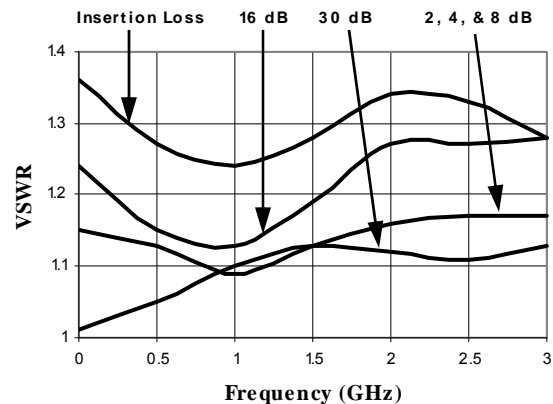
Attenuation Accuracy, 30 dB



Typical RF1 VSWR



Typical RF2 VSWR



Rev. V6

The technical drawing illustrates the dimensions of a MACOM package from three perspectives:

- Top View:** Shows the overall footprint with dimensions such as .0500 / 1.27 for pin pitch, .1535 / 3.90 for body width, and .2362 / 6.00 for the central area. It includes labels for PIN 16, PART NUMBER, XXXXXXXXXX, YYWWXXXX, MACOM, DATE/LOT CODE, COMPANY LOGO, ORIENTATION MARK, and PIN 1.
- Side View:** Displays the profile of the package with dimensions like .0492 MIN. / 1.25 and .0688 MAX. / 1.75. A SEATING PLANE is indicated at the base.
- Cross-Section B-B:** Provides a detailed view of the internal structure, showing the BASE MATERIAL, WITH PLATING, and various layer thicknesses such as .0189 / .0110, .0090 / .0066, .023 / .017, and .0201 / (.0122).

NOTES:

- REFERENCE JEDEC MS-012-AC FOR ADDITIONAL DIMENSIONAL AND TOLERANCE INFORMATION.
- REFERENCE M538 APPLICATION NOTE FOR FOOTPRINT INFORMATION.
- ALL DIMENSIONS SHOWN AS INCHES/MM.

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