

## Features

- 16 Mbit SRAM Multi Chip Module
- Allows 32-, 16- or 8-bit access configuration
- Operating Voltage: 3.3V  $\pm$  0.3V
- Access Time
  - 20 ns, 18 ns for AT68166F
  - <18 ns for AT68166G (in development prototypes in Q4 2007)
- Power Consumption
  - Active: 620 mW per byte (Max) @ 18ns - 415 mW per byte (Max) @ 50ns <sup>(1)</sup>
  - Standby: 13 mW (Typ)
- Military Temperature Range: -55 to +125°C
- TTL-Compatible Inputs and Outputs
- Asynchronous
- Die manufactured on Atmel 0.25  $\mu$ m Radiation Hardened Process
- No Single Event Latch Up below LET Threshold of 80 MeV/mg/cm<sup>2</sup>
- Tested up to a Total Dose of 300 krad (Si) according to MIL-STD-883 Method 1019
- ESD Better than 4000V
- Quality Grades:
  - QML-Q or V with SMD 5962-06229
  - ESCC
- 950 Mils Wide MQFP 68 Package
- Mass : 8.5 grams

Note: 1. Only for AT68166F-18. 450mW for AT68166F-20.

## Description

The AT68166F/G is a 16Mbit SRAM packaged in a hermetic Multi Chip Module (MCM) for space applications.

The AT68166F/G MCM incorporates four 4Mbit AT60142FT SRAM dice. It can be organized as either one bank of 512Kx8, two banks of 512Kx16 or four banks of 512Kx8. It combines rad-hard capabilities, a latch-up threshold of 80MeV.cm<sup>2</sup>/mg, a Multiple Bit Upset immunity and a total dose tolerance of 300Krad, with a fast access time.

The MCM packaging technology allows a reduction of the PCB area by 50% with a weight savings of 75% compared to four 4Mbit packages.

Thanks to the small size of the 4Mbit SRAM die, Atmel has been able to accommodate the assembly of the four dice on one side of the package which facilitates the power dissipation.

The compatibility with other products allows designers to easily migrate to the Atmel AT68166F/G memory.

The AT68166F/G is powered at 3.3V.

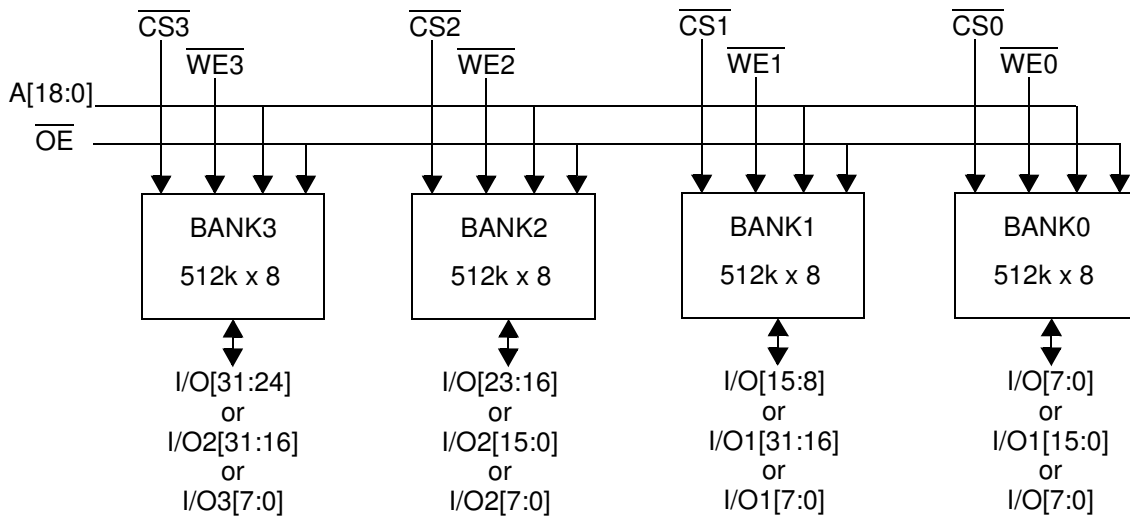
The AT68166F/G is processed according to the test methods of the latest revision of the MIL-PRF-38535 or the ESCC 9000.



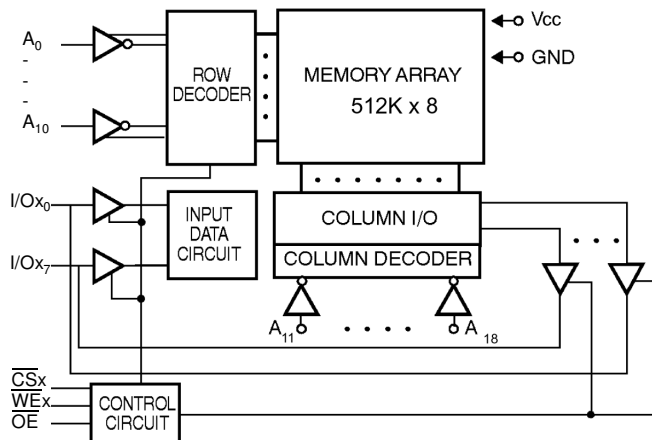
**Rad Hard**  
**16 MegaBit**  
**3.3V**  
**SRAM Multi-**  
**Chip Module**

**AT68166F**  
**AT68166G**

## Block Diagram Figure 1. AT68166F/G Block Diagram



**Figure 2.** 512K x 8 Banks Block Diagram (AT60142F/G)



## Packages

AT68166F and AT68166G are packed in MQFP68.

|          | Access Time |       |        |
|----------|-------------|-------|--------|
|          | 20 ns       | 18 ns | <18 ns |
| AT68166F | YM          | YS    |        |
| AT68166G |             |       | YS     |

The pin assignment depends on the access time. There are 2 versions:

- YM package where 3 pins are not connected.
- YS package where the 3 above pins are connected to GND or  $V_{CC}$ .

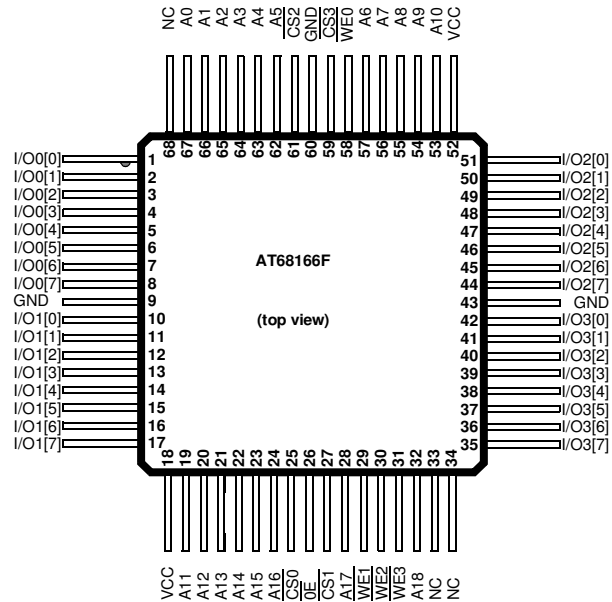
## Pin Configuration

**Table 1.** AT68166F/G pin assignment in YS package

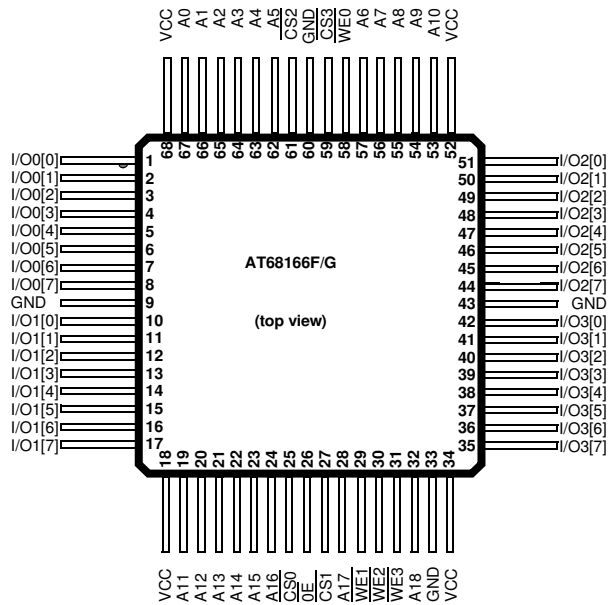
| Lead | Signal  | Lead | Signal | Lead | Signal  | Lead | Signal |
|------|---------|------|--------|------|---------|------|--------|
| 1    | I/O0[0] | 18   | VCC    | 35   | I/O3[7] | 52   | VCC    |
| 2    | I/O0[1] | 19   | A11    | 36   | I/O3[6] | 53   | A10    |
| 3    | I/O0[2] | 20   | A12    | 37   | I/O3[5] | 54   | A9     |
| 4    | I/O0[3] | 21   | A13    | 38   | I/O3[4] | 55   | A8     |
| 5    | I/O0[4] | 22   | A14    | 39   | I/O3[3] | 56   | A7     |
| 6    | I/O0[5] | 23   | A15    | 40   | I/O3[2] | 57   | A6     |
| 7    | I/O0[6] | 24   | A16    | 41   | I/O3[1] | 58   | WE0    |
| 8    | I/O0[7] | 25   | CS0    | 42   | I/O3[0] | 59   | CS3    |
| 9    | GND     | 26   | OE     | 43   | GND     | 60   | GND    |
| 10   | I/O1[0] | 27   | CS1    | 44   | I/O2[7] | 61   | CS2    |
| 11   | I/O1[1] | 28   | A17    | 45   | I/O2[6] | 62   | A5     |
| 12   | I/O1[2] | 29   | WE1    | 46   | I/O2[5] | 63   | A4     |
| 13   | I/O1[3] | 30   | WE2    | 47   | I/O2[4] | 64   | A3     |
| 14   | I/O1[4] | 31   | WE3    | 48   | I/O2[3] | 65   | A2     |
| 15   | I/O1[5] | 32   | A18    | 49   | I/O2[2] | 66   | A1     |
| 16   | I/O1[6] | 33   | GND    | 50   | I/O2[1] | 67   | A0     |
| 17   | I/O1[7] | 34   | VCC    | 51   | I/O2[0] | 68   | VCC    |

Notes: 1. In YM package leads 33, 34 and 68 are not connected.

**Figure 3. AT68166F pin assignment in YM package**



**Figure 4. AT68166F/G pin assignment in YS package**



## Pin Description

**Table 2.** Pin Names

| Name                                | Description       |
|-------------------------------------|-------------------|
| A0 - A18                            | Address Inputs    |
| I/O0 - I/O31                        | Data Input/Output |
| $\overline{CS0}$ - $\overline{CS3}$ | Chip Select       |
| $\overline{WE0}$ - $\overline{WE3}$ | Write Enable      |
| $\overline{OE}$                     | Output Enable     |
| VCC                                 | Power Supply      |
| GND <sup>(1)</sup>                  | Ground            |

Note: 1. The package lid is connected to GND

**Table 3.** Truth Table<sup>(1)</sup>

| $\overline{CSx}$ | $\overline{WEx}$ | $\overline{OE}$ | Inputs/Outputs | Mode           |
|------------------|------------------|-----------------|----------------|----------------|
| H                | X                | X               | Z              | Standby        |
| L                | H                | L               | Data Out       | Read           |
| L                | L                | X               | Data In        | Write          |
| L                | H                | H               | Z              | Output Disable |

Note: 1. L=low, H=high, X= H or L, L=high impedance.

## Electrical Characteristics

### Absolute Maximum Ratings\*

Supply Voltage to GND Potential:.....-0.5V + 4.6V  
 DC Input Voltage:.....GND -0.5V to 4.6V  
 DC Output Voltage High Z State:.....GND -0.5V to 4.6V  
 Storage Temperature: ..... -65°C to + 150°C  
 Output Current Into Outputs (Low): ..... 20 mA  
 Electro Statics Discharge Voltage:.....> 4000V (MIL STD 883D Method 3015.3)

\*NOTE:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Military Operating Range

| Operating Voltage | Operating Temperature |
|-------------------|-----------------------|
| 3.3 ± 0.3V        | -55°C to + 125°C      |

### Recommended DC Operating Conditions

| Parameter       | Description        | Min       | Typ | Max                   | Unit |
|-----------------|--------------------|-----------|-----|-----------------------|------|
| V <sub>CC</sub> | Supply voltage     | 3         | 3.3 | 3.6                   | V    |
| GND             | Ground             | 0.0       | 0.0 | 0.0                   | V    |
| V <sub>IL</sub> | Input low voltage  | GND - 0.3 | 0.0 | 0.8                   | V    |
| V <sub>IH</sub> | Input high voltage | 2.2       | –   | V <sub>CC</sub> + 0.3 | V    |

### Capacitance

| Parameter                                    | Description       | Min | Typ | Max | Unit |
|----------------------------------------------|-------------------|-----|-----|-----|------|
| C <sub>in</sub> <sup>(1)</sup> (OE and Ax)   | Input capacitance | –   | –   | 48  | pF   |
| C <sub>in</sub> <sup>(1)</sup> (CSx and WEx) | Input capacitance | –   | –   | 12  | pF   |
| C <sub>io</sub> <sup>(1)</sup>               | I/O capacitance   | –   | –   | 12  | pF   |

Note: 1. Guaranteed but not tested.

**DC Parameters**

| Parameter          | Description            | Minimum | Typical | Maximum | Unit |
|--------------------|------------------------|---------|---------|---------|------|
| IIX <sup>(1)</sup> | Input leakage current  | -1      | –       | 1       | μA   |
| IOZ <sup>(1)</sup> | Output leakage current | -1      | –       | 1       | μA   |
| VOL <sup>(2)</sup> | Output low voltage     | –       | –       | 0.4     | V    |
| VOH <sup>(3)</sup> | Output high voltage    | 2.4     | –       | –       | V    |

Notes: 1.  $GND < V_{IN} < V_{CC}$ ,  $GND < V_{OUT} < V_{CC}$  Output Disabled.

2.  $V_{CC}$  min.  $I_{OL} = 8$  mA

3.  $V_{CC}$  min.  $I_{OH} = -4$  mA

**Consumption**

| Symbol                                          | Description               | TAVAV/TAVAW Test Condition      | AT68166F-20            | AT68166F-18              | Unit | Value |
|-------------------------------------------------|---------------------------|---------------------------------|------------------------|--------------------------|------|-------|
| I <sub>CCSB</sub> <sup>(1)</sup>                | Standby Supply Current    | –                               | 10                     | 7                        | mA   | max   |
| I <sub>CCSB1</sub> <sup>(2)</sup>               | Standby Supply Current    | –                               | 8                      | 6                        | mA   | max   |
| I <sub>CCOP</sub> <sup>(3)</sup> Read per byte  | Dynamic Operating Current | 18 ns<br>20 ns<br>50 ns<br>1 μs | –<br>170<br>85<br>15   | 170<br>165<br>80<br>12   | mA   | max   |
| I <sub>CCOP</sub> <sup>(4)</sup> Write per byte | Dynamic Operating Current | 18 ns<br>20 ns<br>50 ns<br>1 μs | –<br>150<br>125<br>110 | 145<br>140<br>115<br>105 | mA   | max   |

Notes: 1. All  $\overline{CSx} \geq V_{IH}$

2. All  $\overline{CSx} \geq V_{CC} - 0.3V$

3.  $F = 1/T_{TAVAV}$ ,  $I_{out} = 0$  mA,  $\overline{WEx} = \overline{OE} = V_{IH}$ ,  $V_{IN} = GND/V_{CC}$ ,  $V_{CC}$  max.

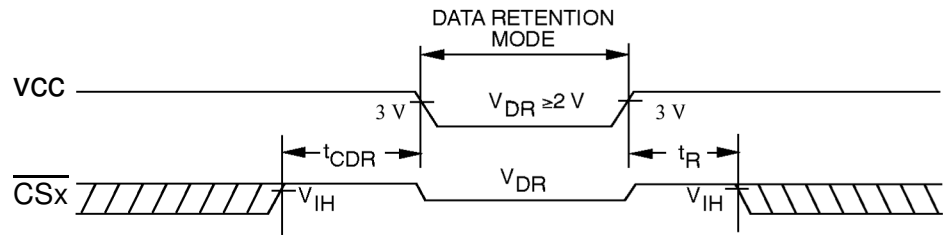
4.  $F = 1/T_{TAVAW}$ ,  $I_{out} = 0$  mA,  $\overline{WEx} = V_{IL}$ ,  $\overline{OE} = V_{IH}$ ,  $V_{IN} = GND/V_{CC}$ ,  $V_{CC}$  max.

## Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. During data retention chip select  $\overline{CSx}$  must be held high within  $V_{CC}$  to  $V_{CC} - 0.2V$ .
2. Output Enable ( $\overline{OE}$ ) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power-up and power-down transitions  $\overline{CSx}$  and  $\overline{OE}$  must be kept between  $V_{CC} + 0.3V$  and 70% of  $V_{CC}$ .
4. The RAM can begin operation  $> t_R$  ns after  $V_{CC}$  reaches the minimum operation voltages (3V).

**Figure 5.** Data Retention Timing



## Data Retention Characteristics

| Parameter        | Description                          | Min              | Typ $T_A = 25^\circ C$ | Max               | Unit |
|------------------|--------------------------------------|------------------|------------------------|-------------------|------|
| $V_{CCDR}$       | $V_{CC}$ for data retention          | 2.0              | —                      | —                 | V    |
| $t_{CDR}$        | Chip deselect to data retention time | 0.0              | —                      | —                 | ns   |
| $t_R$            | Operation recovery time              | $t_{AVAV}^{(1)}$ | —                      | —                 | ns   |
| $I_{CCDR}^{(2)}$ | Data retention current               | —                | 3                      | 6 (AT68166F-20)   | mA   |
|                  |                                      |                  |                        | 4.5 (AT68166F-18) |      |

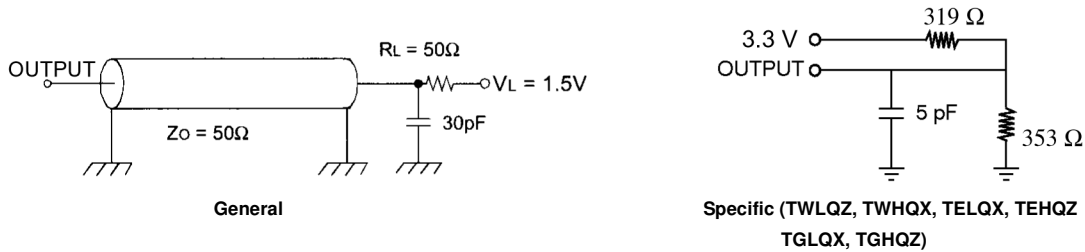
1.  $T_{AVAV}$  = Read cycle time.
2. All  $\overline{CSx} = V_{CC}$ ,  $V_{IN} = GND/V_{CC}$ .



## AC Characteristics

Temperature Range:..... -55 +125°C  
 Supply Voltage: ..... 3.3 ±0.3V  
 Input Pulse Levels: ..... GND to 3.0V  
 Input Rise and Fall Times:..... 3ns (10 - 90%)  
 Input and Output Timing Reference Levels:..... 1.5V  
 Output Loading  $I_{OL}/I_{OH}$ :..... See Figure 3

Figure 6. AC Test Loads Waveforms



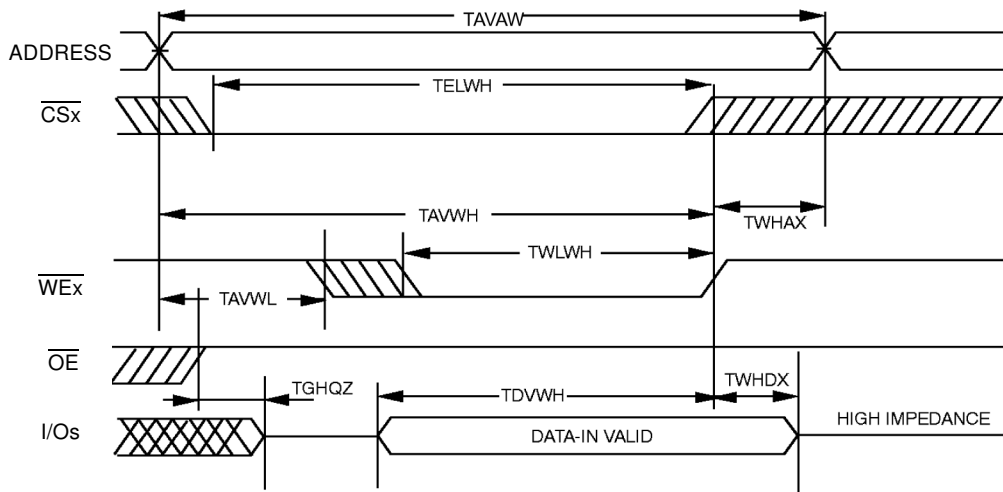
## Write Cycle

Table 4. Write cycle timings<sup>(1)</sup>

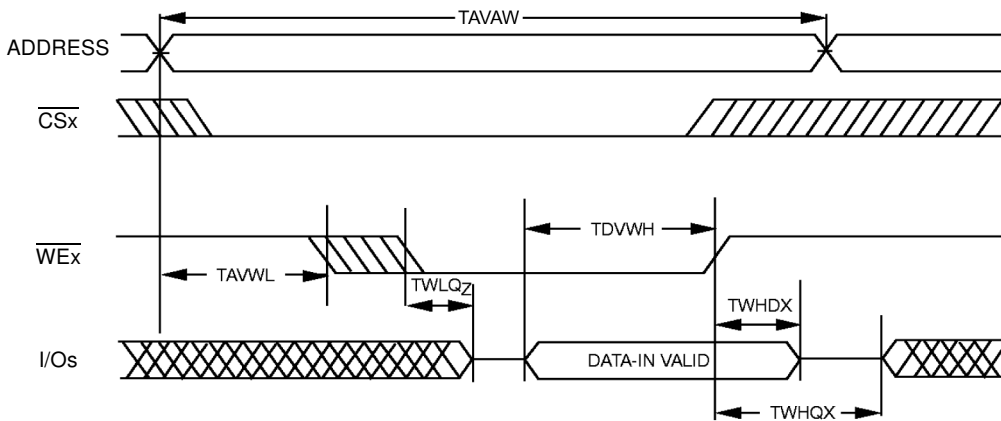
| Symbol | Parameter                        | AT68166F-20 |     | AT68166F-18 |     | Unit |
|--------|----------------------------------|-------------|-----|-------------|-----|------|
|        |                                  | min         | max | min         | max |      |
| TAVAW  | Write cycle time                 | 20          | -   | 18          | -   | ns   |
| TAVWL  | Address set-up time              | 2           | -   | 2           | -   | ns   |
| TAVWH  | Address valid to end of write    | 14          | -   | 11          | -   | ns   |
| TDVWH  | Data set-up time                 | 9           | -   | 8           | -   | ns   |
| TELWH  | $\overline{CS}$ low to write end | 12          | -   | 12          | -   | ns   |
| TWLQZ  | Write low to high $Z^{(2)}$      | -           | 10  | -           | 8   | ns   |
| TWLWH  | Write pulse width                | 12          | -   | 9           | -   | ns   |
| TWHAX  | Address hold from end of write   | 0           | -   | 0           | -   | ns   |
| TWHDX  | Data hold time                   | 2           | -   | 1           | -   | ns   |
| TWHQX  | Write high to low $Z^{(2)}$      | 5           | -   | 3           | -   | ns   |

Notes: 1. Timings figures applicable for 8-bit, 16-bit and 32-bit mode.  
 2. Parameters guaranteed, not tested, with output loading 5 pF. (See "AC Test Loads Waveforms" on page 9.)

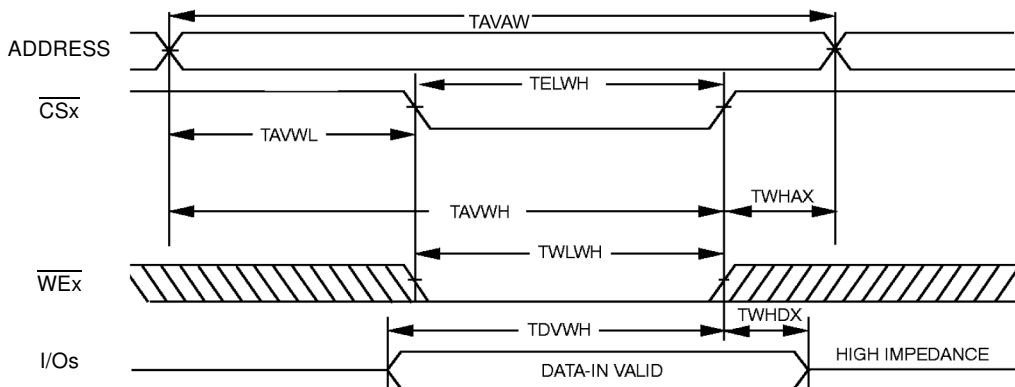
**Figure 7. Write Cycle 1.  $\overline{WE}$  Controlled,  $\overline{OE}$  High During Write**



**Figure 8. Write Cycle 2.  $\overline{WE}$  Controlled,  $\overline{OE}$  Low**



**Figure 9. Write Cycle 3.  $\overline{CS}$  Controlled**



The internal write time of the memory is defined by the overlap of  $\overline{CS}$  Low and  $\overline{WE}$  LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in active mode. The data input setup and hold timing should be referenced to the active edge of the signal that terminates the write. Data out is high impedance if  $\overline{OE} = V_{IH}$ .

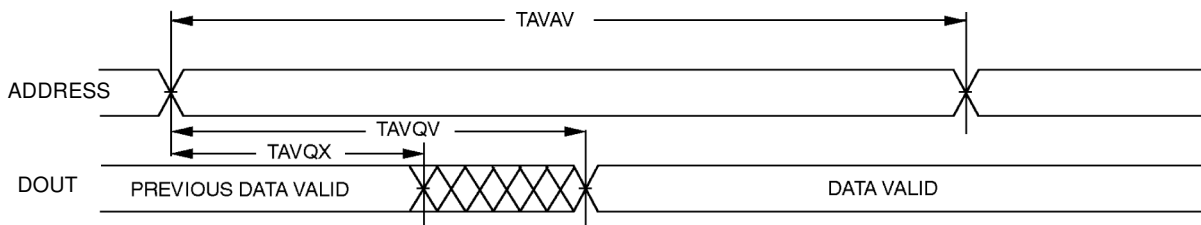
## Read Cycle

**Table 5.** Read cycle timings<sup>(1)</sup>

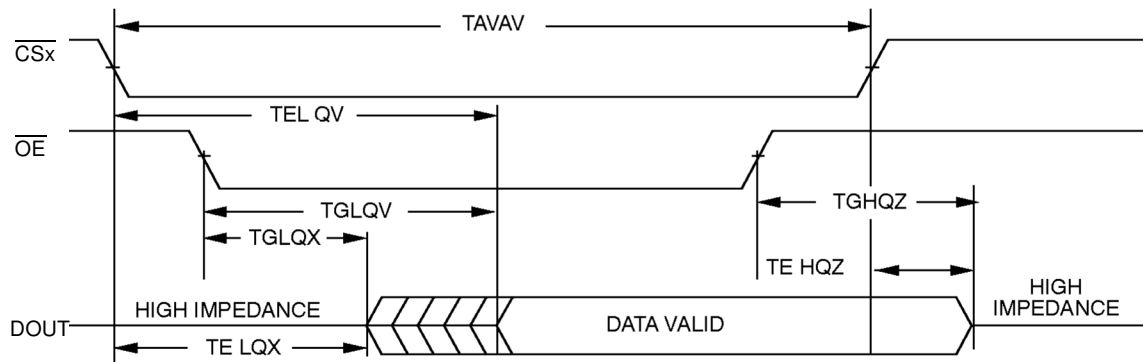
| Symbol | Parameter                                            | AT68166F-20 |     | AT68166F-18 |     | Unit |
|--------|------------------------------------------------------|-------------|-----|-------------|-----|------|
|        |                                                      | min         | max | min         | max |      |
| TAVAV  | Read cycle time                                      | 20          | -   | 18          | -   | ns   |
| TAVQV  | Address access time                                  | -           | 20  | -           | 18  | ns   |
| TAVQX  | Address valid to low Z                               | 5           | -   | 5           | -   | ns   |
| TELQV  | Chip-select access time                              | -           | 20  | -           | 18  | ns   |
| TELQX  | $\overline{\text{CS}}$ low to low Z <sup>(2)</sup>   | 5           | -   | 5           | -   | ns   |
| TEHQZ  | $\overline{\text{CS}}$ high to high Z <sup>(2)</sup> | -           | 9   | -           | 8   | ns   |
| TGLQV  | Output Enable access time                            | -           | 11  | -           | 8   | ns   |
| TGLQX  | $\overline{\text{OE}}$ low to low Z <sup>(2)</sup>   | 2           | -   | 2           | -   | ns   |
| TGHQZ  | $\overline{\text{OE}}$ high to high Z <sup>(2)</sup> | -           | 9   | -           | 8   | ns   |

- Notes: 1. Timings figures applicable for 8-bit, 16-bit and 32-bit mode.  
2. Parameters guaranteed, not tested, with output loading 5 pF. (See “AC Test Loads Waveforms” on page 9.)

**Figure 10.** Read Cycle nb 1: Address Controlled ( $\overline{\text{CS}} = \overline{\text{OE}} = V_{\text{IL}}$ ,  $\overline{\text{WE}} = V_{\text{IH}}$ )



**Figure 11.** Read Cycle nb 2: Chip Select Controlled ( $\overline{WE} = V_{IH}$ )



## Typical Applications

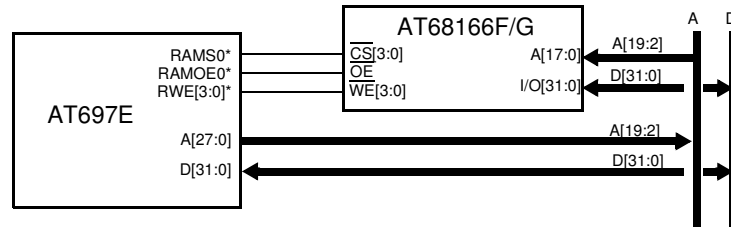
This section presents some standard implementations of the AT68166F/G in application.

### 32-bit mode application

When used on a 32-bit (word) application, the module shall be connected as follow :

- The 32 lines of data are connected to distinct data lines
- The four  $\overline{CS}_x$  are connected together and linked to a single host  $\overline{CS}$  output
- Each one of the four  $\overline{WE}_x$  is connected to a dedicated  $\overline{WE}$  line on the host to allow byte, half word and word format write.

**Figure 12.** 32-bit typical application ( 1 SRAM bank)

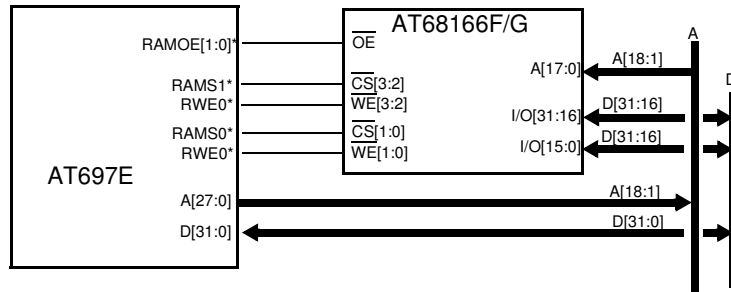


### 16-bit mode application

When used on a 16-bit (half word) application, the module can be connected as presented in the following figure. This allows use of a single AT68166F/G part for two SRAM memory banks.

All input controls of the AT68166F/G not used in the application shall be pulled-up.

**Figure 13.** 16-bit typical application (two SRAM banks)

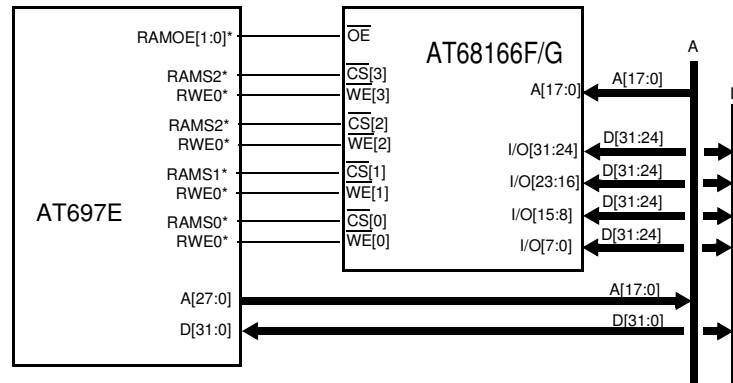


### 8-bit mode application

When used on a 8-bit (byte) application, the module can be connected as presented in the following figure. This allows use of a single AT68166F/G part for up to four SRAM memory banks.

All input controls of the AT68166F/G not used in the application shall be pulled-up.

**Figure 14.** 8-bit typical application (two SRAM banks)



## Ordering Information

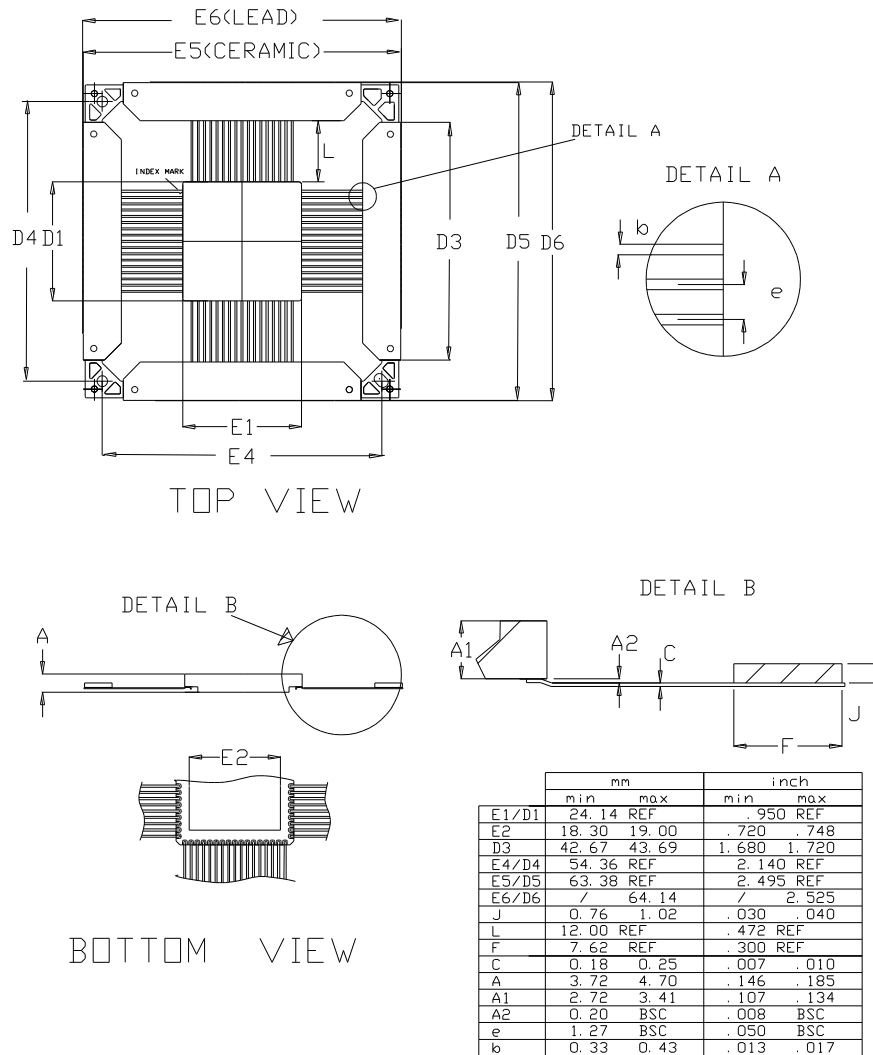
| Part Number                      | Temperature Range | Speed | Package | Flow                |
|----------------------------------|-------------------|-------|---------|---------------------|
| <b>AT68166F</b>                  |                   |       |         |                     |
| AT68166F-YM20-E                  | 25°C              | 20 ns | MQFP68  | Engineering Samples |
| 5962-0622902QXC                  | -55° to +125°C    | 20 ns | MQFP68  | QML Q               |
| 5962-0622902VXC                  | -55° to +125°C    | 20 ns | MQFP68  | QML V               |
| 5962R0622902VXC                  | -55° to +125°C    | 20 ns | MQFP68  | QML V RHA           |
| AT68166F-YM20-SCC                | -55° to +125°C    | 20 ns | MQFP68  | ESCC                |
| AT68166F-YS18-E                  | 25°C              | 18 ns | MQFP68  | Engineering Samples |
| AT68166F-YS18-MQ <sup>(1)</sup>  | -55° to +125°C    | 18 ns | MQFP68  | QML Q               |
| AT68166F-YS18-SV <sup>(1)</sup>  | -55° to +125°C    | 18 ns | MQFP68  | QML V               |
| AT68166F-YS18-SR <sup>(1)</sup>  | -55° to +125°C    | 18 ns | MQFP68  | QML V RHA           |
| AT68166F-YS18-SCC <sup>(1)</sup> | -55° to +125°C    | 18 ns | MQFP68  | ESCC                |

Note: 1. Will be replaced by SMD part number when available.

## Package Drawings

### 68-lead Quad Flat Pack (950 Mils) with non conductive tie bar

68 LEADS FLAT PACK CERAMIC TIE BAR



Note: Lid is connected to Ground.

Note: YM and YS package drawings are identical.





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