

## Features

- Main Supply 3.0V to 3.6V
- Independent 2.5V to 3.6V Auxiliary Supply for Backup Section
- Internal State Machine for Startup
- 25 mA/1.8V-2.75V Linear Low Drop Out Regulator with High PSRR and Low Noise (LDO1)
- 30 mA/1.5V-1.8V Linear Low Drop Out Regulator with High PSRR and Low Noise (LDO2)
- 60 mA/1.23V-1.5V-1.8V Linear Low Drop Out Regulator with High PSRR (LDO3)
- 2 mA/1.2V-1.5V-1.8V Linear Low Drop Out Regulator with Very Low Quiescent Current (LDO4)
- HPBG Economic High Performance Voltage Reference for LDO Supply to RF Sections
- LPBG Low Power Voltage Reference to LDO4 During Backup Battery Operation
- Internal Oscillator Generates Internal Master Clock
- Internal Reset Generator for Main Supply
- Additional External Reset Input
- Two Wire Interface (TWI) for Independent Activation and Output Voltage Programming for Each LDO
- Available in 3 x 3 x 0.9 mm 16-pin QFN Package
- Applications: GPS Modules, WLAN Devices, Wireless Modules

## 1. Description

The AT73C239 is a four-channel Power Supply Power Management Unit (PMU) available in a QFN 3 x 3 mm package. It is a fully integrated, low cost, combined Power Management device for wireless modules, GPS and WLAN devices. It integrates four Linear Low Drop Out (LDO) Regulators, three of which provide high-accuracy RF performance and one (LDO4) with very low quiescent current that is supplied by an external backup battery. A Low Power Bandgap (LPBG) requiring no external capacitor for decoupling, is used as reference voltage for LDO4 and starts when VBAT is present. LDO4 regulates output voltage with extremely low quiescent current, maximizing the lifetime of the backup battery. An Internal State Machine manages the startup of the other LDOs in the order of LDO3 then LDO1 then LDO2. An economic High Power Bandgap (HPBG) provides highly accurate, low noise voltage reference to LDOs 1, 2, 3. HPBG operates in switching mode thereby decreasing its current consumption and becomes inactive when not directly supplied by VIN current. When the RF LDOs are in idle mode, quiescent current is decreased to a minimum.

The AT73C239 features a Two-wire Interface (TWI) to increase the efficiency of the system by disabling LDOs when not needed.



## Power Management and Analog Companions (PMAAC)

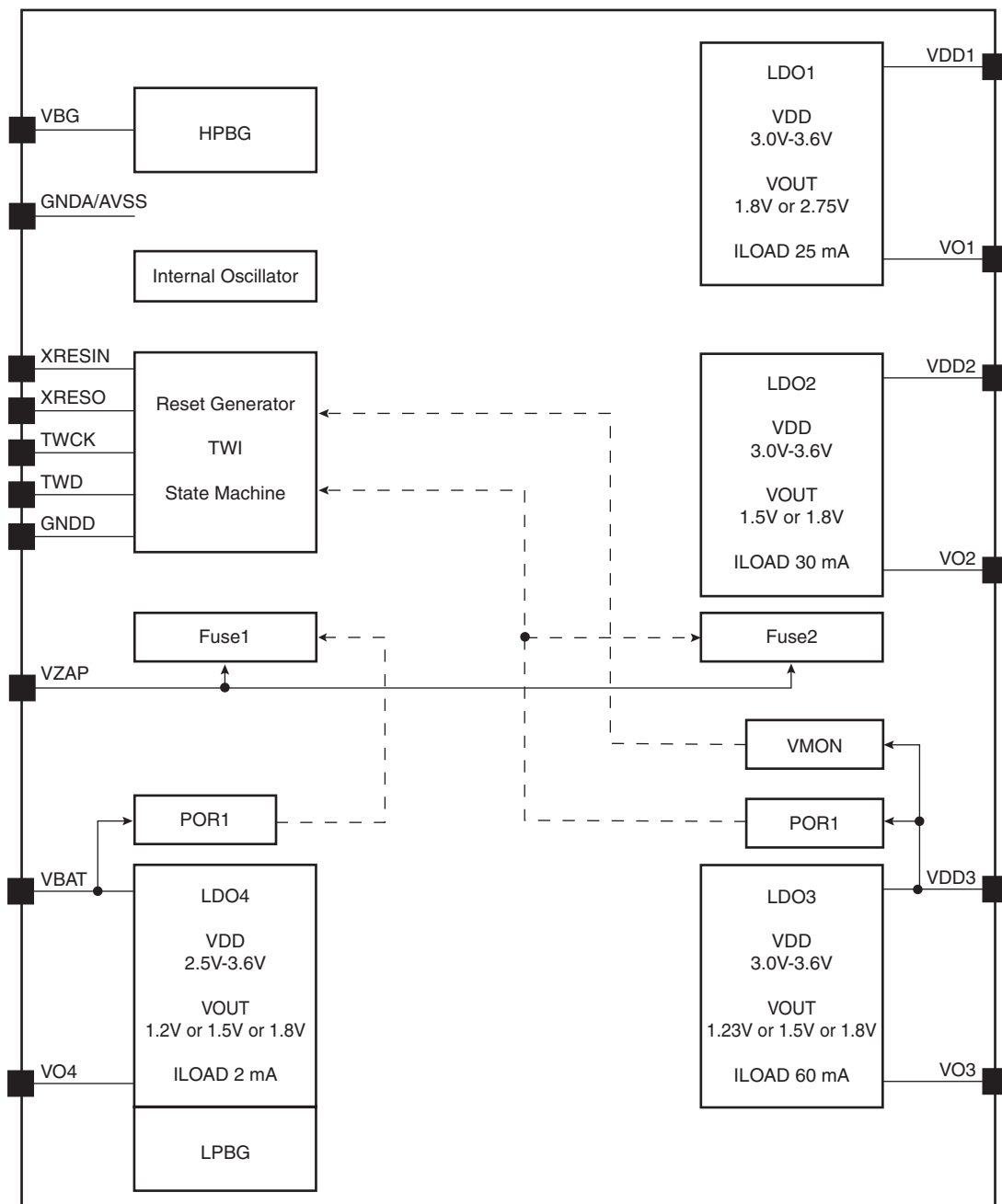
## AT73C239 4-channel Power Management for Wireless Modules

6201C-PMAAC-31-Jul-07



## 2. Block Diagram

**Figure 2-1.** AT73C239 Functional Block Diagram



### 3. Pin Description

**Table 3-1.** Pin Description

| Pin Name             | I/O          | Pin Number | Type    | Function                             |
|----------------------|--------------|------------|---------|--------------------------------------|
| XRESIN               | Input        | 1          | Digital | Reset in pin                         |
| VO3                  | Output       | 2          | Analog  | LDO3 output voltage                  |
| VDD3                 | Input        | 3          | Power   | LDO3 input voltage                   |
| XRESO                | Output       | 4          | Digital | Reset out pin                        |
| VO4                  | Output       | 5          | Analog  | LDO4 output voltage                  |
| GNDD                 | GND          | 6          | Power   | Digital ground                       |
| VBAT                 | Input        | 7          | Power   | LDO4 input voltage                   |
| VZAP <sup>(1)</sup>  | input        | 8          | Digital | Reserved for manufacturing purposes. |
| VDD2                 | Input        | 9          | Power   | LDO2 input voltage                   |
| VO2                  | Output       | 10         | Analog  | LDO2 output voltage                  |
| TWICK <sup>(2)</sup> | Input        | 11         | Digital | TWI input                            |
| TWID <sup>(3)</sup>  | Input/Output | 12         | Digital | TWI input/output                     |
| VDD1                 | Input        | 13         | Power   | LDO1 input voltage                   |
| VO1                  | Output       | 14         | Analog  | LDO1 output voltage                  |
| GNDA/AVSS            | GND/Input    | 15         | Analog  | Analog ground and ESD ground         |
| VBG                  | Output       | 16         | Analog  | Voltage reference for analog cells   |

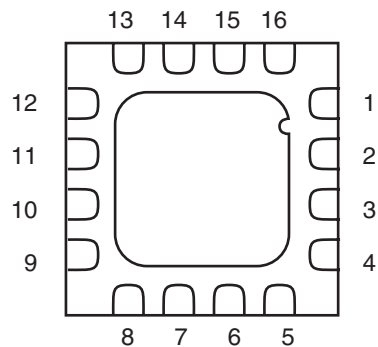
Notes: 1. Connected to ground.  
 2. Connected to VDD1, 2, 3 if TWI is not used.  
 3. Connected to VDD1, 2, 3 if TWI is not used.

## 4. Package

### 4.1 16-pin QFN Package Outline

Figure 4-1 shows the orientation of the 16-pin QFN package.

**Figure 4-1.** 16-pin QFN Package - Bottom View



## 5. Application Block Diagram

Figure 5-1. AT73C239 Application Block Diagram

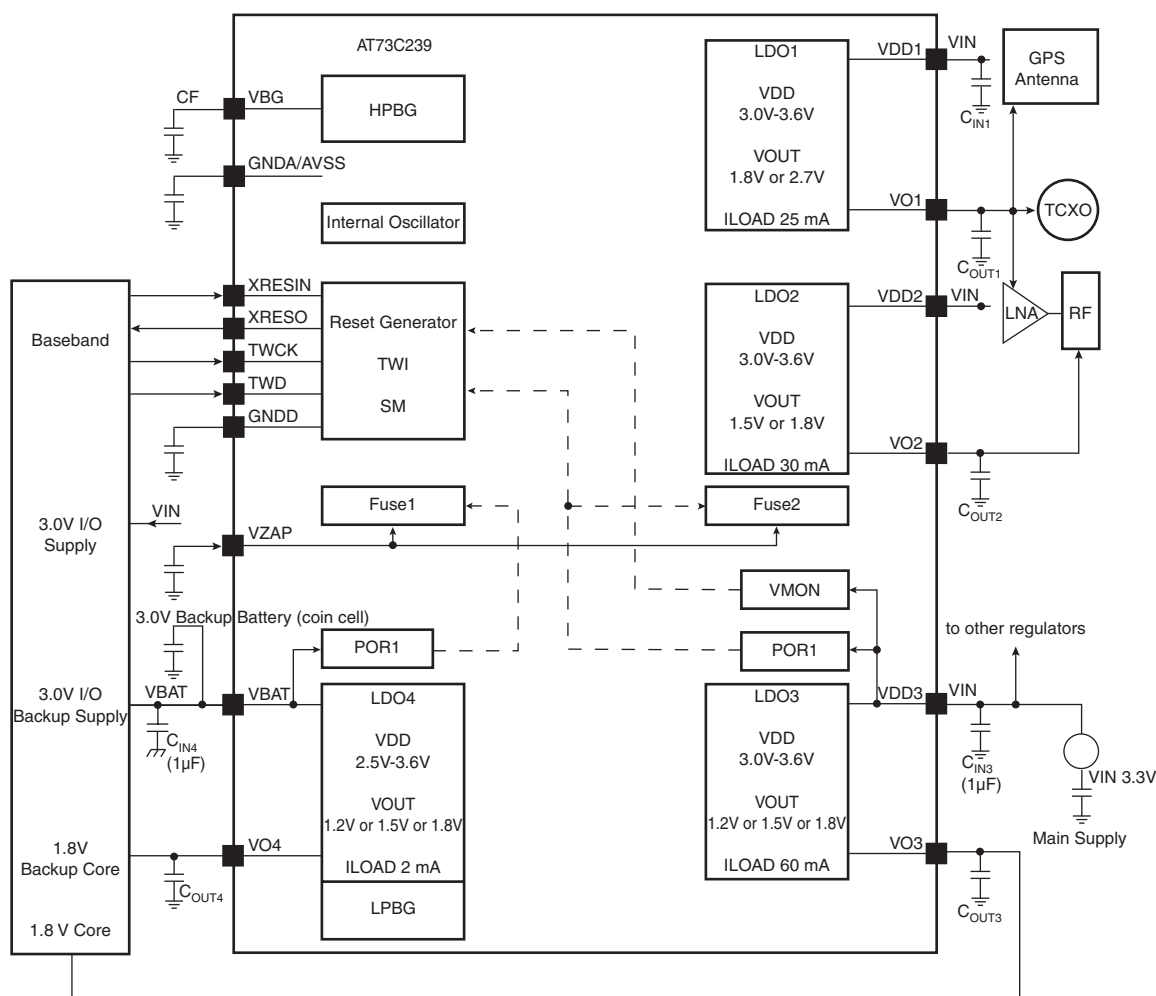


Table 5-1. Application Schematic Reference and Pin Description

| Schematic Reference | Pin  | Description                                |
|---------------------|------|--------------------------------------------|
| C <sub>IN1</sub>    | VDD1 | 1 $\mu$ F $\pm$ 20% Ceramic Capacitor, X5R |
| C <sub>IN2</sub>    | VDD2 |                                            |
| C <sub>IN3</sub>    | VDD3 |                                            |
| C <sub>IN4</sub>    | VBAT |                                            |
| C <sub>OUT1</sub>   | VO1  |                                            |
| C <sub>OUT2</sub>   | VO2  |                                            |
| C <sub>OUT3</sub>   | VO3  |                                            |
| C <sub>OUT4</sub>   | VO4  | 100 nF, $\pm$ 20% Ceramic Capacitor        |
| CF                  | VBG  |                                            |

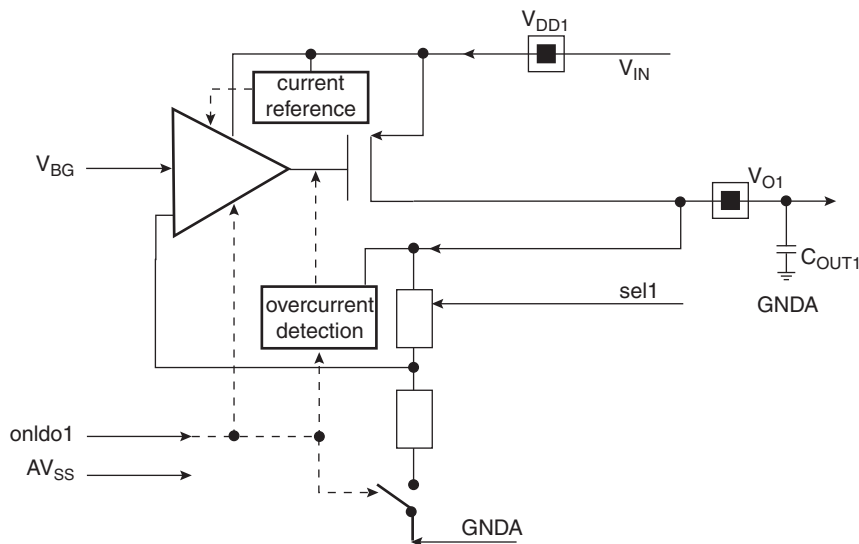
## 6. Functional Description

The AT73C239 integrates the power supply channels described in this section.

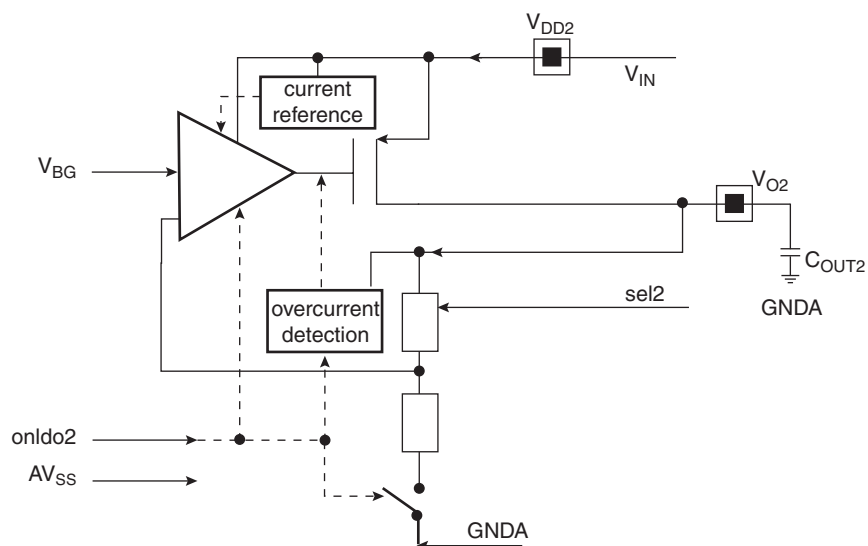
### 6.1 LDO1

LDO1 is a 25 mA/1.8V-2.75V linear low drop out regulator with RF performance. LDO1 operates with supply from 3.0V to 3.6V and requires at least 300 mV of minimum drop-out. LDO1 supplies the RF section of wireless devices, showing high PSRR up to 100 kHz, and very low noise on wide frequency bandwidth. LDO1 requires a 1  $\mu$ F output capacitor.

**Figure 6-1.** LDO1 Functional Diagram



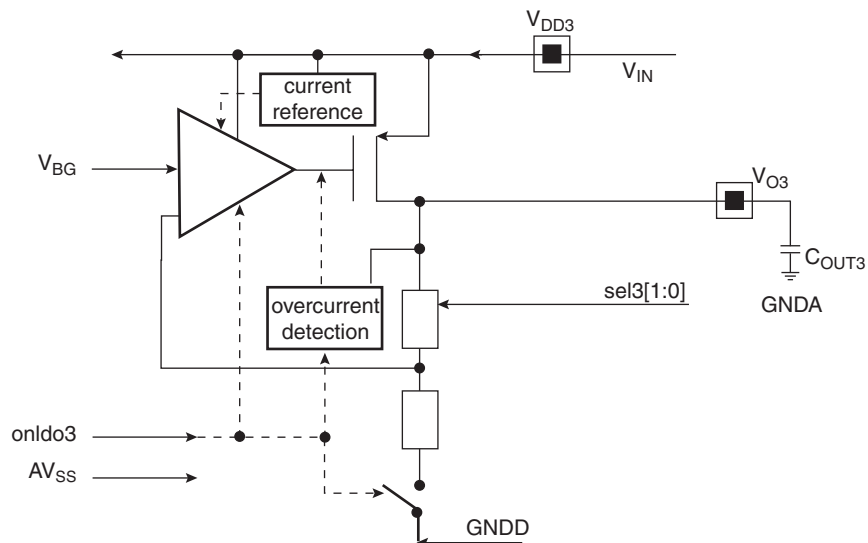
**Figure 6-2.** LDO2 Functional Diagram



## 6.3 LDO3

LDO3 is a 60 mA/1.2V or 1.5V or 1.8V linear low drop out regulator with RF performance. LDO3 operates with supply from 3.0V to 3.6V and needs at least 300 mV of minimum drop-out. LDO3 supplies the RF section of wireless devices, showing high PSRR up to 100 kHz and low noise on wide frequency bandwidth. LDO3 requires a 1  $\mu$ F output capacitor.

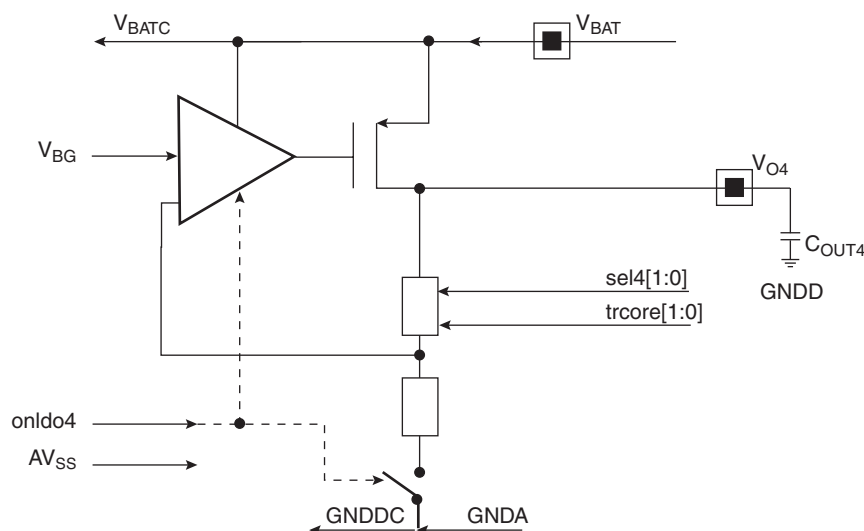
**Figure 6-3.** LDO3 Functional Diagram



## 6.4 LD04

LDO4 is a 2 mA/1.2V or 1.5V or 1.8V low drop out voltage regulator with very low quiescent current. LDO4 operates with supply from 2.5V to 3.6V and needs at least 300 mV of minimum drop-out. LDO4 supplies the very low power section of the wireless baseband. It is usually supplied by the external backup battery and regulates voltage with very low quiescent current, maximizing the lifetime of the backup battery. LDO4 requires a 1  $\mu$ F output capacitor or 470 nF if the load is less than 250  $\mu$ A. LDO4 is always on once the battery is plugged in. The regulator is activated when POR1 is released.

**Figure 6-4.** LDO4 Functional Diagram



## 6.5 High Performance Bandgap (HPBG)

HPBG provides highly accurate, low noise voltage reference to LDOs that supply RF sections. HPBG operates in switching mode, thus decreasing its current consumption. The economic High Performance Bandgap is particularly efficient when RF LDOs are in idle mode (output voltage provided with very low output current e.g. < 1 mA), as the RF section is not active and quiescent current must be decreased as much as possible.

HPBG requires an external 100 nF ceramic capacitor to achieve very low noise high-accuracy voltage reference.

## 6.6 Low Power Bandgap (LPBG)

LPBG is used as reference voltage for LDO4. LPBG starts up as soon as the VBAT pin is active and does not require an external capacitor for decoupling.

## 6.7 Reset Generator

The reset generator produces output reset (XRSTOUT) at least 100 ms after input reset state is activated. Input reset state can be produced the following:

- External manual reset connected to the XRESIN pin
- Internal POR2 monitoring  $V_{IN}$  (on VDD3 pin). POR2 is designed with a maximum threshold at 1.81V.

XRESO pin can be generated only if  $V_{IN}$  is present.

## 6.8 Internal State Machine

The internal state machine manages the start up of the regulators connected to VDD1, VDD2 and VDD3 pins. The startup configuration is in the following order:

1. LDO3
2. LDO1
3. LDO2

## 6.9 Power on Reset on VBAT (POR1)

POR1 monitors the VBAT pin and generates an internal signal (VPOR1) to enable a fuse read operation for LDO4 output voltage programming and LDO4 startup. VPOR1 is released when VBAT is higher than  $1.5V \pm 300\text{ mV}$ .

## 6.10 Power on Reset on VDD3 (POR2)

POR2 monitors the VDD3 pin and generates an internal signal (VPOR2) to reset the internal State Machine and startup the Two-wire Interface (TWI). VPOR2 also enables the fuse read operation for LDO1, LDO2, LDO3 output voltage programming, reference voltage and internal oscillator trimming. VPOR2 is released when  $V_{IN}$  is higher than  $1.5V \pm 300\text{ mV}$ .

## 6.11 Internal Oscillator

The internal oscillator generates the internal master clock to synchronize the state machine that monitors start up of the LDOs and controls HPBG.

## 6.12 Voltage Supply Monitor on VDD3 (VMON)

VMON monitors the VDD3 pin and generates an internal signal to enable the state machine to start up the LDOs and to generate the XRESO signal. Threshold is set to 2.7V at rising and 2.6V at shut down.

## 6.13 Two-wire Interface (TWI)

The TWI can be used to activate, disable and set the output voltage of the LDO1, 2, 3, 4 regulators. ( $V_{DD3}$  must be present in order for TWI to be used with LDO4.)

## 7. Startup Procedure

### At VBAT Rising:

- LPBG automatically starts up.
- POR1 starts up LDO4.

### At VDD3 Rising:

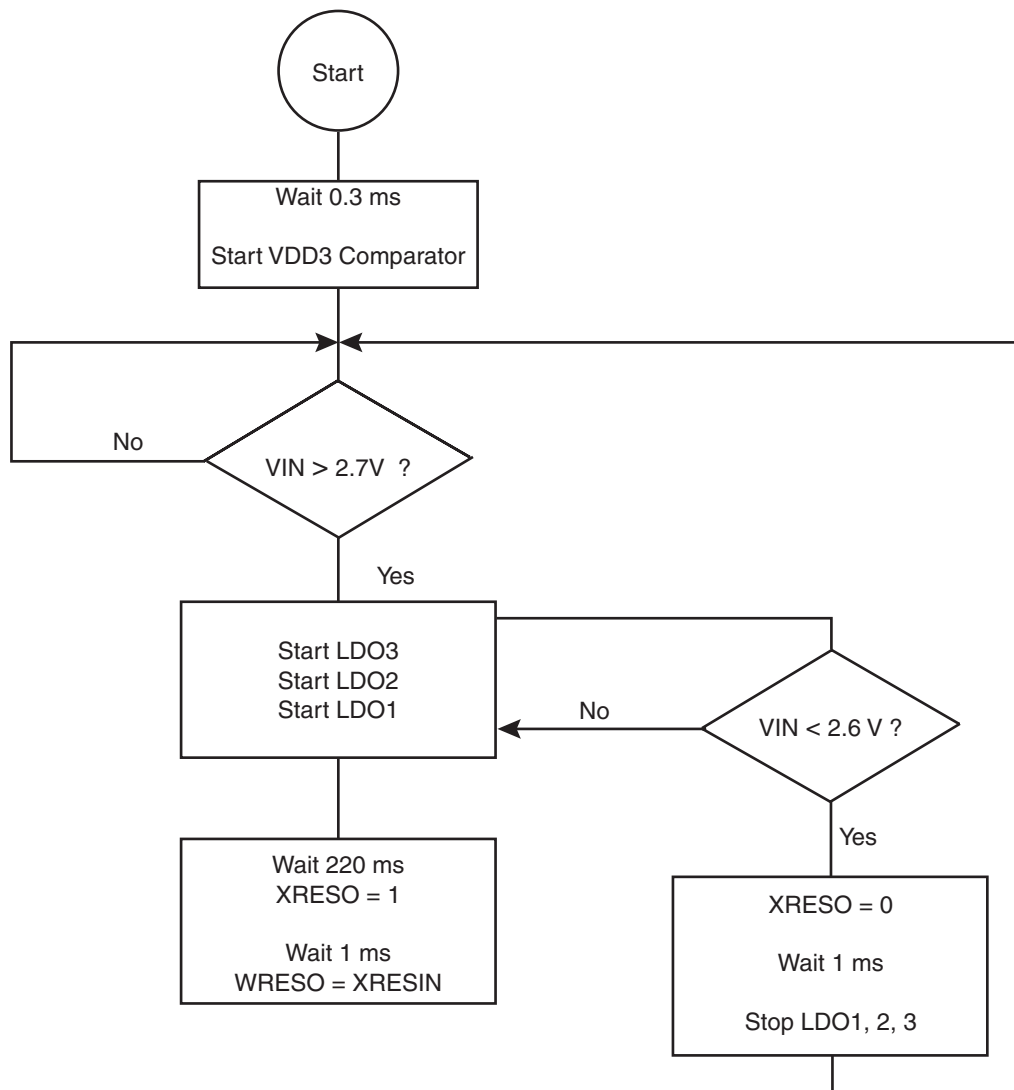
- POR2 enables the following:
  - Supply Monitor with shutdown threshold setup at 2.7V in order to prevent corruption in the baseband chip, when the core is still supplied
  - Internal State machine that enables the other circuits according to the diagram shown in [Figure 7-1 on page 12](#).
  - Two Wire Interface

### At VDD3 Falling:

- The Supply Monitor generates a shut-down control signal when  $V_{DD3}$  reaches 2.6V.
- The State Machine, upon receiving the shut-down control signal, generates the XRESO signal to set the baseband chip in reset mode.
- The State Machine switches off LDO1, LDO2 and LDO3. HPBG is kept on in order to provide a fast startup of the LDOs in case of glitches on  $V_{DD3}$ .

## 7.1 Startup Diagram

Figure 7-1. Startup Diagram



POR2, supplied by  $V_{DD3}$ , resets the startup state machine. After 0.3 ms, the  $V_{DD3}$  comparator is started. If  $V_{DD3}$  is greater than 2.7V, LDO regulators are started in the following order: LDO3, LDO2, LDO1. During LDO regulator  $V_{DD}$  startup, voltage is not checked.

Then XRESO is kept grounded for 220 ms, tied high for 1 ms, before following XRESIN. During that state,  $V_{DD3}$  voltage is monitored and if it is lower than 2.6V, LDO regulators 1, 2 and 3 are stopped and XRESO is grounded.

Both XRESIN and  $V_{DD3}$  comparator output are debounced at rising and falling edges for two 10 kHz clock cycles. Debounce time is typically between 100  $\mu$ s and 200  $\mu$ s. Timings are defined  $\pm 40\%$ .

## 8. Normal Procedure

The State Machine monitors the XRESIN pin and provides the proper XRESO pin signal when reset occurs.

Through the Two-wire Interface (TWI), the user can control and change the output voltage delivered by LDO1, LDO2, LDO3 and LDO4.

## 9. Two-wire Interface (TWI) Protocol

The two-wire interface interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds up to 400 Kbits per second, based on a byte oriented transfer format. The TWI is slave only and has single byte access.

The TWI adds flexibility to the power supply solution, enabling LDO regulators to be controlled depending on the instantaneous application requirements.

The AT73C239 has the following 7-bit address: **1001000**.

Attempting to read data from register addresses not listed in this section results in 0xFF being read out.

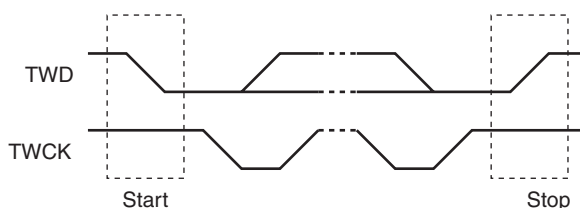
- TWCK is an input pin for the clock
- TWD is an open-drain pin driving or receiving the serial data

The data put on TWD line must be 8 bits long. Data is transferred MSB first. Each byte must be followed by an acknowledgement.

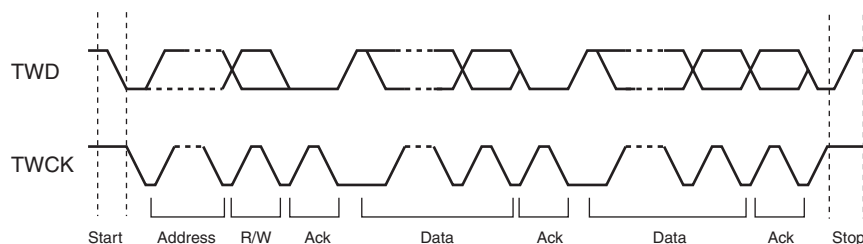
Each transfer begins with a START condition and terminates with a STOP condition.

- A high-to-low transition on TWD while TWCK is high defines a START condition.
- A low-to-high transition on TWD while TWCK is high defines a STOP condition.

**Figure 9-1.** START and STOP Conditions



**Figure 9-2.** Transfer Format

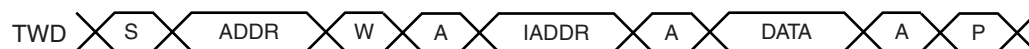


After the host initiates a START condition, it sends the 7-bit slave address defined above to notify the slave device. A read/write bit follows (read = 1, write = 0).

The device acknowledges each received byte. The first byte sent after the device address and the R/W bit, is the address of the device register the host wants to read or write.

For a write operation the data follows the internal address. For a read operation a repeated START condition needs to be generated followed by a read on the device.

**Figure 9-3.** Write Operation



**Figure 9-4.** Read Operation



- S = Start
- P = Stop
- W = Write
- R = Read
- A = Acknowledge
- N = Not Acknowledge
- DADR= Device Address
- IADR = Internal Address

## 10. Normal Modes and Quiescent Current

**Table 10-1.** Normal Modes and Quiescent Current

| Modes          | Conditions                                                                       | Quiescent [ $\mu$ A] |     |
|----------------|----------------------------------------------------------------------------------|----------------------|-----|
|                |                                                                                  | typ                  | max |
| Backup Battery | $V_{BAT}$ present, $V_{DD3}$ not present<br>LDO4 on                              | 10                   | 30  |
| Normal         | $V_{BAT}$ present, $V_{DD3}$ present<br>LDO4 on<br>LDO1 on<br>LDO2 on<br>LDO3 on | 800                  |     |

## 11. Electrical Characteristics

### 11.1 Absolute Maximum Ratings

**Table 11-1.** Absolute Maximum Ratings

|                                                                                    |                  |
|------------------------------------------------------------------------------------|------------------|
| Operating Temperature (Industrial).....                                            | -40° C to +85° C |
| Storage Temperature .....                                                          | -55°C to +150°C  |
| Power Supply Input on V <sub>BAT</sub> .....                                       | -0.3V to + 3.6V  |
| Power Supply Input on V <sub>DD1</sub> , V <sub>DD2</sub> , V <sub>DD3</sub> ..... | -0.3V to + 3.6V  |
| Digital IO Input Voltage .....                                                     | -0.3V to + 3.6V  |
| TWI IO Input Voltage .....                                                         | -0.3V to + 5.5V  |
| All Other Pins.....                                                                | -0.3V to + 3.6V  |

**\*NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

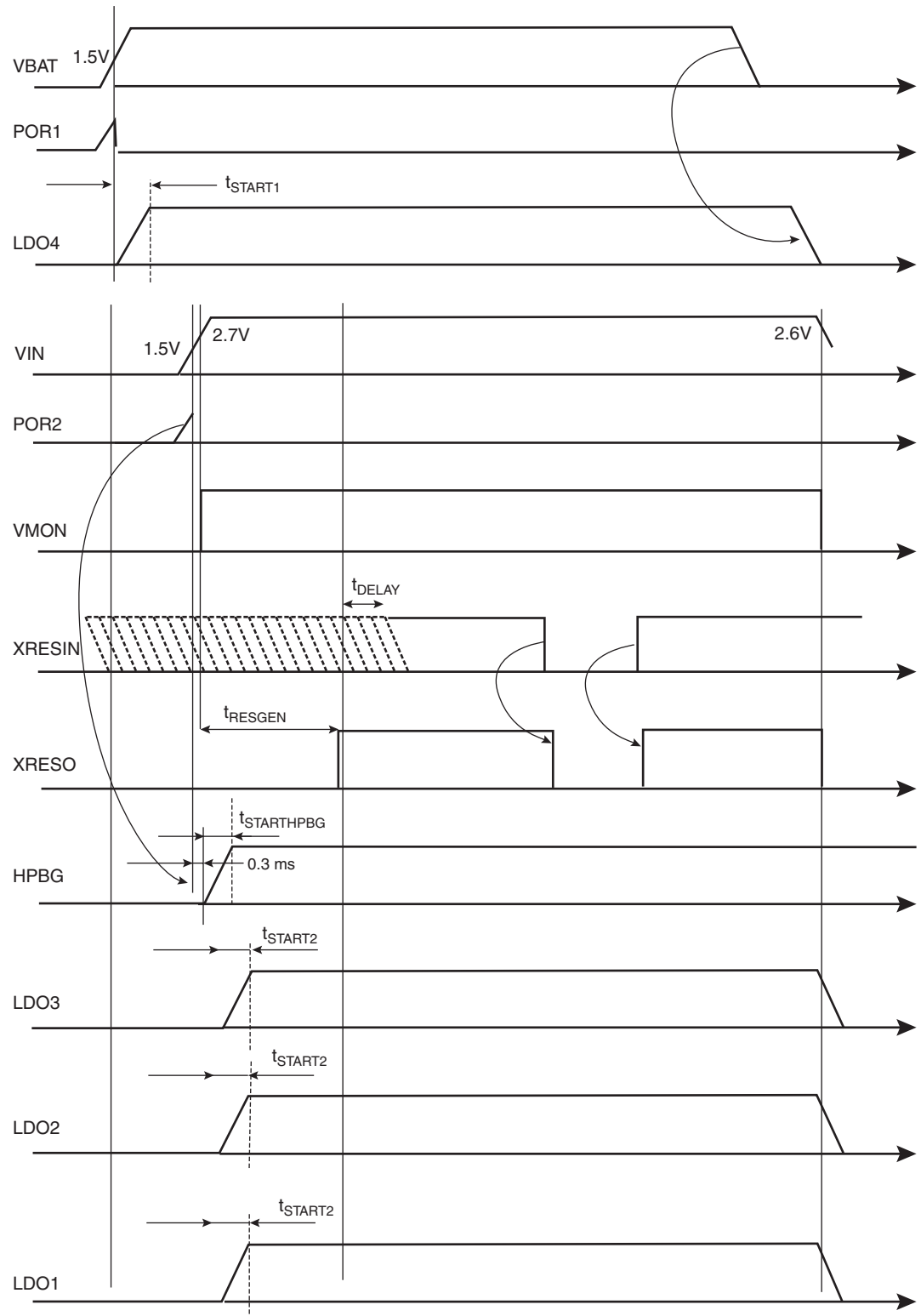
### 11.2 Recommended Operating Conditions

**Table 11-2.** Recommended Operating Conditions

| Parameter             | Condition                                              | Min | Max | Unit |
|-----------------------|--------------------------------------------------------|-----|-----|------|
| Operating Temperature |                                                        | -40 | 85  | °C   |
| Power Supply Input    | V <sub>DD1</sub> , V <sub>DD2</sub> , V <sub>DD3</sub> | 3.0 | 3.6 | V    |
|                       | V <sub>BAT</sub>                                       | 2.5 | 3.6 |      |

## 12. Timing Diagram

Figure 12-1. AT73C239 Timings



At  $V_{DD3}$  startup XRESIN is taken into account only if it occurs after  $t_{DELAY}$ .

**Table 12-1.** Timing Parameters

| Parameter       | Signal                   | Constraint              | Min | Max | Unit            |
|-----------------|--------------------------|-------------------------|-----|-----|-----------------|
| $t_{START1}$    | $V_{O4}$                 | LDO4 Startup time       | 10  | 100 | $\mu\text{sec}$ |
| $t_{START2}$    | $V_{O1}, V_{O2}, V_{O3}$ | LDO1,2,3 Startup time   | 10  | 100 | $\mu\text{sec}$ |
| $t_{STARTHPBG}$ | $V_{BG}$                 | HPBG startup time       |     | 2   | ms              |
| $t_{REGEN}$     | XRESOUT                  | Delay to XRESOUT active | 100 | 500 | ms              |
| $t_{DELAY}$     |                          |                         |     | 1   | ms              |

## 13. Electrical Specification

### 13.1 LD01

**Table 13-1.** LD01 Parametric Table

| Symbol            | Parameter                    | Comments                                                  | Min  | Typ  | Max  | Units                  |
|-------------------|------------------------------|-----------------------------------------------------------|------|------|------|------------------------|
| $V_{DD1}$         | Operating supply voltage     | Switching Regulated                                       | 3.0  | 3.3  | 3.6  | V                      |
| $V_{O1}$          | Output voltage               | Factory programmed                                        | 2.70 | 2.75 | 2.80 | V                      |
|                   |                              | Programmable                                              | 1.75 | 1.8  | 1.85 | V                      |
| $I_1$             | Load current                 |                                                           |      |      | 25   | mA                     |
| $I_{QC}$          | Quiescent current            |                                                           |      |      | 300  | $\mu$ A                |
| $I_{SC}$          | Shutdown current             | HiZ output                                                |      |      | 1    | $\mu$ A                |
| $I_{SH}$          | Short circuit current        |                                                           |      | 200  |      | mA                     |
| $t_R$             | Startup time                 |                                                           |      |      | 100  | $\mu$ s                |
| $\Delta V_{DC}$   | Line regulation static       | From 3.0V to 3.6V                                         |      | 2    |      | mV                     |
| $\Delta V_{DC}$   | Load regulation static       | From 10% to 100% $I_1$                                    |      | 2    |      | mV                     |
|                   |                              | From 0 to 100% $I_1$                                      |      | 7    |      |                        |
| $\Delta V_{TRAN}$ | Line regulation dynamic      | From 3.1V to 3.6V<br>$t_R = t_F = 5 \mu$ s, $I_1 = 5$ mA  |      | 2    |      | mV                     |
| $\Delta V_{TRAN}$ | Load regulation dynamic      | From 10% to 100%<br>$I_1$ , $t_R = t_F = 5 \mu$ s,        |      | 2.5  |      | mV                     |
| PSRR              | Power Supply Rejection Ratio | Sine Wave, 100 kHz frequency,<br>3.3V mean 200 m $V_{PP}$ |      | 48   |      | dB                     |
|                   |                              | Sine Wave, 10 kHz frequency,<br>3.3V mean, 200 m $V_{PP}$ |      | 55   |      | dB                     |
|                   |                              | Sine Wave, 1 kHz frequency,<br>3.3V mean 200 m $V_{PP}$   |      | 60   |      | dB                     |
| $\Delta V_{OUT}$  | StartUp Overshoot            |                                                           |      | 40   |      | mV                     |
| $V_N$             | Output Noise                 | 10 Hz - 100 kHz                                           |      | 45   |      | $\mu$ V <sub>RMS</sub> |
| $V_{NT}$          | Total Output Noise           | 10 Hz - 100 kHz                                           |      | 55   |      | $\mu$ V <sub>RMS</sub> |

**Table 13-2.** LD01 External Components

| Schematic Reference | Description                               |
|---------------------|-------------------------------------------|
| $C_{OUT1}$          | X5R 1 $\mu$ F $\pm$ 20% ceramic capacitor |

**Table 13-3.** Control Modes

| onldo1 | sel1 | VO1   |
|--------|------|-------|
| 0      | 0    | HiZ   |
| 1      | 0    | 2.75V |
| 1      | 1    | 1.8V  |

## 13.2 LDO2

**Table 13-4.** LDO2 Parametric Table

| Symbol            | Parameter                    | Comments                                                  | Min  | Typ | Max  | Units                  |
|-------------------|------------------------------|-----------------------------------------------------------|------|-----|------|------------------------|
| $V_{DD2}$         | Operating supply voltage     | Switching Regulated                                       | 3.0  | 3.3 | 3.6  | V                      |
| $V_{O2}$          | Output voltage               | Factory programmed                                        | 1.75 | 1.8 | 1.85 | V                      |
|                   |                              | Programmable                                              | 1.45 | 1.5 | 1.55 | V                      |
| $I_2$             | Load current                 |                                                           |      |     | 30   | mA                     |
| $I_{QC}$          | Quiescent current            |                                                           |      |     | 300  | $\mu$ A                |
| $I_{SC}$          | Shutdown current             | HiZ output                                                |      |     | 1    | $\mu$ A                |
| $I_{SH}$          | Short circuit current        |                                                           |      | 200 |      | mA                     |
| $t_R$             | Startup time                 |                                                           |      |     | 100  | $\mu$ s                |
| $\Delta V_{DC}$   | Line regulation static       | From 3.0V to 3.6V                                         |      | 2   |      | mV                     |
| $\Delta V_{DC}$   | Load regulation static       | From 10% to 100% $I_2$                                    |      | 2   |      | mV                     |
|                   |                              | From 0 to 100% $I_2$                                      |      | 3   |      |                        |
| $\Delta V_{TRAN}$ | Line regulation dynamic      | From 3.1V to 3.6V<br>$t_R = t_F = 5 \mu$ s, $I_2 = 30$ mA |      | 2   |      | mV                     |
| $\Delta V_{TRAN}$ | Load regulation dynamic      | From 10% to 100%<br>$I_1$ , $t_R = t_F = 5 \mu$ s,        |      | 3   |      | mV                     |
| PSRR              | Power Supply Rejection Ratio | Sine Wave, 100 kHz frequency,<br>3.3V mean 200 m $V_{PP}$ |      | 40  |      | dB                     |
|                   |                              | Sine Wave, 10 kHz frequency,<br>3.3V mean, 200 m $V_{PP}$ |      | 50  |      | dB                     |
|                   |                              | Sine Wave, 1 kHz frequency,<br>3.3V mean 200 m $V_{PP}$   |      | 70  |      | dB                     |
| $\Delta V_{OUT}$  | Startup Overshoot            |                                                           |      | 30  |      | mV                     |
| $V_N$             | Output Noise                 | 10 Hz - 100 kHz                                           |      | 35  |      | $\mu$ V <sub>RMS</sub> |
| $V_{NT}$          | Total Output Noise           | 10 Hz - 100 kHz                                           |      | 45  |      | $\mu$ V <sub>RMS</sub> |

**Table 13-5.** External Components

| Schematic Reference | Description                               |
|---------------------|-------------------------------------------|
| $C_{OUT2}$          | X5R 1 $\mu$ F $\pm$ 20% ceramic capacitor |

**Table 13-6.** Control Modes

| on2ldo | sel2 | VO2  |
|--------|------|------|
| 0      | X    | HiZ  |
| 1      | 0    | 1.8V |
| 1      | 1    | 1.5V |

### 13.3 LDO3

**Table 13-7.** LDO3 Parametric Table

| Symbol            | Parameter                    | Comments                                                  | Min  | Typ  | Max  | Units                  |
|-------------------|------------------------------|-----------------------------------------------------------|------|------|------|------------------------|
| $V_{DD3}$         | Operating supply voltage     | Switching Regulated                                       | 3.0  | 3.3  | 3.6  | V                      |
| $V_{O3}$          | Output voltage               | Factory programmed                                        | 1.75 | 1.8  | 1.85 | V                      |
|                   |                              | Programmable                                              | 1.45 | 1.5  | 1.55 | V                      |
|                   |                              | Programmable                                              | 1.18 | 1.23 | 1.28 | V                      |
| $I_3$             | Load current                 |                                                           |      |      | 60   | mA                     |
| $I_{QC}$          | Quiescent current            |                                                           |      |      | 300  | $\mu$ A                |
| $I_{SC}$          | Shutdown current             | HiZ output                                                |      |      | 1    | $\mu$ A                |
| $I_{SH}$          | Short circuit current        |                                                           |      | 200  |      | mA                     |
| $t_R$             | Startup time                 |                                                           |      |      | 100  | $\mu$ s                |
| $\Delta V_{DC}$   | Line regulation static       | From 3.0V to 3.6V                                         |      | 2    |      | mV                     |
| $\Delta V_{DC}$   | Load regulation static       | From 10% to 100% $I_3$                                    |      | 2    |      | mV                     |
|                   |                              | From 0 to 100% $I_3$                                      |      | 3    |      |                        |
| $\Delta V_{TRAN}$ | Line regulation dynamic      | From 3.1V to 3.6V<br>$t_R = t_F = 5 \mu$ s, $I_3 = 60$ mA |      | 2    |      | mV                     |
| $\Delta V_{TRAN}$ | Load regulation dynamic      | From 10% to 100%<br>$I_1$ , $t_R = t_F = 5 \mu$ s,        |      | 3    |      | mV                     |
| PSRR              | Power Supply Rejection Ratio | Sine Wave, 100 kHz frequency,<br>3.3V mean 200 m $V_{PP}$ |      | 40   |      | dB                     |
|                   |                              | Sine Wave, 10 kHz frequency,<br>3.3V mean, 200 m $V_{PP}$ |      | 50   |      | dB                     |
|                   |                              | Sine Wave, 1 kHz frequency,<br>3.3V mean 200 m $V_{PP}$   |      | 70   |      | dB                     |
| $\Delta V_{OUT}$  | Startup Overshoot            |                                                           |      | 30   |      | mV                     |
| $V_N$             | Output Noise                 | 10 Hz - 100 kHz, without $V_{BG}$                         |      | 35   |      | $\mu$ V <sub>RMS</sub> |
| $V_{NT}$          | Total Output Noise           | 10 Hz - 100 kHz                                           |      | 45   |      | $\mu$ V <sub>RMS</sub> |

**Table 13-8.** External Components

| Schematic Reference | Description                               |
|---------------------|-------------------------------------------|
| $C_{OUT3}$          | X5R 1 $\mu$ F $\pm$ 20% ceramic capacitor |

**Table 13-9.** Control Modes

| onldo3 | sel3[0] | sel3[1] | VO3   |
|--------|---------|---------|-------|
| 0      | X       | X       | HiZ   |
| 1      | 0       | 0       | 1.8V  |
| 1      | 1       | 0       | 1.5V  |
| 1      | 0       | 1       | 1.23V |

## 13.4 LDO4

LDO4 generates 1.2V, 1.5V or 1.8V voltage from VBAT supply. Max DC load is 2 mA. The regulator is activated when POR1 is released.

**Table 13-10.** LDO4 Parametric Table

| Symbol          | Parameter                | Conditions                 | Min | Typ | Max | Unit    |
|-----------------|--------------------------|----------------------------|-----|-----|-----|---------|
| $V_{BAT}$       | Operating supply voltage | Backup Battery or Supercap | 2.5 |     | 3.6 | V       |
| $V_{O4}$        | Output voltage           | Factory programmed         | 1.7 | 1.8 | 1.9 | V       |
|                 |                          | Programmable               | 1.4 | 1.5 | 1.6 | V       |
|                 |                          | Programmable               | 1.1 | 1.2 | 1.3 | V       |
| $I_4$           | Load current             | DC load current            |     |     | 2   | mA      |
| $I_{QC}$        | Quiescent current        |                            |     | 3   | 5   | $\mu A$ |
| $I_{SC}$        | Shutdown current         |                            |     |     | 0.5 | $\mu A$ |
| $t_S$           | Startup time             |                            |     |     | 200 | $\mu s$ |
| $\Delta V_{DC}$ | Line regulation static   | $2.5V < V_{BAT} < 3.6V$    |     |     | 100 | mV      |
| $\Delta V_{DC}$ | Load regulation static   | $0 < I_4 < 2 \text{ mA}$   |     |     | 100 | mV      |

**Table 13-11.** LDO4 External Components

| Schematic Reference | Description                      |
|---------------------|----------------------------------|
| $C_{OUT4}$          | X5R 1 $\mu F \pm 20\%$ capacitor |

**Table 13-12.** onldo4 sel4[1:0] Control Modes

| onldo4 | sel4<1> | sel4<0> | VO4  |
|--------|---------|---------|------|
| 0      | X       | X       | HiZ  |
| 1      | 0       | 0       | 1.8V |
| 1      | 0       | 1       | 1.5V |
| 1      | 1       | 0       | 1.2V |

**Table 13-13.** trcore[1:0] Control Modes

| trcore<1> | trcore<0> | VO4     |
|-----------|-----------|---------|
| 0         | 0         | typ     |
| 0         | 1         | + 80mV  |
| 1         | 0         | - 80 mV |
| 1         | 1         |         |

## 13.5 High Performance Bandgap (HPBG)

**Table 13-14.** HPBG Parametric Table

| Symbol          | Parameter                    | Conditions                     | Min | Typ   | Max | Units             |
|-----------------|------------------------------|--------------------------------|-----|-------|-----|-------------------|
| V <sub>BG</sub> | Output voltage               | Factory trimmed                |     | 1.231 |     | V                 |
| I <sub>SC</sub> | Shutdown current             | encore = en = 0, dcrun = 0 (1) |     | 1     | 6   | μA                |
| I <sub>QC</sub> | Quiescent current            |                                |     |       | 30  | μA                |
| t <sub>S</sub>  | Startup time                 | C <sub>F</sub> = 100 nF        |     | 1     | 2   | ms                |
| V <sub>N</sub>  | Output noise                 | BW 10 Hz to 100 kHz            |     | 7     |     | μV <sub>RMS</sub> |
| PSRR            | Power Supply Rejection Ratio | F = 100 Hz                     |     | 65    |     | dB                |

**Table 13-15.** External Components

| Schematic Reference | Description                                |
|---------------------|--------------------------------------------|
| C <sub>F</sub>      | X5R 100 nF ± 20% ceramic capacitor minimum |

## 13.6 Low Power Bandgap (LPBG)

**Table 13-16.** LPBG Parametric Table

| Symbol            | Parameter                | Conditions                 | Min  | Typ | Max  | Unit |
|-------------------|--------------------------|----------------------------|------|-----|------|------|
| V <sub>BAT</sub>  | Operating supply voltage | Backup Battery or Supercap | 2.5  |     | 3.6  | V    |
| I <sub>QC</sub>   | Quiescent current        |                            |      | 4   | 7.5  | μA   |
| t <sub>S</sub>    | Startup time             |                            |      |     | 100  | μs   |
| V <sub>LPBG</sub> | Bandgap Voltage          |                            | 1.15 | 1.2 | 1.25 | V    |

## 13.7 Power On Reset on VBAT (POR1)

**Table 13-17.** POR1 Parametric Table

| Symbol            | Parameter                | Conditions                 | Min | Typ  | Max | Unit |
|-------------------|--------------------------|----------------------------|-----|------|-----|------|
| V <sub>BAT</sub>  | Operating supply voltage | Backup Battery or Supercap | 2.5 |      | 3.6 | V    |
| I <sub>QC</sub>   | Quiescent current        |                            |     | 3    |     | μA   |
| V <sub>PON</sub>  | POR1 on threshold        |                            |     | 1.45 |     | V    |
| V <sub>POFF</sub> | POR1 off threshold       |                            |     | 1.5  |     | V    |

## 13.8 Power On Reset on VDD3 (POR2)

**Table 13-18.** POR2 Parametric Table

| Symbol            | Parameter                | Conditions          | Min | Typ  | Max | Unit |
|-------------------|--------------------------|---------------------|-----|------|-----|------|
| V <sub>DD3</sub>  | Operating supply voltage | Switching regulated | 0   |      | 3.6 | V    |
| I <sub>QC</sub>   | Quiescent current        |                     |     | 3    |     | μA   |
| V <sub>PON</sub>  | POR2 on threshold        |                     |     | 1.45 |     | V    |
| V <sub>POFF</sub> | POR1 off threshold       |                     |     | 1.5  |     | V    |

## 13.9 Voltage Monitor

**Table 13-19.** Voltage Monitor Parametric Table

| Symbol     | Parameter          | Conditions   | Min | Typ | Max  | Unit    |
|------------|--------------------|--------------|-----|-----|------|---------|
| $I_{QC}$   | Quiescent current  |              |     |     | 20   | $\mu A$ |
| $V_{PON}$  | POR2 on threshold  | on $V_{DD3}$ | 2.7 |     | 2.72 | V       |
| $V_{POFF}$ | POR1 off threshold | on $V_{DD3}$ | 2.6 |     | 2.60 | V       |

## 13.10 XRESIN

**Table 13-20.** XRESIN Parametric Table

| Symbol | Parameter                  | Conditions                           | Min | Typ       | Max | Unit |
|--------|----------------------------|--------------------------------------|-----|-----------|-----|------|
| $V_I$  | Input supply voltage range | driven by CPU GPIO                   | 1.8 |           | 3.3 | V    |
|        |                            | driven by CPU open drain output      |     | Hiz       |     | V    |
|        |                            | connected to $V_{DD3}$ when not used |     | $V_{DD3}$ |     | V    |

## 13.11 XRESO

**Table 13-21.** XRESO Parametric Table

| Symbol | Parameter                  | Conditions | Min | Typ | Max | Unit |
|--------|----------------------------|------------|-----|-----|-----|------|
| $V_I$  | Input supply voltage range |            | 1.8 |     | 3.3 | V    |

## 13.12 TWICK

**Table 13-22.** TWICK Parametric Table

| Symbol | Parameter                  | Conditions | Min | Typ | Max | Unit |
|--------|----------------------------|------------|-----|-----|-----|------|
| $V_I$  | Input supply voltage range |            | 1.8 |     | 5.5 | V    |

## 13.13 TWID

**Table 13-23.** TWID Parametric Table

| Symbol | Parameter                  | Conditions | Min | Typ | Max | Unit |
|--------|----------------------------|------------|-----|-----|-----|------|
| $V_I$  | Input supply voltage range |            | 1.8 |     | 5.5 | V    |

## 14. AT73C239 User Interface

**Table 14-1.** AT73C239 Register Mapping

| Offset | Register  | Register Description | Access     | Reset Value |
|--------|-----------|----------------------|------------|-------------|
| 0x00   | LDO_CTRL  | LDO Control          | Read/Write | 0x0F        |
| 0x08   | LDO_TRIM1 | LDO 1,2,3 Trim       | Read/Write | 0x00        |
| 0x0A   | LDO_TRIM4 | LDO4 Trim            | Read/Write | 0x00        |

## 14.1 LDO Control Register

**Register Name:** LDO\_CTRL

**Reset State:** 0X0F

**Access:** Read/Write

|   |   |   |   |        |        |        |        |
|---|---|---|---|--------|--------|--------|--------|
| 7 | 6 | 5 | 4 | 3      | 2      | 1      | 0      |
| – | – | – | – | Onldo4 | Onldo3 | Onldo2 | Onldo1 |

- **Onldo1:**

LDO1 enable (active high) reset value = 1.

- **Onldo2:**

LDO2 enable (active high) reset value = 1.

- **Onldo3:**

LDO3 enable (active high) reset value = 1.

- **Onldo4:**

LDO4 enable (active high) reset value = 1.

## 14.2 LDO 1, 2, 3 Trim Register

**Register Name:** LDO\_TRIM1

**Reset State:** 0X08

**Access:** Read/Write

|   |   |   |      |      |      |   |   |
|---|---|---|------|------|------|---|---|
| 7 | 6 | 5 | 4    | 3    | 2    | 1 | 0 |
| – | – | – | Sel1 | Sel2 | Sel3 |   | – |

- **Sel3**

LDO3 output voltage select, reset = 00

- **Sel2**

LDO2 output voltage select, reset = 0

- **Sel1**

LDO1 output voltage select, reset = 0

| Sel1 | VO1   | Sel2 | VO2  | Sel3 | VO3   |
|------|-------|------|------|------|-------|
| 0    | 2.75V | 0    | 1.8V | 00   | 1.8V  |
| 1    | 1.8V  | 1    | 1.5V | 01   | 1.5V  |
|      |       |      |      | 10   | 1.23V |
|      |       |      |      | 11   | 1.8V  |

### 14.3 LDO 4 Trim Register

**Register Name:** LDO\_TRIM4

**Reset State:** 0X0A

**Access:** Read/Write

|   |   |   |   |      |   |   |   |
|---|---|---|---|------|---|---|---|
| 7 | 6 | 5 | 4 | 3    | 2 | 1 | 0 |
| – | – | – | – | Sel4 |   | – | – |

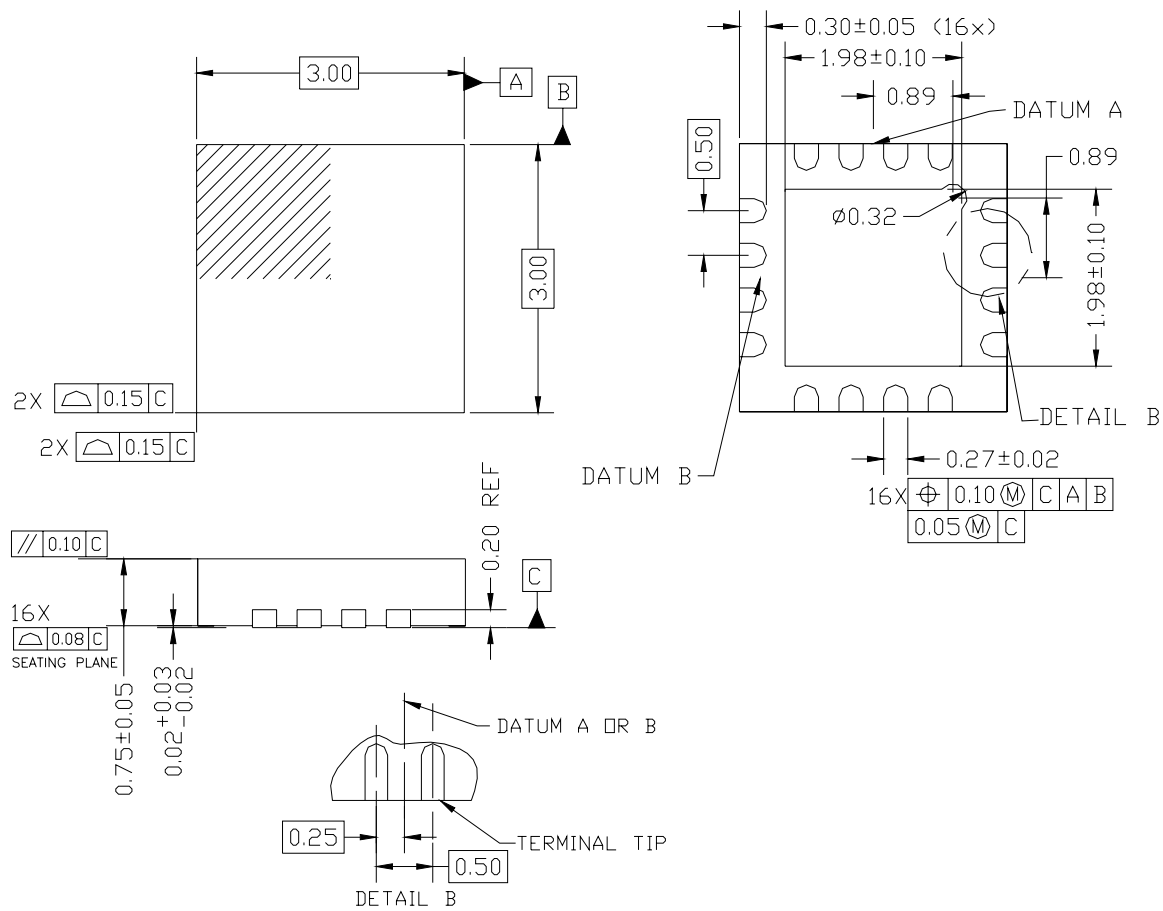
- **Sel4**

LDO4 output voltage select, reset = 00

| Sel4 | VO4  |
|------|------|
| 00   | 1.8V |
| 01   | 1.5V |
| 10   | 1.2V |
| 11   | 1.2V |

## 15. Package Information

**Figure 15-1.** Mechanical Package Drawing for 16-lead Quad Flat No Lead Package



Note: All dimensions are in mm.

## 16. Ordering Information

**Table 16-1.** Ordering Information

| Ordering Code | Package   | Package Type | Temperature Operating Range |
|---------------|-----------|--------------|-----------------------------|
| AT73C239      | QFN3x3 mm | Green        | 0°C to +70°C                |

## Revision History

| Doc. Rev | Date                   | Comments                                                                                                                                                                                                                                                                                                                                                                                                                        | Change Request Ref. |
|----------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|
| 6201A    | 01-Sep-05<br>11-Oct-05 | First issue<br>Unqualified on Intranet                                                                                                                                                                                                                                                                                                                                                                                          |                     |
| 6201B    | 03-Mar-06              | Changed HPBG minimum requirement information in <a href="#">Section 6.5 "High Performance Bandgap (HPBG)"</a> on page 9.<br>Updated <a href="#">Figure 7-1 on page 12</a> with new values.<br>Updated <a href="#">Figure 12-1 on page 17</a> with new information for LDO2 and LDO3 signals.<br>Updated <a href="#">Table 13-14, "HPBG Parametric Table,"</a> on page 23 with max value for startup time and changed condition. | 2472                |
| 6201C    | 09-Jul-07              | Added <a href="#">Section 4. "Package"</a> on page 4.                                                                                                                                                                                                                                                                                                                                                                           | 4591                |



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