Features

- LEON2-FT Sparc V8 Processor
  - 5 stage pipeline
  - 4K instruction caches / 4K data caches
  - Meiko FPU
  - Interrupt Controller
  - Uart serial links
  - 32-bit Timers
  - Memory interface
  - General purpose IO
  - Debug Support Unit (DSU)
- FIFO interface
- ADC/DAC interface
  - 24 channels
  - 8bit/16bit wide data bus
- Two CAN interface
- Two Bidirectional SpaceWire links
  - Full duplex communication
  - Transmit rate from 1.25 up to 200 Mbit/s in each direction
- SpaceWire Link Performance
  - At 3.3V : 200Mbit/s full duplex communication
- JTAG Interface
- Operating range
  - Voltages
    - 1.65V to 1.95V - core
    - 3V to 3.6V - I/O
  - Temperature
    - - 55°C to +125°C
- Maximum Power consumption
  - At 3.6V with a yyyMHz clock: 150mW
- Radiation Performance
  - Tested up to a total dose of 300 Krad (Si) according to the MIL-STD883 method 1019
  - No single event latchup below a LET of 80 MeV/mg/cm2
- ESD better than 2000V
- Quality Grades
  - QML-Q or V with SMD
- Package: 349pins MCGA
- Mass: 9grams

SpaceWire - Remote Terminal Controller (RTC)

AT7913E ADVANCED INFORMATION

7833B–AERO–05/09

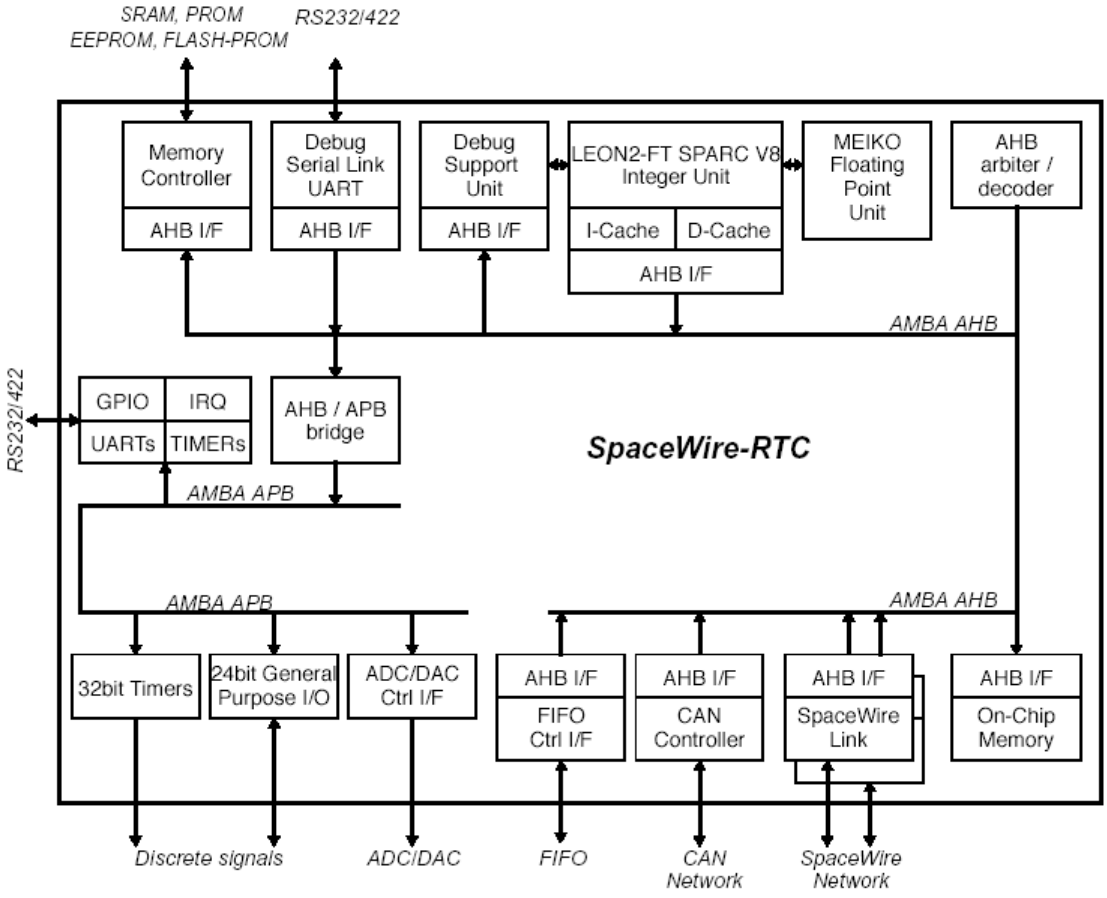
1. Description

The SpaceWire Remote Terminal Controller (RTC) device is a bridge between the SpaceWire network and the CAN bus, providing a fully integrated system. Additional features are provided to carter for autonomy of remote terminals and to relieve the central processing chain of repetitive standard acquisitions and management duties. The SpaceWire-RTC device can be used both in non-intelligent nodes and in nodes with local intelligence.

The SpaceWire-RTC device includes an embedded microprocessor, a CAN bus controller, ADC/DAC interfaces for analogue acquisition/conversion, standard interfaces and resources (UARTs, timers, general purpose input output).

The SpaceWire-RTC device can be operated stand-alone or with a number of external devices such as SRAM, PROM and FIFO memories, ADC and DAC converters. The device can be managed locally by the on-chip processor, or remotely via its SpaceWire link interfaces. SpaceWire-RTC device can operate as a single-chip system, with software being uploaded to its on-chip memory via the SpaceWire link interface, forming a compact solution for remotely controlled applications. Or it can operate in a full-size system, with software being decompressed from local PROM and executed from multiple fast and wide SRAM memory banks. The device provides scalability in terms of use of external devices and operating frequency.

Figure 1-1. AT7913E SpaceWre RTC Block Diagram



2. Pin Configuration

Table 1. Pin assignment

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ADAddr_0	K5	FifoP_0	F6	LeonPio_15	M9	MemD_14	K17	SpwSOut_P_0	A12	VDB22	J15
ADAddr_1	L5	FifoP_1	F4	LeonWDN	N7	MemD_15	K15	SpwSOut_P_1	M19	VDB23	J16
ADAddr_2	K2	FifoRdN	F2	LvdsRef0	D11	MemD_16	K13	SysClk	R1	VDB24	G15
ADAddr_3	K7	FifoWrN	E4	LvdsRef1	L16	MemD_17	J19	SysResetN	R4	VDB25	F17
ADAddr_4	L1	Gpio_0	A9	MemA_0	P9	MemD_18	H17	TapTck	E10	VDB26	F18
ADAddr_5	M3	Gpio_1	B9	MemA_1	R8	MemD_19	J18	TapTdi	G10	VDB30	D17
ADAddr_6	L2	Gpio_2	C9	MemA_2	N9	MemD_20	J17	TapTdo	B10	VSA0	V18
ADAddr_7	L3	Gpio_3	D9	MemA_3	V9	MemD_21	K11	TapTms	C10	VSA1	V4
ADCs	P2	Gpio_4	F9	MemA_4	U9	MemD_22	H15	TapTrstN	E9	VSA2	W4
ADData_0	K9	Gpio_5	J10	MemA_5	P10	MemD_23	H19	VSB31	H8	VSA3	B18
ADData_1	M5	Gpio_6	E8	MemA_6	M10	MemD_24	J12	VSB32	H3	VSA4	A4
ADData_2	M1	Gpio_7	B8	MemA_7	W10	MemD_25	H18	TimeClk	J5	VSA5	A16
ADData_3	L8	Gpio_8	E7	MemA_8	R9	MemD_26	G17	TimeTrig_1	K4	VSA6	B2
ADData_4	M4	Gpio_9	D8	MemA_9	T10	MemD_27	J13	TimeTrig_2	K3	VSA7	B16
ADData_5	N3	Gpio_10	C7	MemA_10	R11	MemD_28	H14	VDA0	V17	VSA8	C3
ADData_6	L7	Gpio_11	G9	MemA_11	V10	MemD_29	F15	VDA1	V16	VSA9	C17
ADData_7	M6	Gpio_12	F8	MemA_12	N10	MemD_30	G18	VDA2	W3	VSA10	D1
ADData_8	N1	Gpio_13	A7	MemA_13	W11	MemD_31	J11	VDA3	B17	VSA11	D19
ADData_9	P5	Gpio_14	E6	MemA_14	U12	MemOeN_0	P13	VDA4	A3	VSA12	T1
ADData_10	N2	Gpio_15	B7	MemA_15	T11	MemOeN_1	V14	VDA5	A17	VSA13	T19
ADData_11	P3	Gpio_16	C6	MemA_16	P11	MemOeN_2	U16	VDA6	B3	VSA14	U3
ADData_12	N4	Gpio_17	D7	MemA_17	L10	MemOeN_3	W15	VDA7	B4	VSA15	U17
ADData_13	L9	Gpio_18	J9	MemA_18	R12	MemWrN_0	V13	VDA8	C1	VSA16	V2
ADData_14	T2	Gpio_19	A6	MemA_19	W12	MemWrN_1	U14	VDA9	C2	VSA17	W16
ADData_15	P4	Gpio_20	F7	MemA_20	R13	MemWrN_2	T13	VDA10	C18	VSB0	D12
ADRc	N6	Gpio_21	D6	MemA_21	T12	MemWrN_3	L11	VDA11	C19	VSB1	H10
ADRdy	L4	Gpio_22	C5	MemA_22	U13	PVDDPLL	A14	VDA12	U1	VSB2	H9
ADTrig	L6	Gpio_23	B6	MemBExcN	D14	PVSSPLL	F14	VDA13	U2	VSB3	B5
ADWr	R3	IoBrdyN	D16	MemCB_0	F19	RomCsN_0	N11	VDA14	U18	VSB4	D2
CanEn_0	E2	IoCsN	C16	MemCB_1	D18	RomCsN_1	P12	VDA15	U19	VSB5	H7
CanEn_1	D4	IoOeN	B14	MemCB_2	F16	SpwClk10Mbit_0	A10	VDA16	V3	VSB6	J6
CanRx_0	D5	IoRead	D15	MemCB_3	E17	SpwClk10Mbit_1	E11	VDA17	W17	VSB7	K8
CanRx_1	G8	IoWrN	A15	MemCB_4	E19	SpwClk10Mbit_2	D10	VDB0	G12	VSB8	N5

CanTx_0	C4	LeonDsuAct	R7	MemCB_5	E16	SpwClkMult_0	D13	VDB1	F10	VSB9	T3
CanTx_1	A5	LeonDsuBre	V8	MemCB_6	H13	SpwClkMult_1	H12	VDB2	A8	VSB10	P8
FifoD_0	G4	LeonDsuEn	N8	MemCB_7	G13	SpwClkMuxSel	H11	VDB3	G7	VSB11	U8
FifoD_1	G2	LeonDsuRx	U7	MemCsN_0	T15	SpwClkPllCnfg_0	C14	VDB4	F1	VSB12	R10
FifoD_2	F3	LeonDsuTx	T8	MemCsN_1	N12	SpwClkPllCnfg_1	A13	VDB5	J8	VSB13	U11
FifoD_3	G1	LeonErrorN	M7	MemCsN_2	T16	SpwClkPllCnfg_2	E14	VDB6	H6	VSB14	V12
FifoD_4	F5	LeonPio_0	P7	MemCsN_3	N14	SpwClkSrc	B13	VDB7	K6	VSB15	R14
FifoD_5	H4	LeonPio_1	T4	MemD_0	T17	SpwDIn_N_0	C11	VDB8	M2	VSB16	U15
FifoD_6	G3	LeonPio_2	W5	MemD_1	R19	SpwDIn_N_1	L17	VDB9	V5	VSB17	R18
FifoD_7	H2	LeonPio_3	T5	MemD_2	R16	SpwDIn_P_0	B11	VDB10	W8	VSB18	P14
FifoD_8	G5	LeonPio_4	V6	MemD_3	P16	SpwDIn_P_1	L18	VDB11	W9	VSB19	N18
FifoD_9	H1	LeonPio_5	U4	MemD_4	P19	SpwDOut_N_0	E13	VDB12	U10	VSB20	M16
FifoD_10	H5	LeonPio_6	T6	MemD_5	T18	SpwDOut_N_1	N15	VDB13	V11	VSB21	K12
FifoD_11	J7	LeonPio_7	W6	MemD_6	N16	SpwDOut_P_0	B12	VDB14	M11	VSB22	K18
FifoD_12	J2	LeonPio_8	P6	MemD_7	P17	SpwDOut_P_1	M18	VDB15	W13	VSB23	J14
FifoD_13	J3	LeonPio_9	T7	MemD_8	N19	SpwSIn_N_0	C12	VDB16	T14	VSB24	H16
FifoD_14	J1	LeonPio_10	M8	MemD_9	P15	SpwSIn_N_1	M17	VDB17	N13	VSB25	G16
FifoD_15	K1	LeonPio_11	V7	MemD_10	L12	SpwSIn_P_0	A11	VDB18	P18	VSB26	G14
FifoEmpN	D3	LeonPio_12	U6	MemD_11	K19	SpwSIn_P_1	L19	VDB19	M12	VSB30	F13
FifoFullN	G6	LeonPio_13	W7	MemD_12	L15	SpwSOut_N_0	F12	VDB20	M13		
FifoHalfN	E1	LeonPio_14	R6	MemD_13	K16	SpwSOut_N_1	M14	VDB21	K14		

3. Pin Description

Table 2. Pin description

Signal Name	Type	Function
VDB	POWER	3.3V Power for the device
VDA, PVDDPLL	POWER	1.8V Power for the device
VSA, VSB, PVSSPLL	POWER	Ground for the device
SysClk	I	System Clock
SysResetN	I	System Reset
LeonErrorN	IO, open-drain, output	LEON Error - This active low output is asserted when the processor has entered error state and is halted. This happens when traps are disabled and an synchronous (un-maskable) trap occurs.
LeonWDN	IO, open-drain, output	LEON watchdog - This active low output is asserted when the watchdog times-out.
LeonDsuEn	I	DSU enable - The active high input enables the DSU unit. If de-asserted, the DSU trace buffer will continue to operate but the processor will not enter debug mode.
LeonDsuTx	O	DSU UART transmit - This active high output provides the data from the DSU communication link transmitter
LeonDsuRx	I	DSU UART receive - This active high input provides the data to the DSU communication link receiver.
LeonDsuBre	I	DSU break - A low-to-high transition on this active high input will generate break condition and put the processor in debug mode
LeonDsuAct	O	DSU active - This active high output is asserted when the processor is in debug mode and controlled by the DSU.
LeonPio[15:0]	IO	LEON Parallel Input / Output - These bi-directional signals can be used as inputs or outputs to control external devices.
Gpio[23:0]	IO	General Purpose Input / Output
TimeClk	I	External timer clock
TimeTrig[2:1]	O	External timer trigger - Asserted for 8 system clock periods
CanTx[1:0]	O	CAN transmit
CanRx[1:0]	I	CAN receive
CanEn[1:0]	O	CAN transmit enable
ADData[15:0]	IO	ADC/DAC data
ADAddr[7:0]	IO	ADC/DAC address

ADWr	O	DAC write strobe
ADCs	O	ADC chip select
ADRc	O	ADC read/convert
ADRdy	I	ADC ready
ADTrig	I	ADC trigger
MemA[22:0]	O	Memory interface address - These active high outputs carry the address during accesses on the memory bus. When no access is performed, the address of the last access is driven (also internal cycles).
MemD[31:0]	IO	Memory interface data - MemD[31:0] carries the data during transfers on the memory bus. The processor only drives the bus during write cycles. During accesses to 8-bit areas, only MemD[31:24] are used.
MemCB[7:0]	IO	Memory interface checkbitsMemCB[6:0] carries the EDAC checkbits, MemCB[7] takes the value of TB[7] in the error control register. The processor only drive MemCB[7:0] during write cycles to areas programmed to be EDAC protected
MemCsN[3:0]	O	SRAM chip select - These active low signals provide an individual output enable for each SRAM bank.
MemOeN[3:0]	O	SRAM output enable -These active low outputs provide the chip-select signals for each SRAM bank.
MemWrN[3:0]	O	SRAM byte write strobe - These active low outputs provide individual write strobes for each byte lane. MemWrN[0] controls MemD[31:24], MemWrN[1] controls MemD[23:16], etc.
RomCsN[1:0]	O	PROM chip select - These active low outputs provide the chip-select signal for the PROM area. RomCsN[0] is asserted when the lower half of the PROM area is accessed (0 - 0x10000000), while RomCsN[1] is asserted for the upper half.
IoCsN	O	I/O area chip select - This active low output is the chip-select signal for the memory mapped I/O area.
IoOeN	O	I/O area output enable - This active low output is asserted during read cycles on the memory bus.
IoRead	O	I/O area read - This active high output is asserted during read cycles on the memory bus.
IoWrN	O	I/O area write - This active low output provides a write strobe during write cycles on the memory bus.
IoBrdyN	I	I/O area ready - This active low input indicates that the access to a memory mapped I/O area can be terminated on the next rising clock edge.

MemBExcN	I	Memory exception - This active low input is sampled simultaneously with the data during accesses on the memory bus. If asserted, a memory error will be generated.
FifoD[15:0]	IO	FIFO data
FifoP[1:0]	IO	FIFO parity
FifoRdN	O	FIFO read strobe
FifoWrN	O	FIFO write strobe
FifoFullN	I	FIFO full
FifoEmpN	I	FIFO empty
FifoHalfN	I	FIFO half-full, half-empty
SpwClkSrc	I	SpaceWire transmitter clock source
SpwClkMult[1:0]	I	SpaceWire clock configuration
SpwClk10Mbit[2:0]	I	SpaceWire clock configuration
SpwClkPllCnfg[2:0]	I	SpaceWire clock configuration
SpwClkMuxSel	I	SpaceWire clock configuration - configuration External clock when 1, internal PLL when 0.
SpwDIn_P[1:0]	I, LVDS positive	SpaceWire Data input, positive
SpwDIn_N[1:0]	I, LVDS negative	SpaceWire Data input, negative
SpwSIn_P[1:0]	I, LVDS positive	SpaceWire Strobe input, positive
SpwSIn_N[1:0]	I, LVDS negative	SpaceWire Strobe input, negative
SpwDOut_P[1:0]	O, LVDS positive	SpaceWire Data output, positive
SpwDOut_N[1:0]	O, LVDS negative	SpaceWire Data output, negative
SpwSOut_P[1:0]	O, LVDS positive	SpaceWire Strobe output, positive
SpwSOut_N[1:0]	O, LVDS negative	SpaceWire Strobe output, negative
LvdsRef[0:1]	Power	LVDS reference voltage for SpaceWire channels

TapTck	I	TAP clock - Used to clock serial data into boundary scan latches and control sequence of the test state machine. TCK can be asynchronous with CLK.
TapTdi	I	TAP data input - Serial input data to the boundary scan latches. Synchronous with TCK
TapTdo	O	Tap data output - Serial output data from the boundary scan latches. Synchronous with TCK
TapTms	I	Tap Mode select - Resets the test state machine. Can be asynchronous with TCK. Shall be grounded for end application.
TapTrst	I	Tap Reset - Resets the test state machine. Can be asynchronous with TCK. Shall be grounded for end application.

4. Functions and Interfaces

The AT7913E SpaceWire Remote Terminal Controller (RTC) is a bridge between the SpaceWire network and the CAN bus. The AT7913E is based on a LEON2-FT SPARC v8 processor core together with a wide range of interfaces including :

- Debug Support Unit
- LEON2-FT Peripherals
  - Interrupt Controller
  - 32-bit Timer
  - UART Serial Links
  - 16-bit General Purpose Input Output
  - Memory Interface
- On-Chip Memory
- FIFO Interface
- ADC/DAC Interface.
- 32-bit Timers
- 24-bit General Purpose Input Output
- CAN Interface
- SpaceWire Link Interface
- JTAG Interface

4.1 LEON2-FT processor

The SpaceWire-RTC ASIC includes the LEON2-FT Integer Unit (IU) and the MEIKO Floating Point Unit (FPU). The LEON2-FT IU implements the SPARC integer instruction set as defined in the SPARC Architecture Manual Version 8.

The LEON2-FT IU has the following features:

- 5-stage instruction pipeline
- Separate instruction and data cache interface
- Support for 8 register windows
- Multiplier 16x16
- Radix-2 divider (non-restoring)

To allow for software compatibility with existing devices such as the AT697E from Atmel, the AT7913E SpaceWire-RTC includes all standard LEON2-FT peripherals and the debug support unit.

The programming model of the SpaceWire-RTC device is thus compatible with the existing devices, only requiring support for the additional functions and interfaces to be added to the existing software development tools and operating systems.

The SpaceWire-RTC includes a LEON2-FT core with 4kbyte Instruction and Data caches. It also includes a MEIKO FPU (the same one as included in the Atmel AT697device).

4.2 Debug Support Unit

The AT7913E SpaceWire RTC includes a hardware debug support to aid software debugging on target hardware. The support is provided through two modules:

- a debug support unit (DSU)
- a debug communication link

4.2.1 Debug Support Unit

The DSU can put the processor in debug mode, allowing read/write access to all processor registers and cache memories. The DSU also contains a trace buffer which stores executed instructions and/or data transfers on the AMBA AHB bus.

The debug support unit is used to control the trace buffer and the processor debug mode. The DSU is attached to the AHB bus as slave, occupying a 2 Mbyte address space. Through this address space, any AHB master can access the processor registers and the contents of the trace buffer.

The DSU control registers can be accessed at any time, while the processor registers and caches can only be accessed when the processor has entered debug mode. The trace buffer can be accessed only when tracing is disabled/completed. In debug mode, the processor pipeline is held and the processor state can be accessed by the DSU.

4.2.2 Debug communication link

The SpaceWire-RTC device includes a debug support unit communication link that consists of a UART connected to the AHB bus as a master. The debug communications link implements a simple read/write protocol and uses standard asynchronous UART communications. The simple communication protocol is supported to transmit access parameters and data.

A link command consists of a control byte, followed by a 32-bit address, followed by optional write data.

4.3 LEON2-FT Peripherals

The AT7913E SpaceWire-RTC includes all the standard LEON2-FT peripherals.

4.3.1 Interrupt Controller

The Interrupt Controller is used to priorities and propagate interrupt requests from internal or external devices to the integer unit. 15 interrupts are handled, divided on two priority levels.

A Secondary Interrupt Controller is included to support the 32 additional interrupts used by the additional on-chip peripherals of the AT7913E device.

4.3.2 32-bit Timer

The timer unit implements two 32-bit timers, one 32-bit watchdog and one 10-bit shared prescaler. The functionality of the timers has not been modified with respect to existing implementations, to allow for software compatibility.

The watchdog functionality is used for overall software timeout handling and is the basis for error management.

4.3.3 UART Serial Links

Two identical UARTs are provided for serial communications. The UARTs support data frames with 8 data bits, one optional parity bit and one stop bit. To generate the bit-rate, each UART has a programmable 12-bits clock divider. Hardware flow-control is supported through handshake signals.

4.3.4 16-bit General Purpose Input Output

The 16-bit general purpose input output port can be individually programmed as output or input. Two registers are associated with the operation of the port; the combined input/output register, and direction register. When read, the input/output register will return the current value of the port; when written, the value will be driven on the port signals. The direction register defines the direction for each individual port.

4.3.5 Memory Interface

The SpaceWire-RTC memory interface is implemented using the LEON2-FT Memory Controller that supports the following:

- 8-bit PROM with sequential EDAC,
- 8-bit SRAM with sequential EDAC
- 32-bit PROM/SRAM with parallel-EDAC
- 8, 16, 32 bit I/O without-EDAC (wait-state and/or ready handshake)
- 16 bit GPIO (byte-wise) when less than 32 bit memory used

4.4 On-Chip Memory

The SpaceWire-RTC device includes a fault tolerant on-chip SRAM with embedded Error Detection And Correction (EDAC) and AMBA AHB slave interface.

One error is corrected and two errors are detected, which is done by using a (32, 7) BCH code. Some of the features available are single error counter, diagnostic reads and writes and auto-scrubbing (automatic correction of single errors during reads).

The on-chip memory comprises a 32-bit wide memory bank of 64 kbytes of data.

4.5 FIFO Interface

This FIFO memory can be accessed as an on-chip memory or as an external interface of the chip via the Memory Interface.

The FIFO interface supports transmission and reception of blocks of data by use of circular buffers located in memory external to the core. Separate transmit and receive buffers are assumed. Reception and transmission of data can be ongoing simultaneously.

4.6 ADC/DAC Interface

The SpaceWire-RTC includes a combined analogue-to-digital converter (ADC) and digital-to-analogue converter (DAC) interface.

The ADC/DAC interface provides a combined signal interface to parallel ADC and DAC devices. The two interfaces are merged both at the pin/pad level as well as at the interface towards the AMBA bus. The interface supports simultaneously one ADC device

and one DAC device in parallel. Address and data signals unused by the ADC and the DAC can be use for general purpose input output, providing 0, 8, 16 or 24 channels.

The ADC interface supports 8 and 16 bit data widths. It provides chip select, read/convert and ready signals. The timing is programmable. It also provides an 8-bit address output. The ADC conversion can be initiated either via the AMBA interface or by internal or external triggers. An interrupt is generated when a conversion is completed.

The DAC interface supports 8 and 16 bit data widths. It provides a write strobe signal. The timing is programmable. It also provides an 8-bit address output.

4.7 32-bit Timers

The SpaceWire-RTC includes a General Purpose Timer Unit that implements one prescaler and two 32-bit decrementing timers.

4.8 24-bit General Purpose Input Output

The SpaceWire-RTC includes a 24-bit General Purpose Input Output core. The AMBA APB bus is used for control and status handling.

The core provides 24 channels. Each channel is individually programmed as input or output. Additionally, 8 of the channels are also programmable as pulse command outputs. The default reset configuration for each channel is as input. The default reset value each channel is logical zero.

The pulse command outputs have a common 20-bit counter for establishing the pulse command length. The pulse command length defines the logical one (active) part of the pulse. It is possible to select which of the channels shall generate a pulse command. The pulse command outputs are generated simultaneously in phase with each other, and with the same length (or duration). It is not possible to generate pulse commands out of phase with each other.

4.9 CAN Interface

The SpaceWire-RTC includes a CAN controller. The CAN protocol is based on the ESA HurriCANe CAN Controller VHDL core.

The controller uses the AMBA APB bus for configuration, control and status handling. The AMBA AHB bus is used for retrieving and storing CAN messages in memory external to the CAN controller. This memory can be located on-chip or external to the chip.

The CAN controller supports transmission and reception of sets of messages by use of circular buffers located in memory external to the core. Separate transmit and receive buffers are assumed. Reception and transmission of sets of messages can be ongoing simultaneously.

4.10 SpaceWire Link Interface

The SpaceWire (SPW2) Module is used for transmitting and receiving data over a SpaceWire link. It provides support for transmitting any type of protocol or data structure using SpaceWire packets.

It provides hardware support for receiving two types of SpaceWire Transfer Protocols, and can relay packets of other protocols to software. The SpaceWire Virtual Channel Transfer Protocol (VCTP) implements multiple virtual channels (only one implemented in SpaceWire-RTC) on a single SpaceWire link. The Remote Memory Access Protocol (RMAP) implements remote memory access to resources in the node via the SpaceWire link.

Data received over the link by the SpaceWire CODEC are temporarily stored in an RxFIFO. Data are then stored to memory by the SpaceWire Module via direct memory-access. Multiple Virtual Receive Channels (RxVC) can be used, each with its private memory area to which data are written. In SpaceWire-RTC one channel (RxVC(1)) is used for storing VCTP packets, and one channel (RxVC(0)) is used for storing RMAP responses, RMAP commands not supported by hardware and packets of other types of Transfer Protocols.

All RxVC share the same link. The SpaceWire Module implements hardware support for the RMAP. RMAP is used for remotely accessing resources on the local AMBA bus. The RMAP implementation can receive commands and generate responses, utilizing the aforementioned RxFIFO and the TxFIFO.

Data to be sent are read by the SpaceWire Module from memory via direct memory access. Data are then temporarily stored in a TxFIFO when forwarded to the SpaceWire CODEC for transmission over the link. Multiple Virtual Transmit Channels (TxVC) can be used, each with its private send list stored in memory from which data are read. In SpaceWire-RTC one channel (TxVC(0)) is used for automatic RMAP responses, and another channel (TxVC(1)) is used for transmissions set up by the user. All TxVC share the same link. RMAP responses have priority over transmissions set up by the user. The arbitration is performed for each packet sent.

4.11 JTAG Interface

The JTAG interface (compliant with IEEE-Std-1149.1) is used for the purpose of boundary scan testing during manufacture and test of printed circuit boards hosting the ASIC.

5. Typical Applications

The capabilities of the SpaceWire-RTC device are not limited to support the CAN bus in the instrument controller unit (ICU), but also allows it to be used in an on-board computer (OBC).

The AT7913E SpaceWire RTC is perfectly suited for application requiring cost optimizations as it can be used in both payload and avionics.

5.1 AT7913E in ICU

The SpaceWire-RTC device can be integrated in the instrument controller Unit (ICU) that acts as the payload data processor and mainly receives payload data from instruments and produces processed data to be down linked. The main data communication is performed via the SpaceWire network. The ICU is however controlled and monitored via the CAN network from the On-Board Computer (OBC).

5.2 AT7913E in OBC

The CAN controller in the SpaceWire-RTC device acts as a remote terminal that is being managed by the OBC. Alternatively, the SpaceWire-RTC device can be integrated in the On-Board Computer (OBC). Since the OBC acts as the network manager on the CAN network, the CAN controller carters capability such as node management and time distribution. The OBC also communicates or manages the SpaceWire network via SpaceWire links.

5.3 AT7913E on payload

The main application of the SpaceWire-RTC device is however in instruments or individual experiments of the payload. It provides an abundance of interfaces, each with a high degree of programmability and configurability. It is able to acquire analogue and digital data, generated by connected peripherals and to generate discrete commands towards the same peripherals.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage - 1.8V Core Voltage	VDA	-0.3 to +2.0	V
Supply Voltage - 3.3V I/O Voltage	VDB	-0.3 to +4.0	V
I/O Input Voltage		-0.3 to 4.0	V
Operating Temperature Range		-55 to +125	°C
Storage Temperature Range	Tstg	-65 to +150	°C
ESD for PLL		>1000	V
ESD for I/O		>2000	V

Stresses above those listed may cause permanent damage to the device.

6.2 DC Electrical Characteristics

Table 6-2. 3.3V operating range DC Characteristics.

Parameter	Symbol	Min.	Max.	Unit	Conditions
Operating Voltage	VCA	1.65	1.95	V	
	VCB	3.0	3.6	V	
Input HIGH Voltage	VIH	2.0		V	
Input LOW Voltage	VIL		0.8	V	
Output HIGH Voltage	VOH	2.4		V	IOL = 3, 6, 12mA / VCC = VCC(min)
Output LOW Voltage	VOL		0.4	V	IOH = 3, 6, 12mA / VCC = VCC(min)
Output Short circuit current	IOS		50 100	mA mA	VOUT = VCC VOUT = GND

6.3 AC Electrical Characteristics

The following table gives the worst case timings measured by Atmel on the 3.0V to 3.6V operating range

Table 6-3. 3.3V operating range timings

Parameter	Symbol	Min.	Max.	Unit
Propagation delay, SysClk rising to MemCsN_0 falling	Tp0		18	ns
Propagation delay, SysClk rising to CanTx_0 rising	Tp1		29	ns
Propagation delay, SysClk rising to Gpio_22 rising	Tp2		25	ns

Propagation delay, SysClk rising to FifoD_1 rising	Tp3		16	ns
Propagation delay, SpwClkSrc rising to SpwDout_P_0 falling	Tp4		14	ns
Propagation delay, SpwClkSrc rising to SpwDout_N_0 rising	Tp5		14	ns

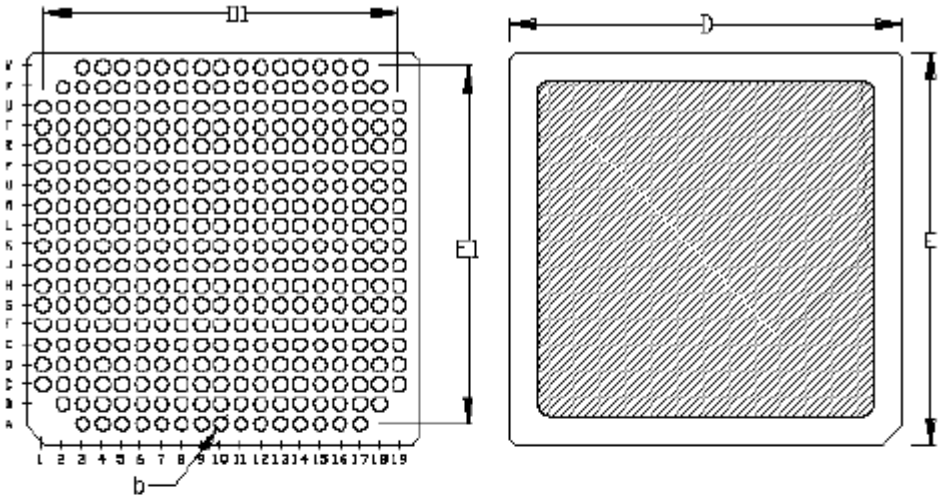
For guaranteed timings on the two operating voltage ranges, refer to the section XXX of the ‘SpaceWire-RTC (SpwRtc) Datasheet’

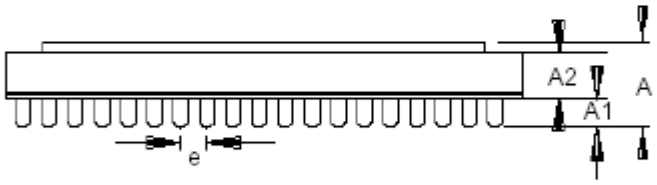
7. Package Drawings

7.1 MCGA349

Here is a presentation of the mechanical outline of the 349 pins Ceramic Quad Flat Pack (MCGA 349) package used for the AT7913E

Figure 7-1. MCGA349 package





	mm		inch	
	min	max	min	max
D/E	24,8	25,2	0,976	0,992
D1/E1	22,86		0,9	
A1	1,4	1,85	0,055	0,073
A2	2,4	3,45	0,094	0,136
A	4,3	5,9	0,169	0,232
b	0,79	0,99	0,031	0,04
e	1,27		0,05	

8. Ordering Information

Part-number	Temperature Range	Package	Quality Flow
AT7913EKB-E	25°C	MCGA349	Engineering sample
AT7913EKB-MQ	-55°C to +125°C	MCGA349	Mil Level B (*)
AT7913EKB-SV	-55°C to +125°C	MCGA349	Space Level B (*)

(*) according to Atmel Quality flow document 4288, see Atmel web site.