Features

- **Six Connections for Series-resonant LF Coil Antennas**
- **Drives up to 1A Peak Current on the First Three Channels and up to 700 mA Peak on the Second Three, Largely Independent of the Battery Voltage**
- **On-off-keyed Data Modulation with up to 6 kbit/s**
- **Sinusoidal-like Output Signal for Superior EMC Behavior**
- **20 Selectable Steps for Current Regulation for Field Strength Measurement (RSSI)**
- **Output Driver Stages are Protected Against Electrical and Thermal Overload**
- **Very Low Power-down Current Consumption**
- **SPI Interface for Easy Microcontroller Bus Connection**
- **LF Data Buffer to Minimize Microcontroller's CPU Load During a Data Transmission**
- **Small Outline Package: QFN48, 7 mm × 7 mm**

Antenna Driver for Multiple Antennas

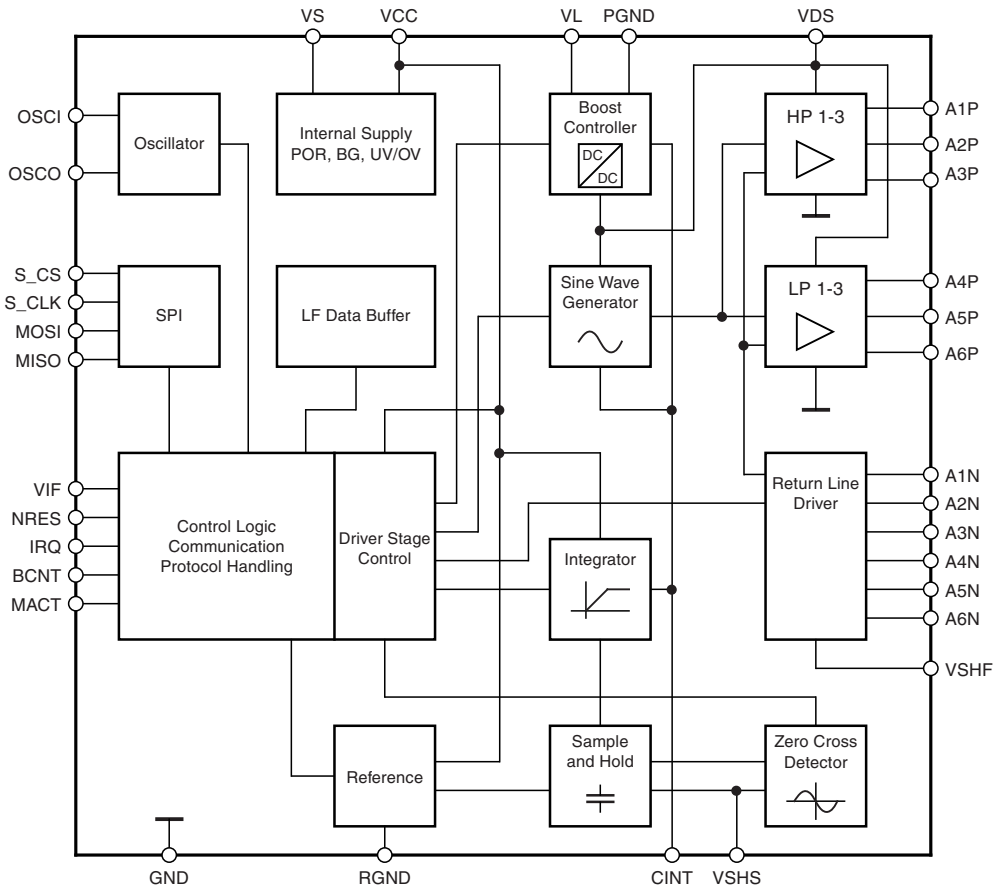
ATA5279N

Preliminary

1. Description

The ATA5279N is an LF coil driver IC intended for passive entry/-go (PEG) systems. It can drive up to six low-frequency-antennas (i.e., coils) to provide a wake-up and initialization channel to the key fob.

Figure 1-1. Block Diagram



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2. Pin Configuration

Figure 2-1. Pinning QFN48

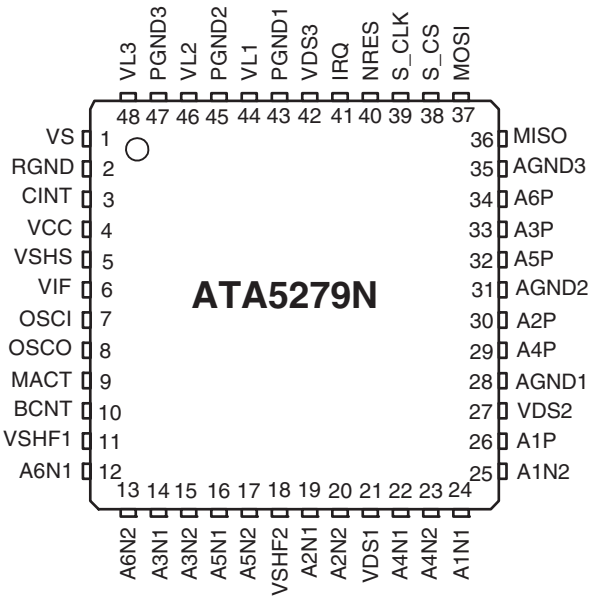


Table 2-1. Pin Description

Pin	Symbol	Function	Pin Group
Heat Slug	PGND	Backside ground connection	-
1	VS	Battery supply pin	-
2	RGND	Reference ground	-
3	CINT	Integration capacitor connection	-
4	VCC	Analog 5V stabilization capacitor connection	-
5	VSHS	Shunt resistor voltage sense input	-
6	VIF	Digital supply voltage input	-
7	OSCI	Oscillator input pin	CSP
8	OSCO	Oscillator output pin	CSP
9	MACT	Modulator active indicator output pin	DO
10	BCNT	LF-bit counter output pin	DO
11	VSHF1	Shunt resistor driving pin 1	RLO
12	A6N1	Coil 6 negative connection line pin 1	LRL
13	A6N2	Coil 6 negative connection line pin 2	LRL
14	A3N1	Coil 3 negative connection line pin 1	HRL
15	A3N2	Coil 3 negative connection line pin 2	HRL
16	A5N1	Coil 5 negative connection line pin 1	LRL
17	A5N2	Coil 5 negative connection line pin 2	LRL
18	VSHF2	Shunt resistor driving pin 2	RLO
19	A2N1	Coil 2 negative connection line pin 1	HRL
20	A2N2	Coil 2 negative connection line pin 2	HRL

Table 2-1. Pin Description (Continued)

Pin	Symbol	Function	Pin Group
21	VDS1	Driver supply pin 1	DS
22	A4N1	Coil 4 negative connection line pin 1	LRL
23	A4N2	Coil 4 negative connection line pin 2	LRL
24	A1N1	Coil 1 negative connection line pin 1	HRL
25	A1N2	Coil 1 negative connection line pin 2	HRL
26	A1P	Coil 1 positive connection line pin	HDL
27	VDS2	Driver supply pin 2	DS
28	AGND1	Driver ground pin 1	-
29	A4P	Coil 4 positive connection line pin	LDL
30	A2P	Coil 2 positive connection line pin	HDL
31	AGND2	Driver ground pin 2	-
32	A5P	Coil 5 positive connection line pin	LDL
33	A3P	Coil 3 positive connection line pin	HDL
34	A6P	Coil 6 positive connection line pin	LDL
35	AGND3	Driver ground pin 3	-
36	MISO	Master-In-Slave-Out SPI output pin	DO
37	MOSI	Master-Out-Slave-In SPI input pin	DI
38	S_CS	SPI chip select pin	DI
39	S_CLK	SPI clock input pin	DI
40	NRES	Chip reset input pin	DI
41	IRQ	Interrupt request output pin	DI
42	VDS3	Driver supply pin 3	DS
43	PGND1	Boost converter low-side switch output 1	-
44	VL1	Boost converter low-side switch input 1	BLS
45	PGND2	Boost converter low-side switch output 2	-
46	VL2	Boost converter low-side switch input 2	BLS
47	PGND3	Boost converter low-side switch output 3	-
48	VL3	Boost converter low-side switch input 3	BLS

3. Functional Description

3.1 Operation Modes

ATA5279N features five operation modes. They are:

- Power-down mode (reset state)
- Idle mode
- Operating mode
- Shutdown mode
- Diagnosis mode

Power-down mode is active after supply voltages have been applied to the chip. No internal circuitry is active in this mode and as such power consumption is minimal. If no operation of the chip is demanded, it should be kept in this state. To enter power-down mode, a negative pulse on the NRES pin for at least $t_{NRES,min}$ is required.

After wake-up from power-down mode by a logic high signal at the S_CS pin, the chip is in idle mode. That is, the oscillator is running and the control logic waits for commands coming from the serial interface. Furthermore, the selected output driver stage is ready for operation (the voltage on the corresponding output pin AxP is approximately half the battery supply voltage). The current consumption of the chip is now mainly defined by the cross current through the active driver stage (please refer also to Section 3.2 “Coil Driver Stage” on page 5).

When processing coil driving commands, the chip is in operation mode. From the interface point of view, there is no difference from the idle mode; however, current consumption is now higher as the output driver stages are operating and, depending on the selected output current, the DC-DC converter is also operating.

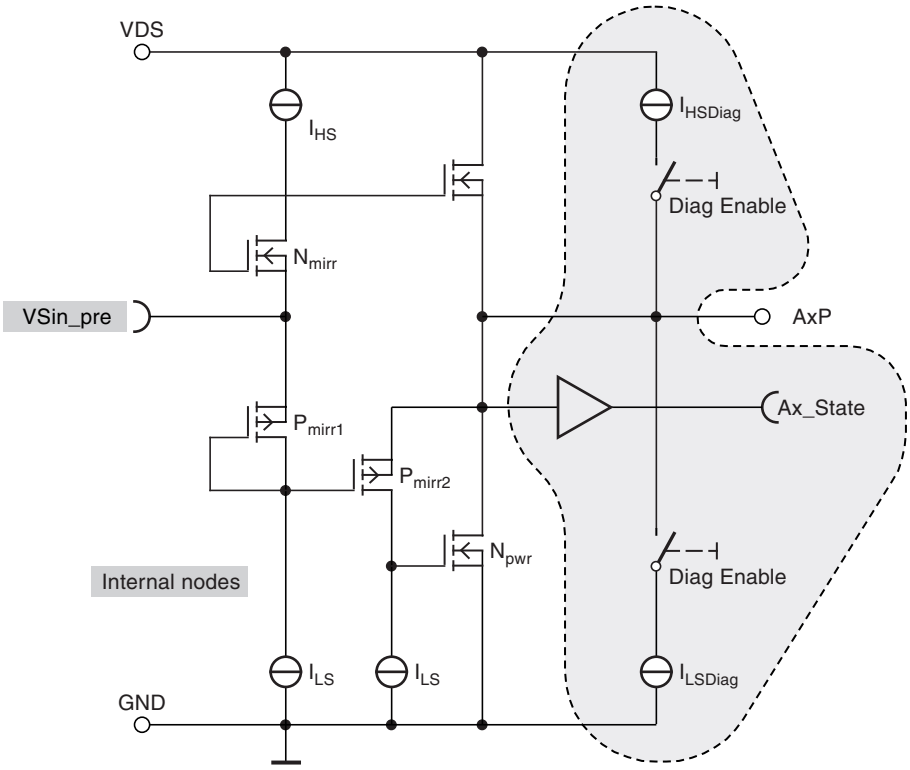
If a connection failure (short circuit on any of the coil connection lines) is detected, the ATA5279N enters the shutdown mode to protect itself from damage. In this mode, the interface operates in idle mode but with all power stages shutdown and no LF transmission command processing. This mode should be exited using the Reset Fault Status command (see below), however, it can also be exited by resetting the chip.

In diagnosis mode, the output driver stages are also disabled. In their place, high-ohmic current sources are activated that can be programmed via the serial interface in order to check the coil connection lines for failures. This mode can be exited by an appropriate SPI command or by resetting the chip.

3.2 Coil Driver Stage

The driver stage for each coil consists of two N-channel DMOS transistors. The low-side transistor is in Darlington configuration to maintain a source-follower characteristic.

Figure 3-1. Principle Driver Stage Setup



In the graphic above, the names of internal pins have a grey shaded background, and the hatched area is not part of the driver stage itself but only used in diagnostic mode (please refer to the Diagnosis Block description for further information on this topic).

The driver stages are supplied by the three VDS pins, which are tied together inside the chip.

A quiescence current regulation ensures low cross current while in idle state. The output transistors are monitored for current and temperature to protect them from damage caused by irregular load conditions or too high ambient temperatures.

The driving stage is optimized for signal quality to ensure low harmonic distortions.

Two groups of driver stages are integrated: the first group is intended for high-current coils, whereas the second group drives low-current coils. Note that there are certain coil impedance ranges for each driver group. If the connected load exceeds this range, proper current regulation and/or data modulation is not guaranteed.

While in idle mode and especially during a transmission, the driver stages of the five inactive (i.e., not selected) coils are switched to high-side outputs, i.e., the positive coil connection lines are tied to the VDS potential. The same applies to the return line inputs AxN. These measures ensure minimum parasitic currents in the disabled coils while the selected coil is operating.

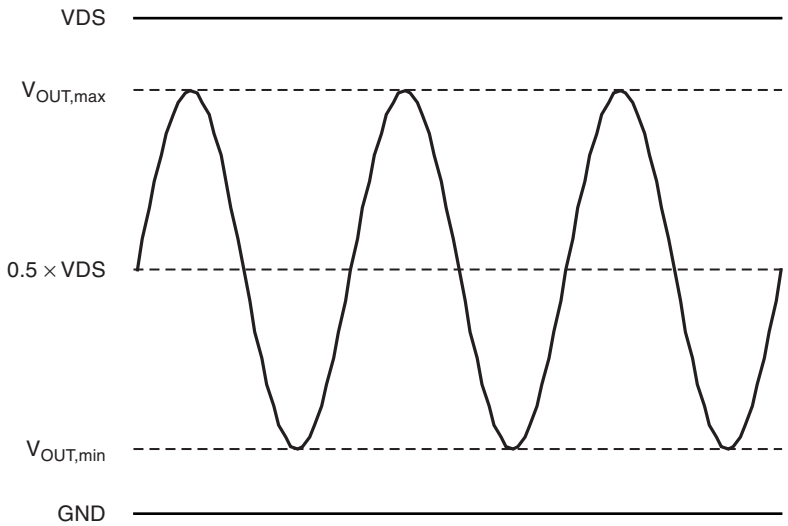
3.3 Sine Wave Generator

The sinusoidal coil-driving signal is internally generated. Its amplitude is dependant on the measured coil current, and the frequency is derived from the oscillator stage. In conjunction with the output driver stages, the generated signal is optimized for low harmonic distortions.

The peak-to-peak amplitude of the sinusoidal signal is directly defined by the voltage on the external integration capacitor connected to the CINT pin. This voltage, with an offset subtracted, is internally used to generate a low-voltage sine wave signal, which is in turn amplified and level-shifted up to the desired output level.

The output signal itself has a DC offset close to the half of the supply voltage, and the maximum possible amplitude has about 3V distance to each of the supplies. Figure 3-2 illustrates this.

Figure 3-2. Maximum Possible Coil Driving Signal for a Given Supply Voltage VDS



In application, the output coil current is the fixed valued (selectable via SPI). Hence, the required output voltage is calculated as follows:

$$V_{Out,p} = I_{Coil,p} \times (|Z_{Coil}| + R_{DSon,HRS/LRS} + R_{Shunt})$$

Here, Z_{Coil} is the complex impedance of the coil, $R_{DSon,HRS/LRS}$ is the on-resistance of the appropriate return line current selector (see also Section 7. “Functional Parameters” on page 31) and R_{Shunt} is the resistance of the externally applied current sense shunt resistor (typ. 1Ω, see also Section 4. “Application” on page 26).

3.4 Boost Converter

The coil driver stage can be supplied by a DC-DC converter in boost configuration. Together with an externally applied choke, freewheeling diode and capacitor, the battery voltage can be brought up to the required value, which is dependant on the coil's impedance and the selected current. The converter is only enabled during an active transmission. The peak current through the low-side switch I_{VL} and the output voltage V_{VDS} are measured to shut down the converter operation in case one of the values exceeds its upper limit.

Note: There is no dedicated temperature monitoring for the boost converter low-side switch. For further details, please refer to the section "Application Hints" on page 27.

The switching frequency is, like the coil driving signal, derived from the oscillator stage and 125 kHz in value when using an 8 MHz input clock. The least possible time the boost converter takes to generate the maximum possible output voltage from the minimum possible input voltage is dependant on several parameters. The values of the external components (choke inductance, charge capacitance and CINT integration capacitance) greatly effects this time.

3.5 Coil Current Sensing (Zero Cross, Sample and Hold, Integrator)

The coil current flows through an external shunt resistor, causing a current-dependant voltage, which is fed into the IC via the VSHS pin. By monitoring the zero crossing events of this signal, the phase of the coil current is known and hence the positive peak value can be sampled.

The peak coil current is then subtracted from an internal reference voltage that is dependant on the selected coil current, which results in the regulation difference.

An amplifier stage converts this difference into a current, which is then fed into an externally applied integration capacitor connected to the CINT pin. The resulting voltage on this capacitor directly influences the amplitude of the sine wave signal. It also determines the supply voltage generated by the boost converter, if the necessary coil supply voltage exceeds the actual supply voltage level. Note that during an active transmission, this voltage is internally limited to $V_{CINT,max}$.

Note that in idle mode, the voltage on the integration capacitor is kept at a value that corresponds to the battery supply voltage. This ensures that the boost converter, if needed, always performs a soft start from the battery voltage level on.

The desired current can be selected via the SPI. A total of 20 predefined steps are available, divided into the following sections:

- The lower four steps (50 mA to 200 mA) are intended for the low-current coils only
- The next ten steps (250 mA to 700 mA) are intended for both types of coils
- The upper six steps (750 mA to 1A) are intended only for the high-current coils

The IC allows the use of a current step not intended for a particular driver group; however, in this case, full functionality, especially a stabilized coil current, cannot be guaranteed. See also the Control Logic block description for an overview over the commands.

3.6 Diagnosis

The diagnosis stage monitors both the positive (AxP) and negative (AxN) connection lines of the six coils. If one of these lines is shorted to battery supply or to ground, the following measures are taken for protection and diagnostic reasons:

- All coil driver stages are shut down, i.e., put into high impedance state
- The shunt resistor is disconnected from the coil return lines
- The reason for the fault shutdown is stored in the fault register
- An interrupt request is triggered (see also control logic block)

In addition to short circuits, a disconnected coil (i.e., open load) or an excessive junction temperature can also lead to such a fault shutdown.

Note that this type of diagnosis is carried out continuously during normal operation of the IC to protect both the IC and the peripherals from damage.

It must be avoided to design the system's load profile in such a way that the protection features of the chip are triggered under normal operating conditions. Consecutive triggering of the overtemperature shutdown may lead to a reduced lifetime.

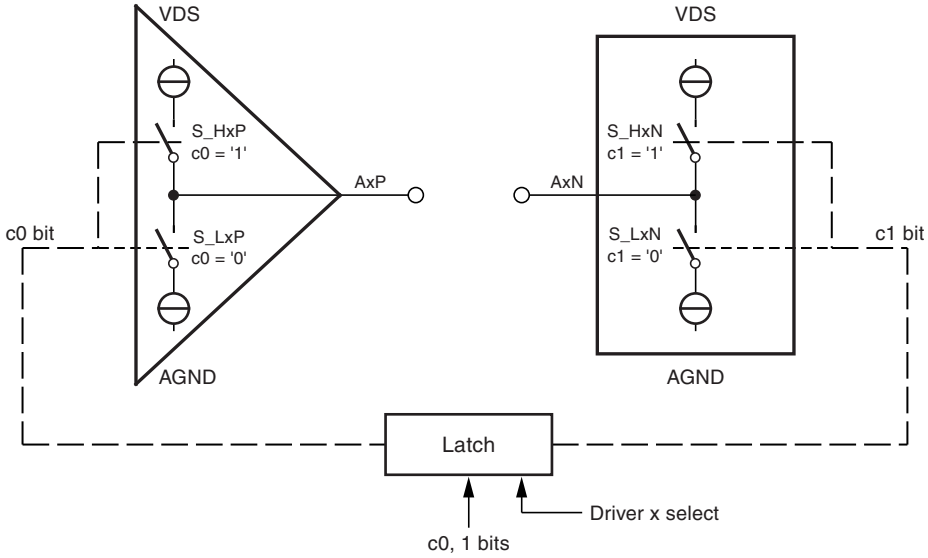
In the event of such a fault shutdown, the IC can be brought back to operation by resetting its fault register with the appropriate SPI command (please refer also to the Section 3.9.2 “General Command Description” on page 20 later in this document). As a result, transmission on non-faulty coils is still possible even if there is a failure of one coil.

Beyond this, the diagnosis of all connected coil lines is a very useful tool for maintenance reasons. The ATA5279N has implemented test structures that can be activated and read out via SPI commands, so that the microcontroller can be programmed to detect most of the possible faults, for example, shorts between different coil connection lines and multiple shorts in one pair of lines.

3.6.1 Functional Description of Diagnosis Mode

In this diagnosis mode, the coil-line drivers themselves are switched to high impedance. Hence, only the test structure at every coil connection (both at the positive outputs AxP of the drivers and at the negative outputs AxN) is present and can directly test the status of the line. Figure 3-3 illustrates this:

Figure 3-3. Base Structure of the Diagnosis Module of One Output Channel



The structure above can be found in each of the six channels of ATA5279N. As soon as the diagnosis mode is engaged, all channels are operated in this way. On the channel that is actually selected, the setting of the switches can be changed with the Set Coil Current command and the status of the two connection lines can be checked with the Get Driver Setup command.

The two switches in the P line driver are controlled with one bit. That means, either the high-side (S_HxP) or the low-side (S_LxP) switch is closed. The same is true for the N line driver (S_HxN, S_LxN). The controlling bits c_0 and c_1 are taken from the coil current selection register (see Section 3.9.2 “General Command Description” on page 20 in this document).

Note that the setting of the switches is latched. That means, if the setting on the switches of the selected driver is changed, the setting on the five other channels remains unchanged.

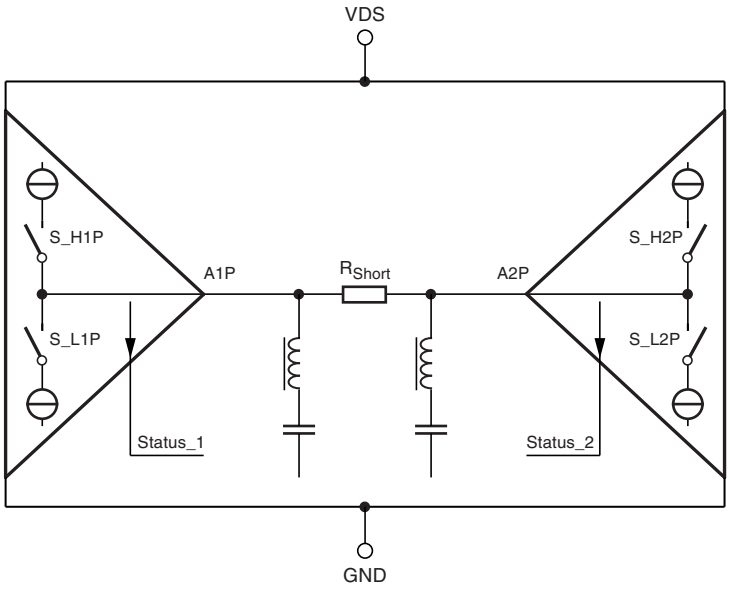
By a combination of test structures, many different faults, even between the coils, can be detected.

As described in the principle schematic of a driver stage above, a test structure consists of two switchable current sources (one to VDS and one to GND) and a comparator that converts the voltage level on the line into a digital signal. The switches for the current sources can only be controlled in diagnosis mode, with the corresponding coil being selected (see also Driver Command description). Note that one switch is always closed, either the high-side or the low-side switch of one test structure. These structures are independent, i.e., they can be set up for each line individually and at the same time.

The status of the connection lines of the selected coil can be read out with a SPI command.

In the following example, there is a short circuit between the positive coil connections of coil 1 and 2.

Figure 3-4. Example 1, Using the Diagnosis Mode



Taking the circuit situation shown above, the test run starts with both S_L1P and S_L2P switches closed (default state when entering the diagnosis mode for the first time). The read-back of the line state result in both times 0, which is not unexpected. However, the result does not change when either altering the channel 1 or the channel 2 switch setting. That can be caused both by the failure shown above and by short-circuits of both lines to ground. The final diagnosis can be identified by changing both channels to the high-side switches (S_H1P and S_H2P). In this case, the two status lines both return 1s – which eliminates the possibility of two short-circuits to ground.

Table 3-1 summarizes this test sequence.

Table 3-1. Sequence for Example 1, Using the Diagnosis Mode

Step	Command	I/O	Coding	Actions/Remarks
1	Select Driver	I	00101001 – 29h	Selects driver 1 with Diagnosis Mode enabled
2	Get Driver Setup	I O	01101000 – 68h 00000001 – 01h	Reads back active driver info: Channel 1 active, both lines return a 0
3	Select Driver	I	00101010 – 2Ah	Selects driver 2 with Diagnosis Mode enabled
4	Get Driver Setup	I O	01101000 – 68h 00000010 – 02h	Reads back active driver info: Channel 2 active, both lines return a 0
5	Set Coil Current	I	10100001 – A1h	Closes test switches S_H2P and S_L2N Note: S_L2P and S_H2N are then open
6	- no command -			Wait for the test structures to stabilize in the new setting, see below
7	Get Driver Setup	I O	01101000 – 68h 00000010 – 02h	Reads back active driver info: Channel 2 active, but both lines return a 0
8	Select Driver	I	00101001 – 29h	Selects driver 1 with Diagnosis Mode enabled
9	Set Coil Current	I	10100001 – A1h	Closes test switches S_H1P and S_L1N (Note: S_L1P and S_H1N are then open)
10	- no command -			Wait for the test structures to stabilize in the new setting, see below
11	Get Driver Setup	I O	01101000 – 68h 00001001 – 09h	Reads back active driver info: Channel 1 active and A1P returns a 1
12	Select Driver	I	00101010 – 2Ah	Selects driver 2 with Diagnosis Mode enabled
13	Set Coil Current	I	10100000 – A0h	Closes test switches S_L2P and S_L2N Note: S_H2P and S_H2N are then open
14	- no command -			Wait for the test structures to stabilize in the new setting, see below
15	Get Driver Setup	I O	01101000 – 68h 00000010 – 02h	Reads back active driver info: Channel 2 active and A2P returns a 1

Note: Steps 6, 10 and 14 are wait states, as the test structures need some time to stabilize in their new setting. This depends mainly on the externally applied capacitors on the AxP and the AxN pins.

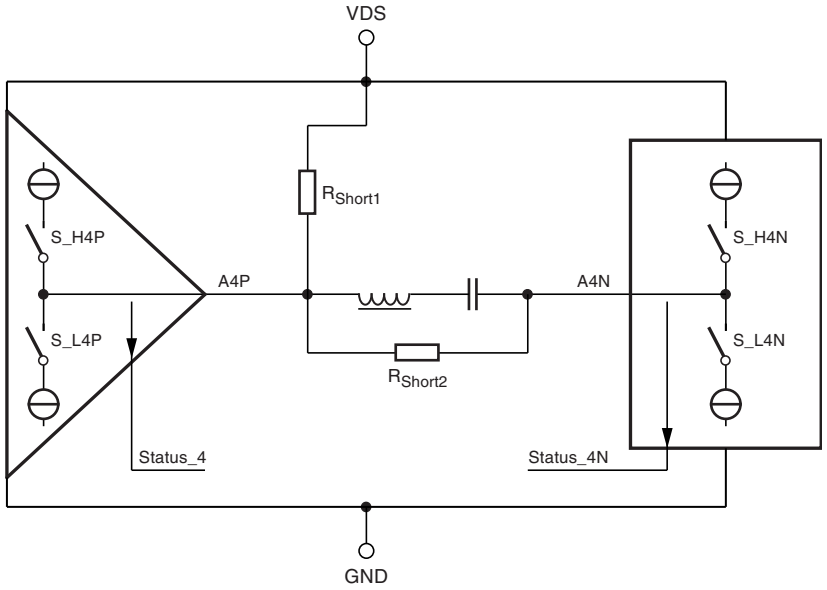
The suggested waiting time is calculated as follows:

$$t_{diag,wait} = \frac{2 \times V_S \times (C_e + C_{ant})}{300\ \mu A}$$

The sequence above is an example of how the failure illustrated in Figure 3-4 on page 10 could be detected. Depending on the grade of detection detail that is required, a matrix for the test sequence should be set up to find the most effective way of programming and testing. For more details on the commands, please refer also to Section 3.9.2 “General Command Description” on page 20.

The second example circuit has two faults in the circuitry.

Figure 3-5. Example 2, Using the Diagnosis Mode



If channel four is activated in normal operation, a fault shutdown will occur. The reason for this shutdown (i.e., the entry in the fault register) could either be an overload on the A4P line (here a short circuit to VS) or a short-circuit on the A4N line to VS. In any case, the IC protects itself and the external components from damage; however, the fact that there is more than one failure in the wiring cannot be discovered.

In diagnosis mode, by testing the A4P line with S_H4P and S_L4P, the short circuit to VS could be found first. The same result would be found when testing the return line switch 4 accordingly, so the presence of more than one fault on coil 4 is determined. The precise fault cannot be found though. The diagnosis result would be the same both for the above shown circuit and for the A4N line being directly shorted to VS (without the failure in the coil module, here R_{Shunt2}) and for the combination of the two.

Table 3-2. Sequence for Example 2, Using the Diagnosis Mode

Step	Command	I/O	Coding	Actions / Remarks
1	Select Driver	I	00101101 – 2Dh	Selects driver 4 with Diagnosis Mode enabled
2	Get Driver Setup	I O	01101000 – 68h 00011101 – 15h	Reads back active driver info: Channel 4 active, A4N returns a 1
3	Set Coil Current	I	10100010 – A2h	Closes test switches S_L4P and S_H4N Note: S_H4P and S_L4N are open then
4	- no command -			Wait for the test structures to stabilize in the new setting, see first example
5	Get Driver Setup	I O	01101000 – 68h 00011101 – 1Dh	Reads back active driver info: Channel 4 active, both lines return a 1
6	Set Coil Current	I	10100000 – A0h	Closes test switches S_L4P and S_L4N Note: S_H4P and S_H4N are open then
7	- no command -			Wait for the test structures to stabilize in the new setting, see first example
8	Get Driver Setup	I O	01101000 – 68h 00010101 – 15h	Reads back active driver info: Channel 4 active and A4N returns a 1

Again, this is only an example of how the diagnosis system can be used. Generally, a more systematic approach is suggested in order to efficiently test all connection lines used.

Note: To exit the diagnosis mode correctly, two SPI commands have to be sent: the first is the Select Driver command with the DM bit set to 0 and the second is a Reset Fault Status command. See also SPI Command Description.

3.7 SPI

The SPI is used to select the required coil and its current, to provide LF data to the IC, to select and start an LF transmission, and to read out status information. It is equipped with a chip select input to enable or disable communication. When disabled, the data output of the IC is in high impedance mode, so other devices may communicate on the same bus.

The interface is configured as a slave device, always requiring a master (e.g., a microcontroller) for operation. The maximum input clock frequency is 1/4 of the system clock present at the OSCI pin, resulting, for example, in a maximum signal speed of 2 Mbit/s when using a typical 8 MHz input clock. The SPI features four different operation modes, which only differ in the relationship between the clock signal (S_CLK) and the data I/Os.

Both the SPI itself and the corresponding I/O lines are supplied by the application-provided logic supply voltage connected to the VIF pin. This ensures that the controller (master) and the IC (slave) operate with the same voltage levels.

In total, four modes of operations are possible, each differing in clock polarity and phase.

Figure 3-6 and Figure 3-7 illustrate this.

Figure 3-6. SPI Operation in POL = 0 and PHA = 0 Mode

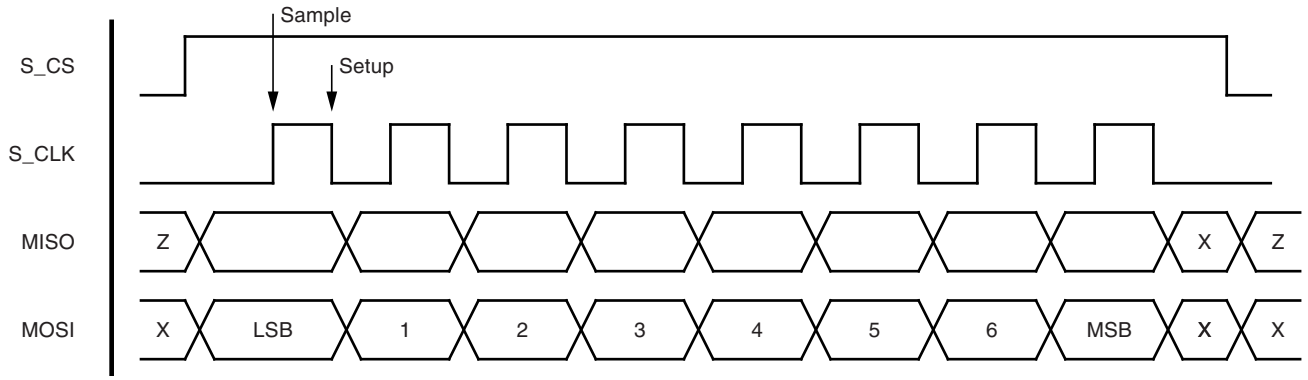


Figure 3-7. SPI Operation in POL = 1 and PHA = 0 Mode

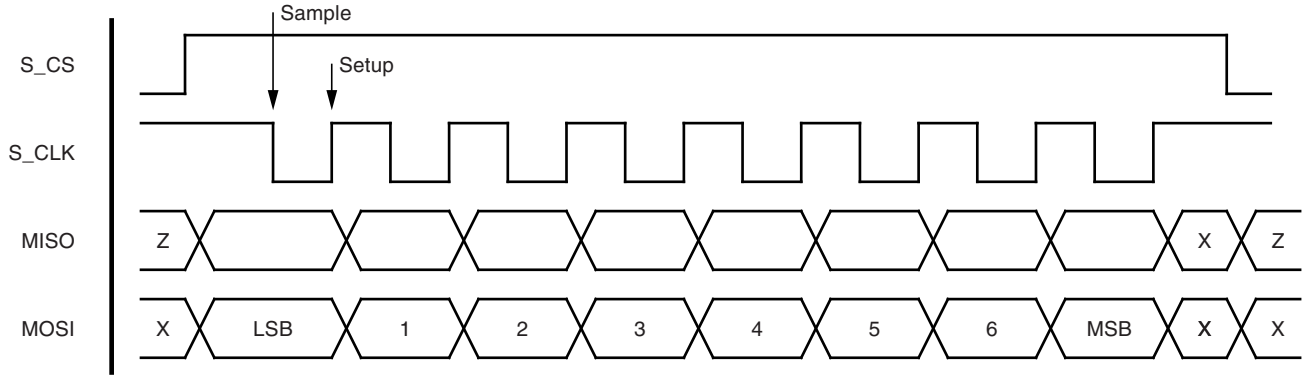


Figure 3-8. SPI Operation in POL = 0 and PHA = 1 Mode

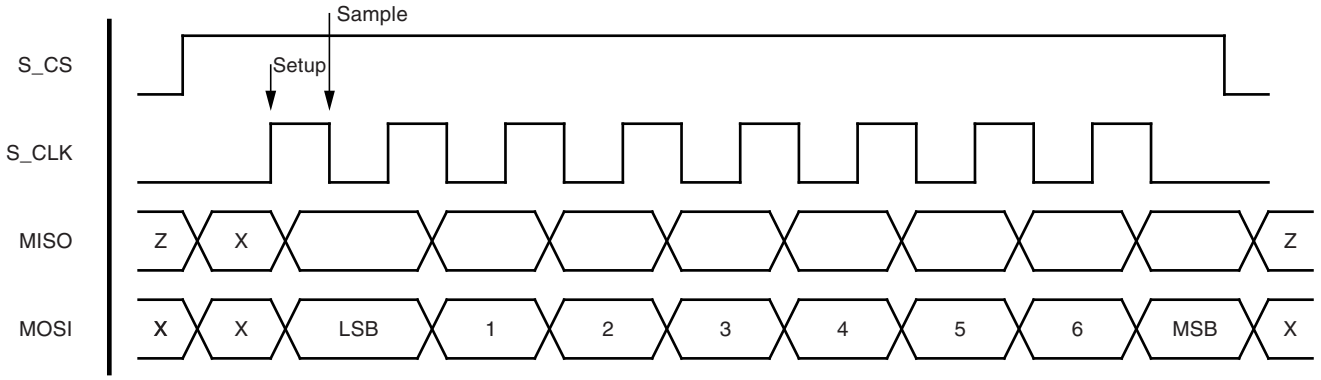
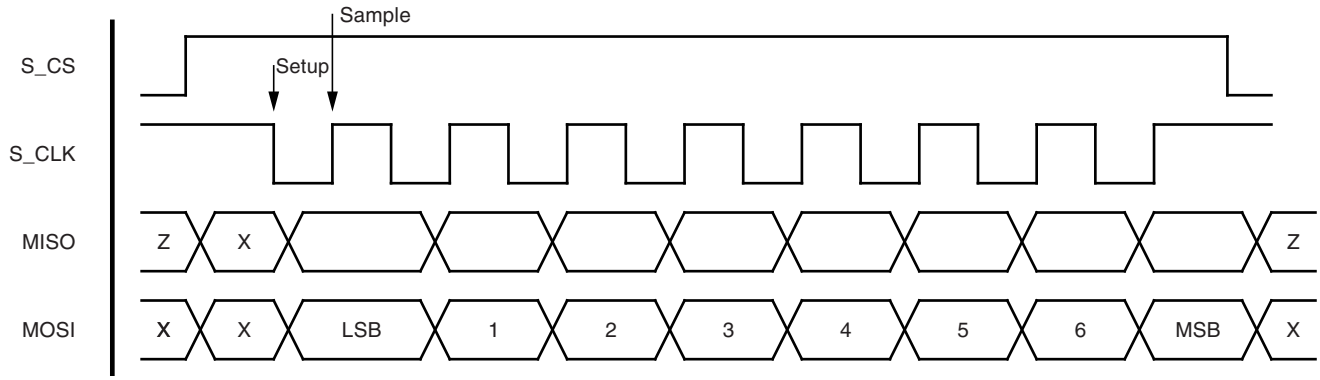


Figure 3-9. SPI Operation in POL = 1 and PHA = 1 Mode

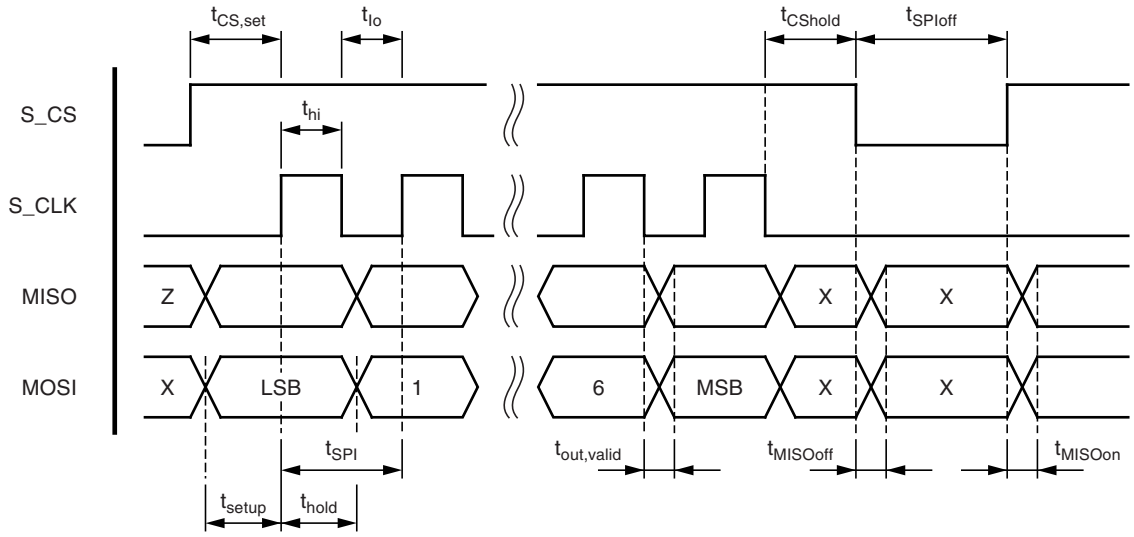


The configuration mode can be selected with the appropriate SPI command (see Section 3.9.2 “General Command Description” on page 20). Note that after power-up or a reset, the IC is always in its default configuration (POL = 1, PHA = 1), which must be used to alter the configuration. At the end of the SPI configuration-changing command, the new configuration is activated with the falling edge of the S_CS signal.

3.7.1 Timing

Figure 3-10 illustrates the timing parameters of the SPI communication.

Figure 3-10. Timing Parameters of the SPI Communication



Note: The diagram above is using POL = 0 and PHA = 0 as a setup for the SPI. The values are also valid for the other three configurations. The limits for the timing values shown above can be found in Section 7. “Functional Parameters” on page 31.

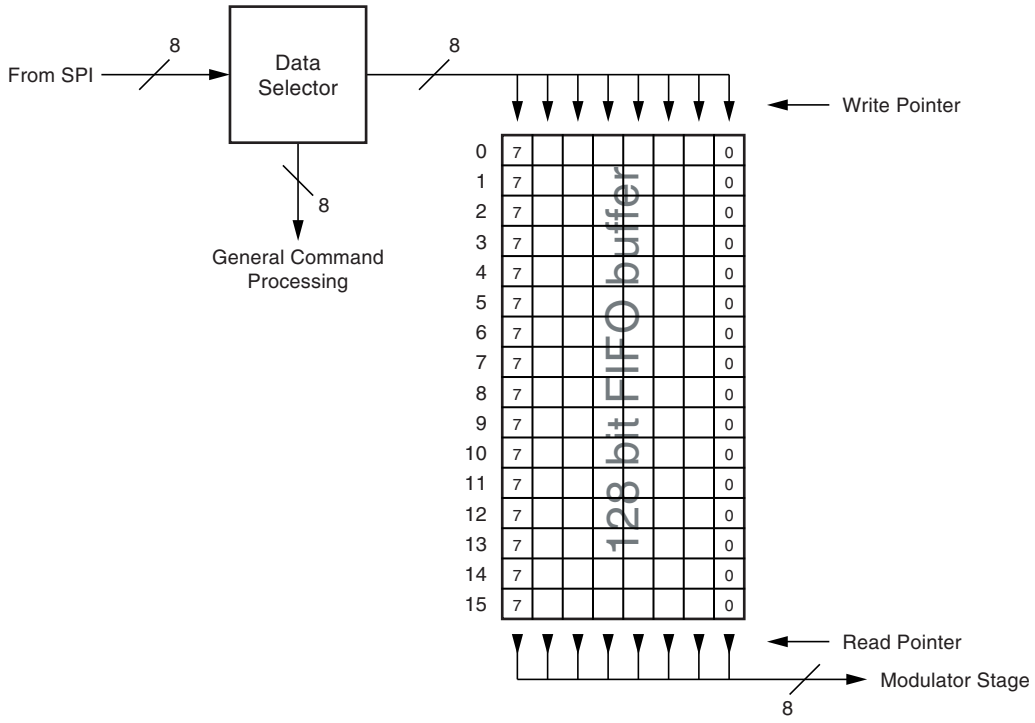
3.8 Command Buffer

This buffer is a First-In-First-Out (FIFO)-type buffer, located between the SPI and the modulator stage. The microcontroller can write coil-driving related commands and data with full SPI speed to keep the CPU and bus load low.

3.8.1 Structure

The buffer can store up to 128 bits, organized in 16 words, each eight bit in size. Hence, each data word from the SPI that contains a control command for the driver stages (i.e., select a certain driver, select a certain current, transmit LF-data bits and transmit a constant wave) is stored in a buffer word. Figure 3-11 outlines this.

Figure 3-11. Structure of 128 bit FIFO Command Buffer



The read pointer indicates the next word to be processed by the Modulator Stage, whereas the write pointer indicates the next free location for data from the SPI. These pointers are controlled by the internal logic to enable the first-in-first-out functionality.

3.8.2 Usage

After wake-up from power-down, the buffer is empty and ready to receive commands and LF data. Any LF command and data is fed into the buffer via the SPI. The buffer can be filled even during an active data modulation, i.e., when some LF data and/or commands remain in the buffer while waiting to be processed. This increases the independency of the coil driver from the microcontroller. An interrupt request (IRQ) is triggered when the fill state of the buffer drops below 25% or if too many words are sent and a FIFO overflow occurs.

Seamless data processing is an important feature of the command buffer. LF data intended for the same coil and the same current step can be distributed to several commands without the risk of having unwanted gaps in the LF telegram. This allows protocols to have any length and is usable both with the Send LF-data and the Send Carrier command. Refer also to the Section 3.9.1 “Modulator Stage” on page 17 for further details.

3.9 Control Logic

The internal control logic handles all information coming from the SPI and controls the power stages. Diagnostic information is also collected and evaluated here.

3.9.1 Modulator Stage

The modulator stage controls the coil drivers. It gets all necessary information from the command buffer. That is:

- Which coil to drive
- Which current to maintain in this coil/which diagnosis switch to close (in diagnosis mode)
- Which baud rate to use for LF data transmission
- What kind of transmission (i.e., data or carrier)
- LF data itself (respectively the on-time when a carrier is to be transmitted)

When a modulator operation is started by an SPI command, the data in the buffer is processed in the order it arrives via SPI, command by command. The time for this data processing depends on the command itself and, if LF transmissions are involved, the amount and length of the data bits.

Table 3-3 lists the timings for the driver-related commands.

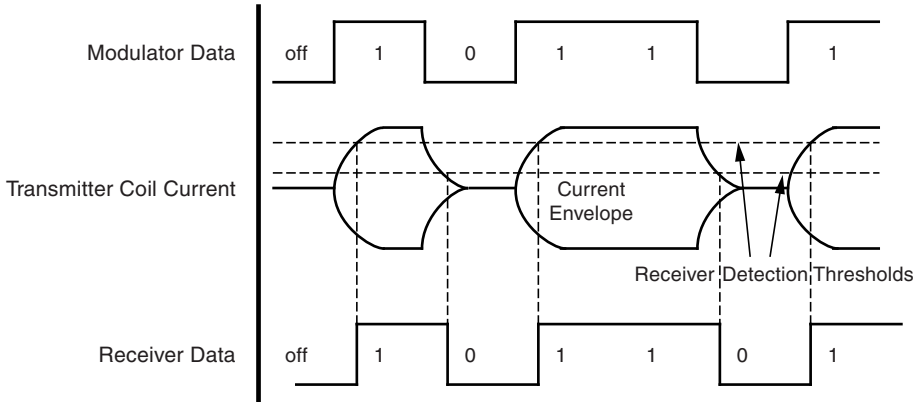
Table 3-3. Execution Durations of Driver-related Commands

Command	Dur. [LF per.]	Comment
Select Driver	64	During the first 32 periods, the actual driver is stopped in order to decay any oscillation in the coil. Then the switching itself is performed and another 32 periods waiting time is started in order to wait for the new driver to reach its operation point
Select Coil Curr.	< 1	The switching time of internal references takes less than 1 LF period. Note that there will always be an interruption in a telegram if the coil current is changed between two transmission commands
Send LF Data	N × 2 × {32 / 22}	The duration of this command depends on the selected data rate (4 kbit/s, i.e. 32 periods/LF bit, or 5.7 kbit/s, i.e., 22 periods/LF bit) and the amount of nibbles N (2 LF data bits) to be transmitted
Send LF Carrier	T × (32 / 22)	The duration of this command depends on the selected data rate (see also above) and the carrier duration T

Note: Table 3-3 lists the duration of command execution for the different commands and not the decoding or processing time. This is done simultaneous, so that two commands can be executed seamlessly.

LF data is transmitted on-off-keyed (OOK). “1” enables the field, whereas “0” disables it. Note that the field generation strongly depends on the bandwidth (the Q factor) of the coil. If it is too narrow, the receiver might not be able to decode the data correctly. Figure 3-12 shows the signal path from the modulator stage to the receiver.

Figure 3-12. Example for OOK-data Modulation with ATA5279N



Coils with high Q values need more periods to reach the desired field strength and hence appropriate detection level thresholds in the receiver. So the Q factor must be adapted in order to ensure proper data communication. For example, the thresholds here are chosen at 70% of the required output current for a 0 to 1 and at 30% for a 1 to 0 detection.

The IC supports two data rates: standard, which is 4 kbit/s (or 32 LF periods), and high speed, rated with 5.7 kbit/s (or 22 LF periods). Note that this refers to the encoded (net) data rate. The minimum length of an active field (e.g., the time for the first 1 in Figure 3-12), is 16 LF periods in standard and 11 LF periods in high speed mode (i.e., gross data rate).

Another aspect of the LF data transmission is that current regulation can only be done roughly, as the measurement must be interrupted over and over again. At a 0 to 1 transition, the current measurement will not start until the 5th period, and there will not be any measurement during a 0-transmission. The regulation precision that is achieved during carrier transmission is not valid here.

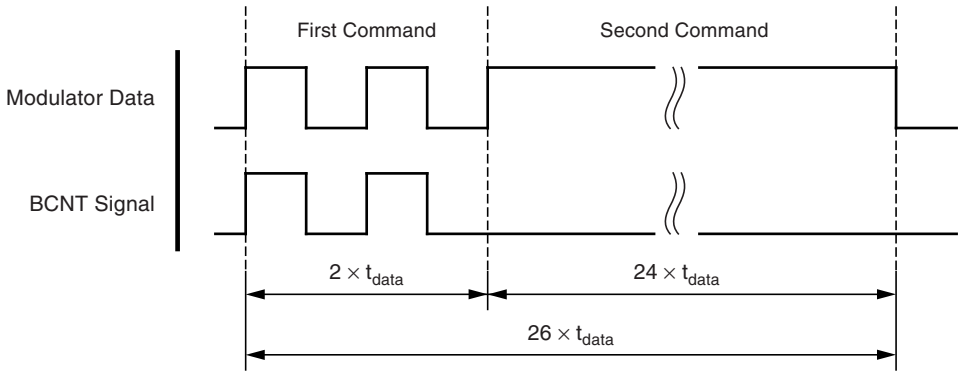
As described in Section 3.8 “Command Buffer” on page 16, data is processed seamlessly to avoid gaps in longer LF telegrams. The following example illustrates this feature.

Assume that following data words have been written into the command buffer via the SPI:

1. Send 2 LF bits (SPI data 00h 05h)
2. Send carrier with a length of 24 data bits (SPI data 98h)

In this example, the output signal of the modulator resembles the illustration below.

Figure 3-13. Example of Data Transmission of Two Consecutive Commands

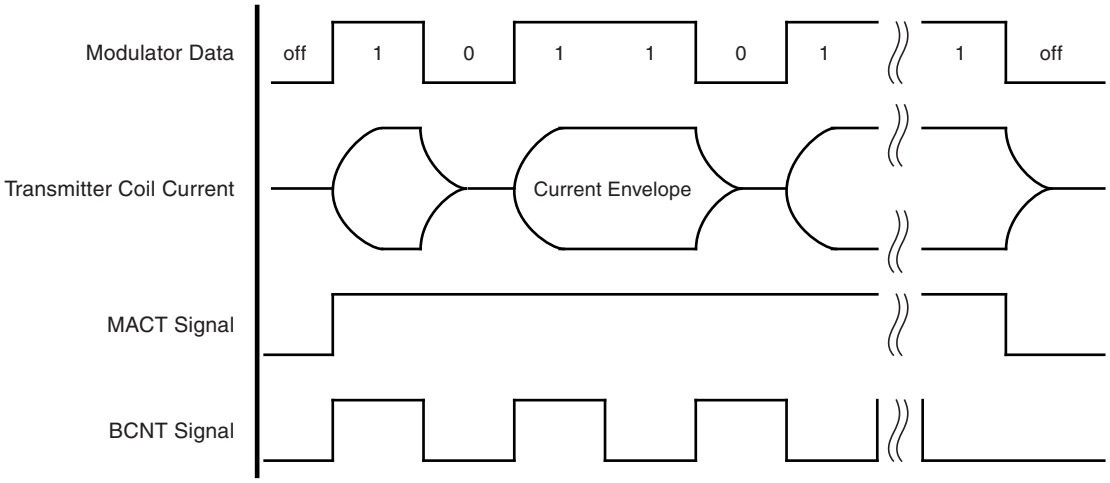


The value for t_{data} depends on the speed setting of the modulator (32 LF-periods in standard and 22 periods in high speed mode, with one period being 8 µs when operating with 125 kHz output frequency and therefore 8 MHz system clock).

The least amount of data that can be processed by the modulator stage is four LF bits or two (e.g. Manchester-encoded) data bits. The first command in the upper example is a minimum-length LF data command.

To ensure the traceability of the LF protocol, two pins are provided, which indicate an active data transmission (MACT) and the change of an LF bit (BCNT). Figure 3-12 illustrates the function of these two signals:

Figure 3-14. LF Transmission Tracing Signals



The MACT signal can be used to start a timer whereas BCNT can be used as input signal to a counter. Note that for carrier transmissions, only the MACT signal is active. There are not any pulses on the BCNT line.

3.9.2 General Command Description

The following commands are directly processed by the control logic, i.e., they are not fed into the data buffer:

Table 3-4. Bit Definitions of the General SPI Commands

Command	Input Word (MOSI Data)								Output Word (MISO Data)							
	MSB	6	5	4	3	2	1	LSB	MSB	6	5	4	3	2	1	LSB
Get status info	0 X	1 X	1 X	0 X	0 X	0 X	0 X	0 X	X R	X F	X BO	X BU	X T	X S	X Op	X X
Get driver setup	0 X	1 X	1 X	0 X	1 X	0 X	0 X	0 X	X C_4	X C_3	X C_2	X C_1	X C_0	X D_G	X D_1	X D_0
Get fault info	0 X	1 X	1 X	1 X	0 X	0 X	0 X	0 X	X D_G	X D_1	X D_0	X T	X F_{03}	X F_{02}	X F_{01}	X F_{00}
Reset fault status	0	1	0	0	0	0	0	0	X	X	X	X	X	X	X	X
Set SPI config	0	1	0	0	1	0	PO	PH	X	X	X	X	X	X	X	X
Halt operation	0	1	0	1	0	0	0	0	X	X	X	X	X	X	X	X

Refer to Section 3.7 “SPI” on page 13 for bit direction definitions.

- Get Status Info:
  This command delivers the general IC status information back to the microcontroller (via the SPI bus). One part of the return word is the interrupt request source. If such a request is active (i.e., the IRQ line is high), the source for it is coded here.
- Possible sources include the diagnosis block to indicate a driver stage fault (bit F), a general reset (either triggered externally by the NRES pin or internally by the power-on reset structure, bit R), an overtemperature of the chip (bit T), or the FIFO buffer indicating that the fill state has dropped to 25% or below (i.e., only 4 words are left, bit BU), or the fill state exceeds the upper limit of 16 bytes (bit BO). The IRQ signal is reset with this command. Additionally, the operability flag of the IC (bit Op) is returned in the word. Note that only if no fault is stored in the fault register and all operation voltages are present and valid, the operability is given (indicated by a 1 in the Op bit). Otherwise, ATA5279N will not process any driver-related command. Finally, the LF speed mode bit returned here indicates the current speed state of the modulator stage (bit S, 0 for normal speed, 1 for high speed).

  bit R: Chip reset - either triggered externally by the NRES pin or internally by the power on reset structure
  bit F: Indicator for a driver stage fault
  bit BO: The FIFO buffer fill state exceeds the upper limit of 16 bytes
  bit BU: The FIFO buffer fill state drops to 25% or below, i.e., only 4 words are left
  bit T: Chip overtemperature indicator
  bit S: LF modulator speed mode indicator
  bit Op LF driver stage operability indicator

- Get Driver Setup:
  This command returns the actual setup of the driver stage, i.e., the selected coil, encoded in the bits D_G,$D_{1..0}$, and the selected current, which can be found in the bits $C_{4..0}$ (see also “Select Driver” and “Set Coil Current” command description below for details on bit coding). This command is also used in diagnosis mode to fetch the state of the coil connection lines.
- Get Fault Info:
  This command returns the content of the driver stage fault register back to the microcontroller via the SPI bus. The register contains both the code for the detected fault and the number of the driver stage that was active when the fault occurred. Refer also to the Section 3.9.4 “Status Monitor” on page 24 for further details.
- Reset Fault Status:
  This command clears the content of the driver stage fault register and sets the operability bit in the general state register if all supply voltages are present and valid. This command is necessary to resume normal operation following the occurrence and subsequent removal of a fault. Please note that prior to this command, the active channel should be switched to a line that is not faulty. Otherwise, the internal logic might get corrupted and must then be reset with a negative pulse on the NRES line.
  Note that this command is also required to bring ATA5279N back into operation mode once the diagnosis mode was active and was then cleared by a Select Driver command.
- Set SPI Config:
  This command changes the two configuration bits PO(L) and PH(A). These bits are responsible for the serial data processing of the SPI.
  Default: PO = 1, PH = 1
- Halt Operation:
  As this command is processed immediately, it is not written to the FIFO buffer even if it is a driver-related command. The effect of this command is that the content of the FIFO buffer is cleared, hence no new LF data is available, and if any driver is active it will be stopped. Note that such stops are only carried out at the end of an LF period (i.e., when the sinusoidal output signal reaches half of the supply voltage).

3.9.3 Driver-related Command Description

Following commands are processed via the LF data buffer:

Table 3-5. Bit Definitions of the Driver-Related SPI Commands

	Input Word								Output Word							
Command	**MSB**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**	**MSB**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
Select driver	0	0	1	BR	DM	D_G	D_1	D_0	X	X	X	X	X	X	X	X
Select coil current	1	0	1	C_4	C_3	C_2	C_1	C_0	X	X	X	X	X	X	X	X
Send LF data	0 L_7 ..	0 L_6 ..	0 L_5 ..	0 L_4 ..	N_3 L_3 ..	N_2 L_2 ..	N_1 L_1 ..	N_0 L_0 ..	X 0 L_7	X 0 L_6	X 0 L_5	X 0 L_4	X N_3 L_3	X N_2 L_2	X N_1 L_1	X N_0 L_0
Send LF carrier	1	0	0	T_4	T_3	T_2	T_1	T_0	X	X	X	X	X	X	X	X

- Select Driver:
  This command selects the coil that is to be driven or tested next. The BR-bit indicates the modulation speed (0 for 4 kbit/s, i.e., 32 LF periods and 1 for 5.7 kbit/s, i.e., 22 LF periods).
- The $D_{G,1..0}$ bits indicate the channel number to be activated. D_G selects the driver group (0 for high-current driver 1..3, 1 for low-current driver 4..6) and $D_{1..0}$ the required driver in the group (01 for driver 1 / 4, 11 for driver 3 / 6). For connection line diagnosis, the diagnosis mode can be enabled by setting the DM-bit to 1.

  bit BR: LF modulator speed (0 for 4 kbit/s, i.e., 32 LF periods and 1 for 5.7 kbit/s, i.e., 22 LF periods

  bit DM: Diagnosis mode selector (0: Normal LF operation mode, 1: Coil connection diagnosis mode)

Notes:
1. If set, all coil connections are switched to this mode. Normal operation is not possible. (i.e., LF transmission). The same works for the opposite way: once a Select Driver command is received with the DM-bit at 0, all connection lines are switched back to normal operation mode.
2. For a proper operation after a diagnosis run, a Reset Fault Status command also needs to be sent.

bits $D_{G,1..0}$: Active channel indicator

bit D_G: Driver group selector (0 for high-current driver 1..3, 1 for low-current driver 4..6)

bits $D_{1..0}$: Driver selector , i.e. 01 is driver 1 (D_G = 0) / 4 (D_G = 1), 11 is driver 3 (D_G = 0) / 6 (D_G = 1).

Default: $D_{G,1..0}$ = [001], DM = 0, BR = 0 --> Channel 1, diagnosis mode off and normal LF speed selected.

- Select Coil Current
  This command defines the current to be established for the next LF transmissions.

  bits $C_{4..0}$: Contain the step number in the range of 0 to 19 (00hex to 13hex)

  bits $C_1..C_0$: Are used in diagnosis mode, to control the test switches of the activated connection line

  whereas …

  bit C_0: The low/high-side switch of the AxP line

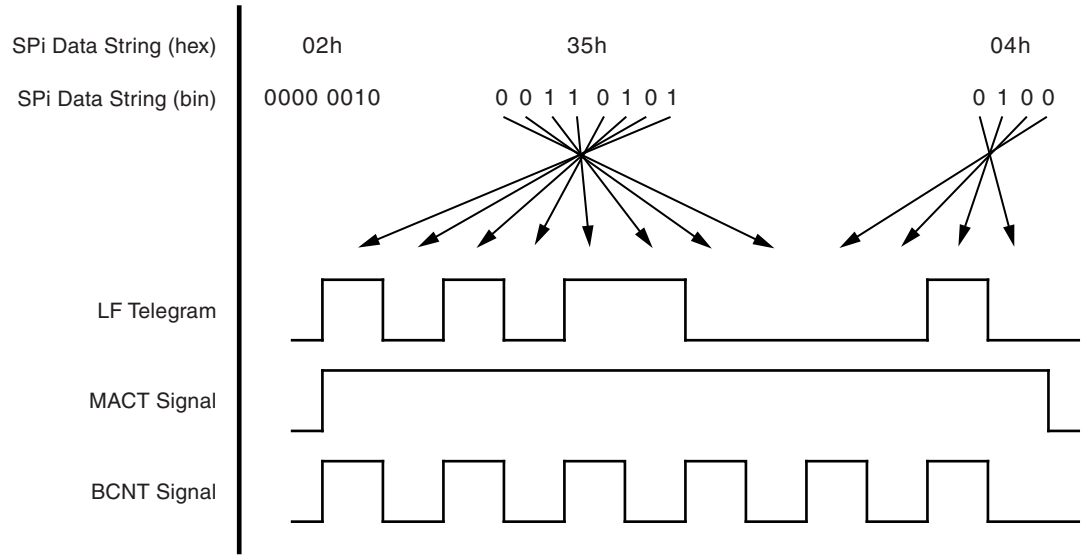
  bit C_1: The low/high-side switch of the AxN line)

  Default: $C_{4..0}$ = [00000] --> 50 mA coil current selected.
- Send LF Data:
  This command must be used to start an LF data telegram on the selected coil. The bits $N_{3..0}$ contain the amount of nibbles to be transferred into the LF data buffer of ATA5279N. This amount has to be coded as follows:
  $N_{3..0} = (n_{Nibbles} - 1)$
  Hence, a maximum of 16 nibbles or 8 words and a minimum of 1 nibble can be written into the buffer using one command.
  Note also that this command uses one more word of space in the buffer, as the header word is also stored. So for example, if the LF telegram consists of four words, the required space in the LF data buffer is five words (four words of pure data and one word for the command header).

  It is important that the amount of nibbles passed in the header word matches the number of words transferred afterwards to the IC, as no data consistency checking can be carried out here. If an odd number of nibbles is to be transferred, the data word on the SPI has to be completed with dummy data in the upper nibble, as the SPI always requires complete data

words on the bus. The FIFO buffer is also only filled with complete words.
For an example, if 7 nibbles of LF data (i.e., 14 LF data bits) are to be sent by ATA5279N via the LF channel, the Send LF Data command consists of five words, the header word (here 06h) and four LF data words, whereas the last word contains only four bits (the four least significant) of the LF data.
For an additional example, see Figure 3-15, which illustrates how LF transmission data is processed in ATA5279N.

Figure 3-15. LF Data Processing



- Send LF Carrier:
  This command should be used when a carrier shall be transmitted on the LF channel via the selected coil. The current will be regulated by ATA5279N to the value selected with the last Select Coil Current command (resp. the default value of 50 mA). See also Section 3.5 “Coil Current Sensing (Zero Cross, Sample and Hold, Integrator)” on page 7 for further details.
  The duration of this carrier can be defined by the $T_{4..0}$ bits. Note that the time unit here is one LF data bit, i.e., 32 LF periods in normal- and 22 LF periods in high-speed mode. That leads to a maximum definable carrier time per command of 31 × 0.256 ms = 7.936 ms when using an 8 MHz system clock.
  However, when the $T_{4..0}$-value is set to 0, an endless carrier transmission with the actually selected current on the actually active coil is started. This can be used for long-term measurements or for energy-coupling purposes. Be aware that long-term transmissions can produce a huge amount of heat in the driver, dependant on the selected coil current and the properties of the coil itself. It is therefore strongly recommended to use this feature only with a maximum current settings of 100 mA; otherwise, the chip temperature might reach excessive values.

3.9.4 Status Monitor

The status monitor holds all information from the diagnosis stage. In case of an existing fault, all power stages are disabled. As soon as a fault is stored, an interrupt request (IRQ) to the microcontroller is generated. This signal is persistent until the status info is polled by the microcontroller. The entry in the fault register can only be cleared by the Reset Fault command or a global reset.

There are two different status registers:

- A general IC status register (requestable by the Get Status Info command)
- A coil-driver related fault register (requestable by the Get Fault Info command)

The fault register is encoded as follows:

Table 3-6. Fault Assignment between Driver Stages and the Fault Registers

	MSB							LSB
Fault Register	D_G	D_1	D_0	T	F_{03}	F_{02}	F_{01}	F_{00}

The meaning of the bits is described below:

- D_G, $D_{1..0}$: The driver group and number that was active when the fault occurred. Only a selected driver can be affected by external faults. Therefore, it is sufficient to store the type of failure and the corresponding driver number. Refer to Section 3.9.3 “Driver-related Command Description” on page 21 for further details on the coding of these bits.
- T: A temperature shutdown has occurred. Note that there is not necessarily a link between the driver number and this fault, as all sensor signals of the chip are OR’ed together. However, in general, it can be assumed that the last active driver also caused the overtemperature condition.
- F_{03}: This bit indicates a missing return line signal during modulation. That means that the current detection unit was not able to find a sinusoidal signal on the VSHS pin although the LF coil was driven. The reason for this can either be an open load condition or a short-circuit on the AxN pin towards ground.
- F_{02}: This bit indicates an excessive positive voltage on the VSHS pin. In normal applications, this is only the case if there is a high current flowing through the shunt resistor. The typical reason for this is a short-circuit on the AxN line towards battery. Another possible reason could be a shorted LF coil.
- F_{01}: This bit indicates an excessive current through the high-side transistor that drives the AxP line. The most typical reason for this is a short-circuit towards ground.
- F_{00}: This bit indicates an excessive current through the low-side transistor that drives the AxP line. The most typical reason for this is a short-circuit towards battery.

3.10 Oscillator

This block provides the clock signals internally needed for control logic, the LF driver stage, and the boost converter. The oscillator requires an external clock source, which can either be an active signal from a microcontroller for example, or a passive oscillation device like a crystal or a ceramic resonator. As the LF carrier frequency is directly derived from this clock, the (resonance) frequency of the clock source must be chosen to match the desired LF frequency. Possible values range from 6.4 MHz to 9.6 MHz, where 8 MHz is the typical value resulting in an LF frequency of 125 kHz.

Note that during start-up (i.e., as long as no stable oscillation can be detected), the driving current for the crystal is increased to shorten the start-up delay. Furthermore, the IC is only functional if the oscillator is working properly. That means, during start-up after a power-down phase, no communication and no operation of the IC is possible until the oscillator reaches its operation point.

If an external clock source such as a microcontroller is to be used, the logic-level clock signal must be applied at the OSCI pin, and the OSCO pin must be left open. Note that the chip protection features, need a clock signal present at the OSCI pin; without this, the chip is not fully protected. Therefore, if the chip is in any mode but in power-down (reset), a clock signal is needed.

The oscillator block is, like the control logic and the SPI, supplied by the application-provided logic supply voltage connected to the pin VIF.

3.11 Internal Supply

The internal power supply stage provides all internally needed BIAS currents and reference voltages. An integrated one-time-programming (OTP) structure is used to adjust internal settings. This ensures parameter stability over the production process.

The internal supply block performs monitoring functions to reset or shut down the IC in case of supply shortages or during power-up. A power-management minimizes current consumption during power-down mode of the IC.

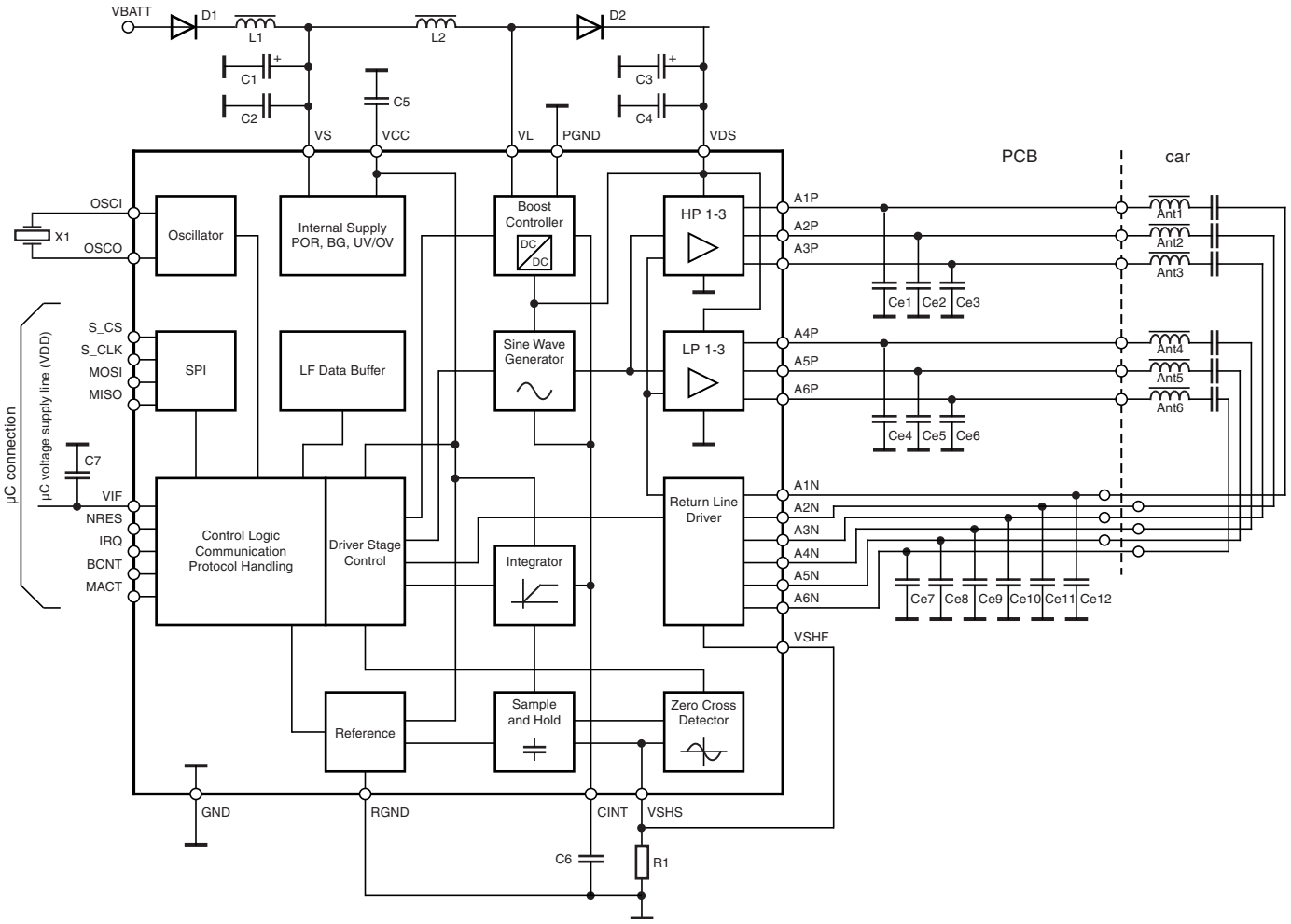
Another part of this block is the internal 5V voltage regulator. It is supplied by the VS pin, i.e., the battery supply connection. This voltage is used for all internal analog functions and driving processes. It is active as long as the IC is not in power-down mode. To increase stability and quality of this supply line, it is externally available (pin VCC) for connection to a ceramic capacitor for filtering and buffering. Note that no loads must be connected to this pin.

As with the oscillator, this supply voltage must settle in its operation point prior to any operation. The control logic checks the status of this voltage and inhibits operation until it reaches the required level. Furthermore, the driver supply voltage present on the VDSx pins is also monitored. If the level falls below $V_{VDS,min}$, the operability flag of the chip is cleared (bit Op in the Status Register) and driver-related commands cannot be processed. Once the voltage level is valid again, the Op bit is set again, and operability is restored.

4. Application

Find below a typical application schematic for ATA5279N.

Figure 4-1. Application Schematic for ATA5279N



Note: A negative current on pin MISO that causes the voltage to drop below –0.6V with respect to ground might lead to a chip reset, comparable to a logic low on the NRES pin.

Table 4-1. Bill of Materials (BOM) for Typical Application Circuit

Part	Value	Description
R1	1	Shunt resistor, ±1% tol.
C1	220 µF/50V	Supply line input filter and stabilizing cap
C2	100 nF cer.	Supply line input filter cap
C3	4.7 µF/50V tant.	Boost converter storage cap, low ESR
C4	100 nF cer.	Boost converter filter cap (+ESD clamp)
C5	100 nF cer.	Internal 5V supply line stabilizing cap
C6	33 nF cer.	Integration cap for current regulation loop
C7	100 nF cer.	Filter cap for µC supply line
Ce1..12	1 nF cer.	Add. ESD buffer, necessity tbc
D1	50V/3A	Rectifying diode
D2	50V/3A/50 ns	High-speed freewheeling diode
L1	150 µH	Supply line input filter choke, I_{sat} > 3A
L2	82 µH	Boost converter charging choke, I_{sat} > 3A
X1	8 MHz	Crystal or resonator

4.1 Application Hints

An important application aspect is the thermal budget. Under certain conditions, high power dissipations can occur during operation of the chip. The ATA5279N's power dissipation mainly depends on the supply voltage and the selected antenna output current. Under worst case conditions (e.g., low supply voltage and maximum antenna power) the power dissipation increases exponentially and may rise to values exceeding 10W. It must be avoided under all circumstances to exceed the specified maximum average junction temperature. Therefore, the thermal aspects of the entire application, along with the electrical design, are essential.

The thermal resistance between the IC and the ambient has to be designed according to the specific application requirements. It is mandatory to solder the exposed die pad to the PCB. As many vias as possible must be provided between the top and the bottom layer (soldering side to the PCB's backside). This copper plane is able to store and dissipate the heat. It must be electrically connected to ground, and an appropriate heat transfer away from the chip must be ensured. In addition, multi-layer-PCBs (more than two layers) are recommended.

The ATA5279N's power dissipation depends on the supply voltage, the selected antenna current, the antenna's impedance and further parameters such as the external components used for the DC-DC converter. Background information, design hints and an example are given in the application note "Thermal Considerations for ATA5279".

It is strongly recommended to measure the power dissipation in the target application during the design phase to verify the system's thermal budget. One option is to calculate the difference between input and output power.

See the following description for details:

$$P_{diss,tot} = P_{in} - P_{out}$$

$$P_{in} = U_{VS} \times I_{VBATT}$$

Mean value measured during an LF carrier transmission with the desired output current.

$$P_{out} = \left(\frac{I_{Ant,p}}{\sqrt{2}}\right)^2 \times |Z_{Ant}| + P_{diss,ext}$$

$P_{diss,ext}$ is the sum of power dissipated by the external components.

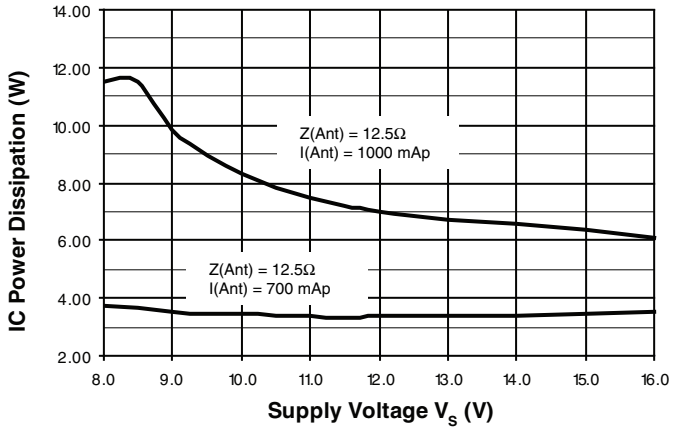
$$P_{out} = \left(\frac{I_{Ant,p}}{\sqrt{2}}\right) \times \frac{U_{Ant,pp}}{2 \times \sqrt{2}} + P_{diss,ext}$$

Alternative formula for calculating the output power.

Note: The output power can either be calculated by using the impedance of the antenna or by measuring the peak-to-peak amplitude of the sinusoidal voltage applied to the antenna. As the impedance may change under load conditions, it is recommended to use the formula with the peak-to-peak antenna voltage.

The input power determination should be done by transmitting a single LF carrier burst with a length of for example 8 ms. The required electrical data needs to be recorded with a digital sampling oscilloscope (DSO) and a current probe. Note that the start-up phase of the LF field must not be used for reading out the data.

Figure 4-2. Power Dissipation on Chip Measured at Application Board ATAB5279



Note: If the VDS output voltage regulation fails due to too high input currents or too high output voltage, the power dissipation increases up to 40%

The power dissipation of the external components depends on their parameters and the supply current. Regarding choke L_2, it is the DC resistance, regarding the freewheeling diode D_2, it is the forward biasing voltage. In addition, the equivalent series resistance (ESR) of the charging capacitor C_3 is important. The devices' names refer to the application schematic (see Figure 4-1 on page 26).

Note: To define the operation limits, the static thermal resistance of the PCB must be known (see the measurement hints in the application note). The ATAB5279 application board features a total thermal resistance of 42 K/W.

Under worst case conditions, e.g., low supply voltage and high antenna impedance, the maximum antenna current might not be reached.

A "static" operation of ATA5279N is not allowed for typical transmit currents of several hundreds of mAs. Typical applications are operated with a temporary LF field, resulting in an on/off operation mode of the chip. A suitable on/off duty cycle n_{duty} reduces the average power dissipation and keeps the thermal budget of the system. Therefore, following equation needs to be fulfilled:

$$T_{amb} + R_{thJA} \times P_{diss,tot} \times n_{duty} < T_{j,max}$$

with

T_{amb}	the application's maximum ambient temperature
$P_{diss,tot}$	the total power dissipation of the chip
n_{duty}	Operation duty cycle, On-time during period, t_1/t_{per}

Note: It must be avoided to design the system's load profile in such a way that the protection features of the chip are triggered under normal operating conditions. If the output voltage reaches the upper shutdown limit, the power dissipation of the DC-DC converter increases significantly. Consecutive triggering of the overtemperature shutdown may lead to a reduced lifetime.

In addition to the average junction temperature $T_{j,max}$, the maximum peak temperature during a transmission must not be exceeded. The equation to be met is as follows:

$$T_{peak} \geq P_{diss} \times \left[R_{thjc} + R_{thca} \times \left(1 - e^{\frac{t_1}{\tau_{PCB}}} \right) \right] + n_{duty} \times P_{diss} \times (R_{thjc} + R_{thca}) + T_{amb}$$

with:

T_{peak}	maximum peak temperature = 200°C
R_{thca}	Thermal resistance case-to-ambient (PCB)
t_1	Transmission on-time, 10 ms ≤t_1 ≤1 sec
tau_{PCB}	Thermal time constant of PCB (Rthca x Cthca)
n_{duty}	Operation duty cycle

5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Voltage range on pin VS	V_{VS}	–0.3	40	V
Voltage range on pins VDSx, VLx	$V_{VDS,max}$	–0.3	46	V
Voltage range on pins AxP	$V_{AxP,max}$	–0.3	V_{VDS} + 0.3	V
Voltage range on pins VSHFx, VSHS	$V_{VSHF,max}$	–3	V_{VCC} + 0.3	V
Voltage range on pins AxNx	$V_{AxNx,max}$	V_{VSHF} – 0.3	46	V
Voltage range on pins VCC, VIF	$V_{DIGSUP,max}$	–0.3	+5.5	V
Voltage on pins RGND, PGNDx	$V_{GND,max}$	–0.3	+0.3	V
Voltage range on pins NRES, S_CS, S_CLK, MOSI, OSCI, MACT, BCNT, IRQ, MISO, OSCO	$V_{IO,max}$	–0.3	V_{VIF} + 0.3	V
Voltage range on pin CINT	$V_{CINT,max}$	–0.3	V_{VCC} + 0.3	V
ESD Voltage Ratings - HBM (MIL-STD-883F, M. 3015.7)	V_{ESD}	2		kV
Maximum average junction temperature	$T_{j.max}$		150	°C

Note: All voltages refer to the AGND pins.

6. Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance junction to case	R_{thJC}	10	K/W
Thermal resistance junction to ambient[1]	R_{thJA}	35	K/W

Note: 1. Value that can be achieved when providing sufficient thermal vias and heat dissipation area

7. Functional Parameters

All parameters valid for 7.0V ≤ VS ≤ 16.5V and –40°C ≤ T_a ≤ 105°C unless otherwise noted.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Power Supply**								
1.1	VS-pin power-down mode supply current	V_{VS} ≤ 14V	1	I_{VSpd}		5.5	10	µA	A
1.2	VS-pin idle mode supply current	V_{VS} = 16.5V	1	$I_{VS,idle}$		3.5	5	mA	A
1.3	Internal VCC voltage - idle - load	7V ≤VS ≤28V I_{VCC} = 0 I_{VCC} = 5 mA	4	$V_{VCC,0}$ $V_{VCC,1}$	4.8	5.05	5.3	V	A
1.4	VS voltage clamp	VS = 28V VS = 40V	1	$I_{VS,C28}$ $I_{VS,C40}$	50 1.5	180 3	400 4.5	µA mA	A
1.5	VCC power-on reset threshold		4	V_{PORVCC}	4.1		4.8	V	A
1.6	VDS operation threshold	VS = 16.5V	DS	$V_{VDS,min}$	5.1	5.15	6	V	A
1.7	Battery supply range for normal operation	Idle mode	1	V_{VS}	7		16.5	V	D
1.8	VDS power-down mode supply current	V_{VDS} = 28V	DS	$I_{VDS,0}$	0	0.12	1.4	µA	A
1.9	VDS fault-shutdown mode supply current	V_{VDS} = 16.5V	DS	$I_{VDS,FS}$	0.85		2.45	mA	A
1.10	Battery supply range for Jump start operation	Idle mode	1	V_{VS}	7		26.5	V	D
2	**Boost Converter**								
2.1	Overvoltage shut-down level		DS	V_{VDSmax}	40	42	44	V	A
2.2	Switch overcurrent shutdown level		BLS	I_{VLmax}	2.9	3.2	4	A	A
2.3	Switch on-state resistance	I_{VL} = 500 mA	BLS	$R_{DSon,VL}$			0.5	Ω	A
2.4	Max duty cycle (t_{on} / T)		BLS	D_{Boost}			0.875	-	A
2.5	Switch leakage current	V_{VL} = 38V	BLS	$I_{VL,leak}$			500	nA	A
2.6	Switch fall time	I_{VL} = 200 mA	BLS	$t_{VL,f}$	50		200	ns	A
2.7	Switch rise time	I_{VL} = 200 mA	BLS	$t_{VL,r}$	50		200	ns	A
3	**Oscillator**								
3.1	External clock source frequency range		CSP	f_{OSC}	6.4	8	9.6	MHz	D
3.2	Driver output sink resistance during startup	I_{OSCO} = 100 µA	CSP	$R_{OSC,L1}$	0.9		2.2	kΩ	A
3.3	Driver output sink resistance during operation	I_{OSCO} = 100 µA	CSP	$R_{OSC,L1}$	1.8		4.4	kΩ	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
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2. Operation of coils with higher impedance than the given value is possible but functional limitations might occur (inability to reach to configured coil current). Coils with lower impedance should not be used as they might be detected as faulty.

7. Functional Parameters (Continued)

All parameters valid for 7.0V ≤ VS ≤ 16.5V and –40°C ≤ T_a ≤ 105°C unless otherwise noted.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.4	Driver output source resistance during startup	I_{OSCO} = –100 µA	CSP	$R_{OSC,L1}$	0.9		2.2	kΩ	A
3.5	Driver output source resistance during operation	I_{OSCO} = –100 µA	CSP	$R_{OSC,L1}$	1.8		4.4	kΩ	A
3.6	Feedback resistance	$V_{OSCI, OSCO}$ = 5V	CSP	$R_{FB,OSC}$	220		360	kΩ	A
3.7	Clock input low-to-high detection threshold		CSP	$V_{LH,OSC}$	0.45 × VIF		0.55 × VIF		A
3.8	Power-down input pull-down resistance	V_{OSCI} = 5V V_{VIF} = 5V	7	$R_{OSCI,0}$	3		6	kΩ	A
4	**High-current Driver Stage (A1P, A2P, A3P)**								
4.1	Sourcing current limit (RMS)	Idle mode, DC ramping	HDL	$I_{HP,HSCL}$	–1.7		–0.88	A	B
4.2	Sinking current limit (RMS)	Idle mode, DC ramping	HDL	$I_{HP,LSCL}$	1.1		2	A	B
4.3	Signal difference carrier to harmonics 2, 3, 4, 5	$V_{AxP,pp}$ = 30V $I_{coil,p}$ = 200 mA f_{OSCI} = 8 MHZ	HDL	D_{Sig}			–34	dB	A
4.4	Load imped. range (amount of complex impedance)[2]	$I_{coil,pp}$ = 2 A_{pp}	HDL HRL	$Z_{Coil,HP}$	2		12	Ω	D
4.5	Min. output voltage	I_{AxP} = 200 mA $T_j \cong$ 30°C	HDL	$V_{OHP,min}$	2.5		4.3	V	A
4.6	Max. output voltage	I_{AxP} = –200 mA $T_j \cong$ 30°C	HDL	$V_{OHP,max}$	VDS – 4.5		VDS – 2.5	V	A
4.7	Idle mode cross current	V_{VDS} = 16.5V	DS	$I_{AxPH,CC}$	35	50	68	mA	A
4.8	Idle mode output voltage	V_{VDS} = 20V I_{AxP} = 0 I_{AxP} = ±200 mA $T_j \cong$ 30°C	HDL	$V_{AxPH,dile}$	9		11	V	A
4.9	Inactive pull-up current	V_{VDS} = 20V I_{AxP} = –100 µA	HDL	$R_{AxPH,PU}$	11.5		27	kΩ	B
4.10	Diagnosis mode pull-up current	V_{VDS} = 16.5V V_{AxP} = 0V		$I_{PU,Diag}$	–150		–100	µA	A
4.11	Diagnosis mode pull-down current	V_{VDS} = 16.5V V_{AxP} = 16.5V		$I_{PD,Diag}$	170		260	µA	A
5	**Low Current Driver Stage (A4P, A5P, A6P)**								
5.1	Sourcing current limit (RMS)	Idle mode, DC ramping	LDL	$I_{LP,HSCL}$	–1.2		–0.55	A	B
5.2	Sinking current limit (RMS)	Idle mode, DC ramping	LDL	$I_{LP,LSCL}$	0.9		1.7	A	B

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7. Functional Parameters (Continued)

All parameters valid for 7.0V ≤ VS ≤ 16.5V and –40°C ≤ T_a ≤ 105°C unless otherwise noted.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5.3	Signal difference carrier to harmonics 2, 3, 4, 5	$V_{AxP,pp}$ = 30V $I_{coil,p}$ = 200 mA f_{OSCI} = 8 MHZ	LDL	D_{Sig}			–34	dB	A
5.4	Load imped. range (amount of complex impedance)(2)		LDL LRL	$Z_{Coil,LP}$	10		25	Ω	D
5.5	Min. output voltage	I_{AxP} = 200 mA $T_j \cong$ 30°C	LDL	$V_{OLP,min}$	2.5		4.3	V	A
5.6	Max. output voltage	I_{AxP} = –200 mA $T_j \cong$ 30°C	LDL	$V_{OLP,max}$	VDS – 4.5		VDS – 2.5	V	A
5.7	Idle mode cross current	V_{VDS} = 16.5V	DS	$I_{AxPL,CC}$	28	40	53	mA	A
5.8	Idle mode output voltage	V_{VDS} = 20V I_{AxP} = 0 I_{AxP} = ±200 mA $T_j \cong$ 30°C	HDL	$V_{AxPL,dile}$	9		11	V	A
5.9	Inactive pull-up current	V_{VDS} = 20 V I_{AxP} = –100 µA	HDL	$R_{AxPL,PU}$	11.5		27	kΩ	B
5.10	Diagnosis mode pull-up current	V_{VDS} = 16.5V V_{AxP} = 0V	HDL LDL	$I_{PU,Diag}$	–150		–100	µA	A
5.11	Diagnosis mode pull-down current	V_{VDS} = 16.5V V_{AxP} = 16.5V	HDL LDL	$I_{PD,Diag}$	170		260	µA	A
6	**Coil Return Line and Diagnosis Stage (A1N … A6N)**								
6.1	Return line switch on-state resistance	I_{HPS} = 0.3A I_{LPS} = 0.22A	HRL LRL	$R_{DS,onHPS}$ $R_{DS,onLPS}$			1.05 1.2	Ω Ω	A
6.2	Return line switch overcurrent shutdown threshold	R_{Shunt} = 1Ω Ch. 1-3 selected Ch. 4-6 selected	RLO	$I_{Shunt,max}$	1.25 0.875		1.75 1.225	A A	A
6.3	Diagnosis mode pull-up current	V_{VDS} = 16.5V $V_{AxP/N}$ = 0V	HRL LRL	$I_{PU,Diag}$	–150		–100	µA	A
6.4	Diagnosis mode pull-down current	V_{VDS} = 16.5V $V_{AxP/N}$ = 16.5V	HRL LRL	$I_{PD,Diag}$	170		260	µA	A
6.5	Overtemperature shutdown threshold			T_{OTsdwn}	145		170	°C	B
6.6	Open load detection delay		HRL LRL	t_{OLdet}	115		215	µs	A
7	**Zero Crossing Detector**								
7.1	Pos. slope detection threshold		5	V_{ZC}	–10		+10	mV	A
7.2	Switching propagation delay	Voltage jump from V_{VSHS} – 20 mV to V_{VSHS} + 20 mV	5	t_{ZCdel}	150		290	ns	A

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7. Functional Parameters (Continued)

All parameters valid for 7.0V ≤ VS ≤ 16.5V and –40°C ≤ T_a ≤ 105°C unless otherwise noted.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8	**Sample and Hold Stage**								
8.1	Sampled differential voltage	Sampling state Current step 20 selected V_{VSHS} = 200 mV_{pp} V_{VSHS} = 1 V_{pp}	5	 $V_{smpl,1}$ $V_{smpl,2}$	 830 440		 970 560	 mV mV	A
9	**Integrator Stage**								
9.1	Input offset voltage		5	$V_{ofs,Integ}$	–2.5		+2.5	mV	B
9.2	Positive output linearity	V_{VSHS} = 1.1 V_{pp} Current step 20 selected	3	$I_{INT,POS}$	–20		–8	µA	A
9.3	Negative output linearity	V_{VSHS} = 0.9 V_{pp} Current step 20 selected	3	$I_{INT,NEG}$	8		20	µA	A
9.6	Upper output voltage limit	I_{CINT} = 30 µA V_{SHS} = 100 mV_p Current step 20 selected	3	$V_{CINT,max}$	3.15		3.45	V	A
10	**References**								
10.1	Current step 1 level		-	$V_{REF,S1}$	49.5		54.5	mV	A
10.2	Current step 2 level		-	$V_{REF,S2}$	97		105	mV	A
10.3	Current step 3 level		-	$V_{REF,S3}$	145		157	mV	A
10.4	Current step 4 level		-	$V_{REF,S4}$	192		208	mV	A
10.5	Current step 5 level		-	$V_{REF,S5}$	245		255	mV	A
10.6	Current step 6 level		-	$V_{REF,S6}$	294		306	mV	A
10.7	Current step 7 level		-	$V_{REF,S7}$	343		357	mV	A
10.8	Current step 8 level		-	$V_{REF,S8}$	392		408	mV	A
10.9	Current step 9 level		-	$V_{REF,S9}$	441		459	mV	A
10.10	Current step 10 level		-	$V_{REF,S10}$	490		510	mV	A
10.11	Current step 11 level		-	$V_{REF,S11}$	539		561	mV	A
10.12	Current step 12 level		-	$V_{REF,S12}$	588		612	mV	A
10.13	Current step 13 level		-	$V_{REF,S13}$	637		663	mV	A
10.14	Current step 14 level		-	$V_{REF,S14}$	686		714	mV	A
10.15	Current step 15 level		-	$V_{REF,S15}$	735		765	mV	A
10.16	Current step 16 level		-	$V_{REF,S16}$	784		816	mV	A
10.17	Current step 17 level		-	$V_{REF,S17}$	833		867	mV	A
10.18	Current step 18 level		-	$V_{REF,S18}$	882		918	mV	A
10.19	Current step 19 level		-	$V_{REF,S19}$	931		969	mV	A
10.20	Current step 20 level		-	$V_{REF,S20}$	980		1020	mV	A

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7. Functional Parameters (Continued)

All parameters valid for 7.0V ≤ VS ≤ 16.5V and –40°C ≤ T_a ≤ 105°C unless otherwise noted.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11	**Digital Interface (SPI, Control Logic)**								
11.1	Supply current in operation mode	V_{VIF} ≤ 5.5V	6	I_{supVIF}	0.6	1.9	3	mA	A
11.2	Supply current in power-down mode	V_{VIF} = 5.0V	6			2	30	µA	A
11.3	SPI clock period		39	T_{SPI}	4 × 1/f_{OSCI}			s	D
11.4	SPI clock low-phase timing		39	$t_{Lo,min}$	2 × 1/f_{OSCI}			s	D
11.5	SPI clock high-phase timing		39	$t_{hi,min}$	2 × 1/f_{OSCI}			s	D
11.6	SPI output enabling time			$t_{MISOon,max}$			100	ns	D
11.7	SPI output disabling time			$t_{MISOoff,max}$			100	ns	D
11.8	Minimum SPI disable time			$t_{SPIoff,min}$	4 × 1/f_{OSCI}			s	D
11.9	Minimum chip select setup time			$t_{CSset,min}$	2 × 1/f_{OSCI}			s	D
11.10	Minimum chip select hold time			$t_{CShold,min}$	2 × 1/f_{OSCI}			s	D
11.11	Minimum data input setup time			$t_{setup,min}$	100			ns	D
11.12	Minimum data input hold time			$t_{hold,min}$	100			ns	D
11.13	Output source capability	V_{VIF} = 5V I_{Source} = –1 mA	DO	$V_{dig,H}$	4.75			V	A
11.14	Output sink capability	V_{VIF} = 5 V I_{sink} = 1 mA	DO	$V_{dig,L}$			0.25	V	A
11.15	Input current	V_{in} = 0 V V_{VIF} = 5.5V V_{in} = 5.5V V_{VIF} = 5.5V	37 38 39 40 37 38 39 40	$I_{in,L}$ $I_{in,H}$	–0.2 –0.2 –0.2 –60 0 12 0 0		0 0 0 –20 0.2 40 0.2 0.2	µA	A
11.16	Input high level threshold	V_{VIF} = 3.1V	DI	V_{LH}	0.48		0.64	V_{VIF}	A
11.17	Input low level threshold	V_{VIF} = 3.1V	DI	V_{HL}	0.32		0.48	V_{VIF}	A
11.18	External reset input timing			$t_{NRES,min}$	100			ns	D
11.19	Tristate output leakage current	V_{MISO} = 2.5V		$I_{L,max}$			500	nA	A

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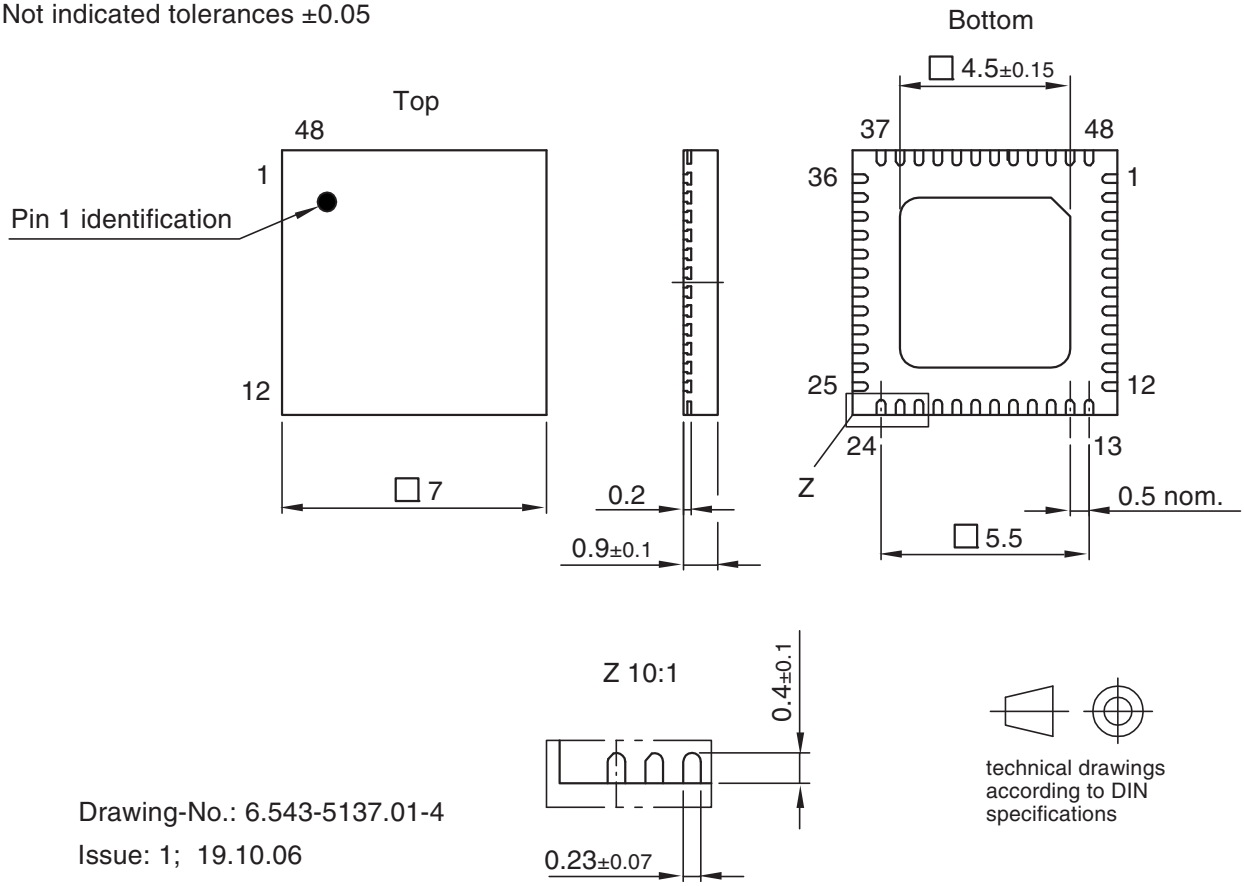
8. Ordering Information

Extended Type Number	Package	Remarks
ATA5279N-PLQW	VQFN48, 7 mm × 7 mm	Taped and reeled, MOQ 4000

9. Package Information

Package: VQFN_7 x 7_48L
Exposed pad 4.5 x 4.5
Dimensions in mm

Not indicated tolerances ±0.05



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Issue: 1; 19.10.06

10. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9125F-RKE-09/09	• Features changed • Table 2-1 (page 2) changed • Page 23: last paragraph changed • Text under heading 3.4 “Boost Converter” changed • Text under heading 3.6 “Diagnosis” changed • New section “4.1 Application Hints” added • Table Abs. Max. Ratings changed • Table Th. Resistance added • Table El. Charactristics changed
9125E-RKE-04/09	• Table “Functional Parameters” item 1.10 added and item 1.3 changed
9125D-RKE-02/09	• Section 3.9.2 “General Command Description” on pages 20 to 21 changed • Section 3.9.3 “Driver-related Command Description” on pages 21 to 22 changed
9125C-RKE-01/09	• ATA5279 renamed in ATA5279N
9125B-RKE-12/08	• Table 3-1 “Sequence for Example 1, Using the Diagnosis Mode” on page 11 changed • Table 3-2 “Sequence for Example 2, Using the Diagnosis Mode” on page 13 changed • Section 4 “Application” on page 26 changed • Section 6 “Functional Parameters” on pages 28 to 32 changed

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