

Features

- High-performance, Low-power AVR 8/16-bit XMEGA Microcontroller
- Non-volatile Program and Data Memories
 - 256 KB of In-System Self-Programmable Flash
 - 8 KB Boot Code Section with Independent Lock Bits
 - 4 KB EEPROM
 - 16 KB Internal SRAM
- Peripheral Features
 - Four-channel DMA Controller with support for external requests
 - Eight-channel Event System
 - Seven 16-bit Timer/Counters
 - Four Timer/Counters with 4 Output Compare or Input Capture channels
 - Three Timer/Counters with 2 Output Compare or Input Capture channels
 - High-Resolution Extension on all Timer/Counters
 - Advanced Waveform Extension on one Timer/Counter
 - Six USARTs
 - IrDA modulation/demodulation for one USART
 - Two Two-Wire Interfaces with dual address match (I²C and SMBus compatible)
 - Two SPI (Serial Peripheral Interface) peripherals
 - AES and DES Crypto Engine
 - 32-bit Real Time Counter with separate Oscillator and Battery Backup System
 - Two Eight-channel, 12-bit, 2 Msps Analog to Digital Converters
 - One Two-channel, 12-bit, 1 Msps Digital to Analog Converters
 - Four Analog Comparators with Window compare function
 - External Interrupts on all General Purpose I/O pins
 - Programmable Watchdog Timer with Separate On-chip Ultra Low Power Oscillator
- Special Microcontroller Features
 - Power-on Reset and Programmable Brown-out Detection
 - Internal and External Clock Options with PLL
 - Programmable Multi-level Interrupt Controller
 - Sleep Modes: Idle, Power-down, Standby, Power-save, Extended Standby
 - Advanced Programming, Test and Debugging Interfaces
 - JTAG (IEEE 1149.1 Compliant) Interface for test, debug and programming
 - PDI (Program and Debug Interface) for programming and debugging
- I/O and Packages
 - 49 Programmable I/O Lines
 - 64-lead TQFP
 - 64-pad QFN/MLF
- Operating Voltage
 - 1.6 – 3.6V
- Speed performance
 - 0 – 12 MHz @ 1.6 – 3.6V
 - 0 – 32 MHz @ 2.7 – 3.6V

Typical Applications

- | | | |
|----------------------|-------------------|----------------------------------|
| • Industrial control | • Climate control | • Hand-held battery applications |
| • Factory automation | • ZigBee | • Power tools |
| • Building control | • Motor control | • HVAC |
| • Board control | • Networking | • Metering |
| • White Goods | • Optical | • Medical Applications |



8/16-bit **AVR**[®] XMEGA A3B Microcontroller

ATxmega256A3B

Preliminary



1. Ordering Information

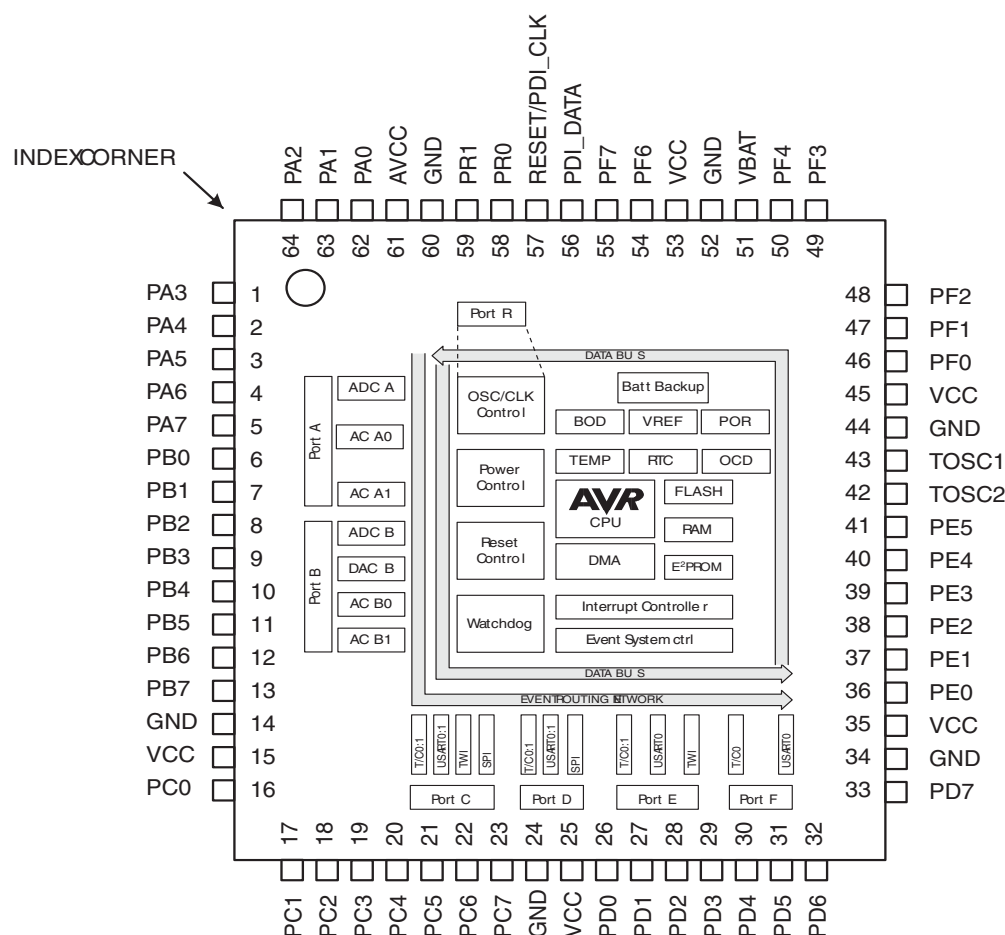
Ordering Code	Flash	E ²	SRAM	Speed (MHz)	Power Supply	Package ⁽¹⁾⁽²⁾⁽³⁾	Temp
ATxmega256A3B-AU	256 KB + 8 KB	4 KB	16 KB	32	1.6 - 3.6V	64A	-40°C - 85°C
ATxmega256A3B-MU	256 KB + 8 KB	4 KB	16 KB	32	1.6 - 3.6V	64M2	

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For packaging information, see ["Packaging information" on page 60.](#)

Package Type	
64A	64-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)
64M2	64-pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 7.65 mm Exposed Pad, Micro Lead Frame Package (MLF)

2. Pinout/Block Diagram

Figure 2-1. Block diagram and pinout.



Note: for full details on pinout and pin functions refer to ["Pinout and Pin Functions" on page 50.](#)

3. Overview

The XMEGA™ A3V is a family of low power, high performance and peripheral rich CMOS 8/16-bit microcontrollers based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the XMEGA A3B achieves throughputs approaching 1 Million Instructions Per Second (MIPS) per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The XMEGA A3B devices provides the following features: In-System Programmable Flash with Read-While-Write capabilities, Internal EEPROM and SRAM, four-channel DMA Controller, eight-channel Event System, Programmable Multi-level Interrupt Controller, 49 general purpose I/O lines, 32-bit Real Time Counter (RTC) with Battery Backup System, seven flexible 16-bit Timer/Counters with compare modes and PWM, six USARTs, two Two Wire Serial Interfaces (TWIs), two Serial Peripheral Interfaces (SPIs), AES and DES crypto engine, two 8-channel, 12-bit ADCs with optional differential input with programmable gain, one 2-channel 12-bit DAC, four analog comparators with window mode, programmable Watchdog Timer with separate Internal Oscillator, accurate internal oscillators with PLL and prescaler and programmable Brown-Out Detection.

The Program and Debug Interface (PDI), a fast 2-pin interface for programming and debugging, is available. The devices also have an IEEE std. 1149.1 compliant JTAG test interface, and this can also be used for On-chip Debug and programming.

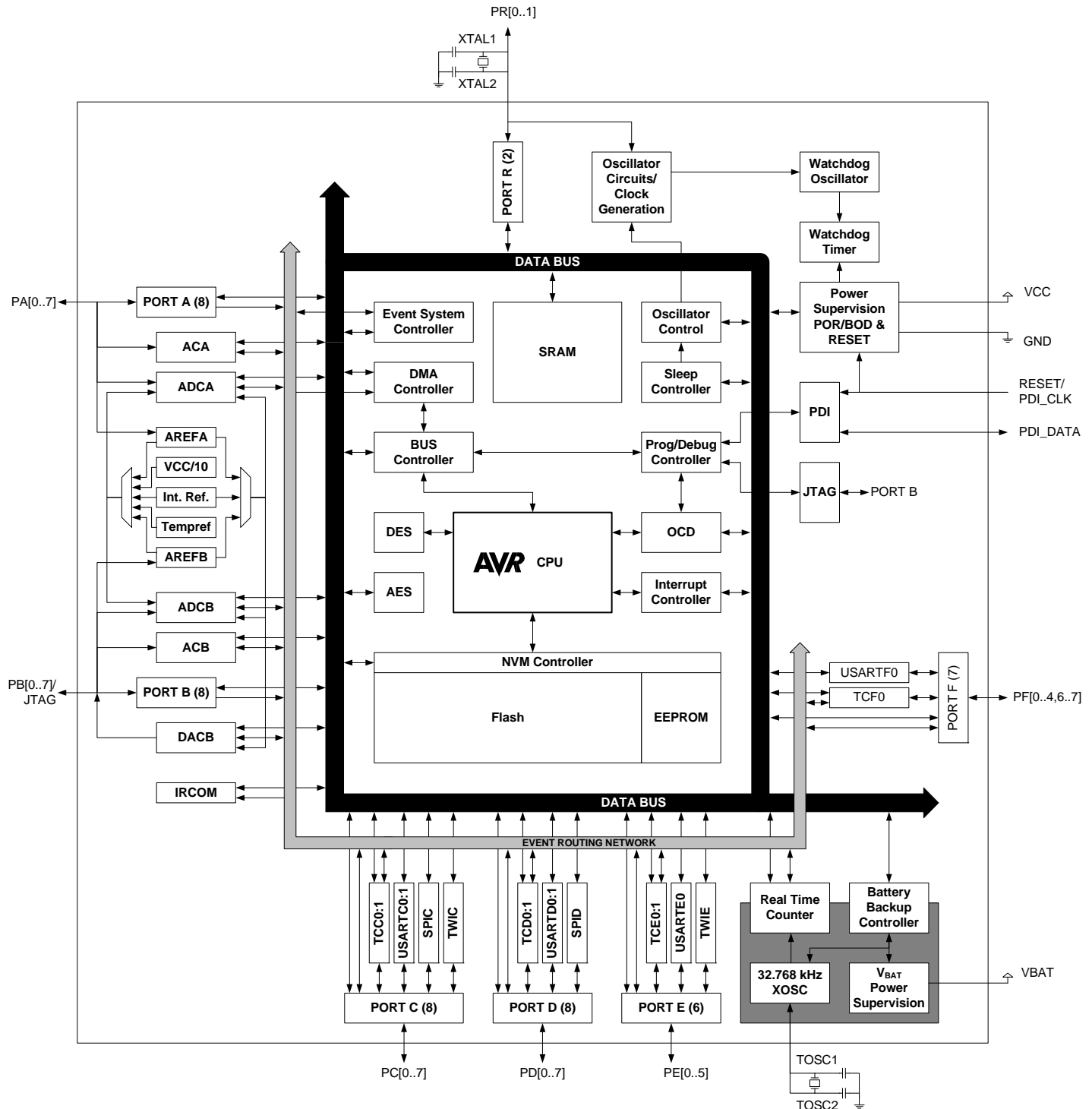
The XMEGA A3B devices have five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, DMA Controller, Event System, Interrupt Controller and all peripherals to continue functioning. The Power-down mode saves the SRAM and register contents but stops the oscillators, disabling all other functions until the next TWI or pin-change interrupt, or Reset. In Power-save mode, the asynchronous Real Time Counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In Standby mode, the Crystal/Resonator Oscillator is kept running while the rest of the device is sleeping. This allows very fast start-up from external crystal combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in Active mode and Idle sleep mode.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The program Flash memory can be reprogrammed in-system through the PDI or JTAG. A Bootloader running in the device can use any interface to download the application program to the Flash memory. The Bootloader software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8/16-bit RISC CPU with In-System Self-Programmable Flash, the Atmel XMEGA A3B is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

The XMEGA A3B devices are supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

3.1 Block Diagram

Figure 3-1. XMEGA A3B Block Diagram



4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

4.1 Recommended reading

- XMEGA A Manual
- XMEGA A Application Notes

This device data sheet only contains part specific information and a short description of each peripheral and module. The XMEGA A Manual describes the modules and peripherals in depth. The XMEGA A application notes contain example code and show applied use of the modules and peripherals.

The XMEGA A Manual and Application Notes are available from <http://www.atmel.com/avr>.

5. Disclaimer

For devices that are not available yet, typical values contained in this datasheet are based on simulations and characterization of other AVR XMEGA microcontrollers manufactured on the same process technology. Min. and Max values will be available after the device is characterized.

6. AVR CPU

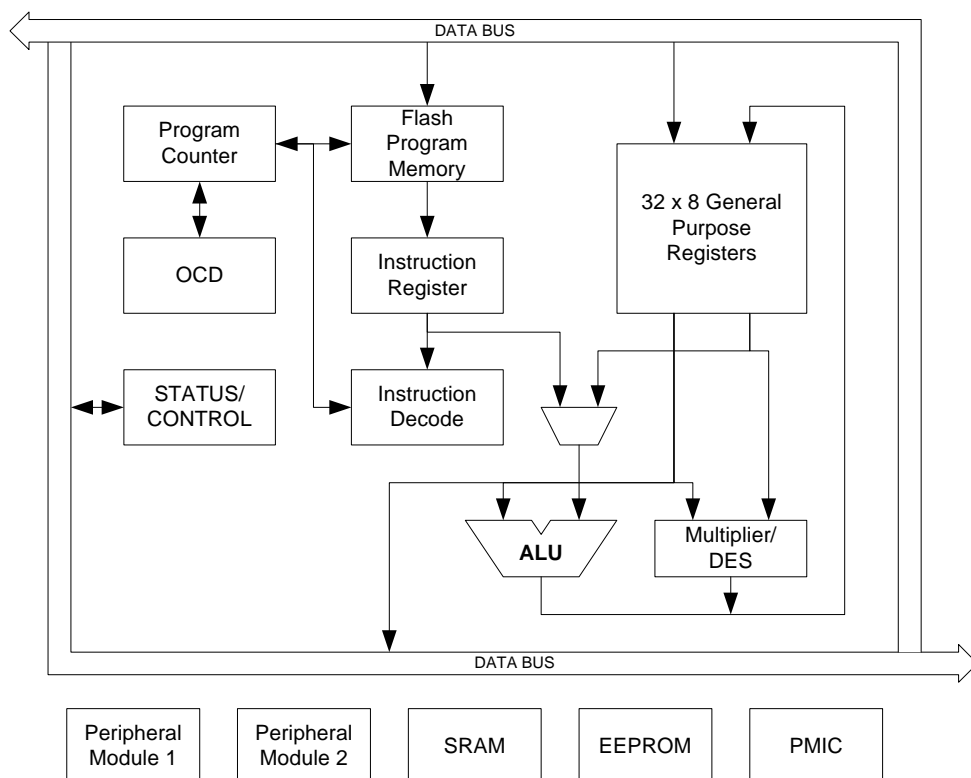
6.1 Features

- 8/16-bit high performance AVR RISC Architecture
 - 138 instructions
 - Hardware multiplier
- 32x8-bit registers directly connected to the ALU
- Stack in SRAM
- Stack Pointer accessible in I/O memory space
- Direct addressing of up to 16M Bytes of program and data memory
- True 16/24-bit access to 16/24-bit I/O registers
- Support for 8-, 16- and 32-bit Arithmetic
- Configuration Change Protection of system critical features

6.2 Overview

The XMEGA A3B uses the 8/16-bit AVR CPU. The main function of the CPU is program execution. The CPU must therefore be able to access memories, perform calculations and control peripherals. Interrupt handling is described in a separate section. [Figure 6-1 on page 6](#) shows the CPU block diagram.

Figure 6-1. CPU block diagram



The AVR uses a Harvard architecture - with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This

concept enables instructions to be executed in every clock cycle. The program memory is In-System Self-Programmable Flash memory.

6.3 Register File

The fast-access Register File contains 32 x 8-bit general purpose working registers with single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU cycle, the operation is performed on two Register File operands, and the result is stored back in the Register File.

Six of the 32 registers can be used as three 16-bit address register pointers for data space addressing - enabling efficient address calculations. One of these address pointers can also be used as an address pointer for look up tables in Flash program memory.

6.4 ALU - Arithmetic Logic Unit

The high performance Arithmetic Logic Unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed. After an arithmetic or logic operation, the Status Register is updated to reflect information about the result of the operation.

The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Both 8- and 16-bit arithmetic is supported, and the instruction set allows for easy implementation of 32-bit arithmetic. The ALU also provides a powerful multiplier supporting both signed and unsigned multiplication and fractional format.

6.5 Program Flow

When the device is powered on, the CPU starts to execute instructions from the lowest address in the Flash Program Memory '0'. The Program Counter (PC) addresses the next instruction to be fetched. After a reset, the PC is set to location '0'.

Program flow is provided by conditional and unconditional jump and call instructions, capable of addressing the whole address space directly. Most AVR instructions use a 16-bit word format, while a limited number uses a 32-bit format.

During interrupts and subroutine calls, the return address PC is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. After reset the Stack Pointer (SP) points to the highest address in the internal SRAM. The SP is read/write accessible in the I/O memory space, enabling easy implementation of multiple stacks or stack areas. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR CPU.

7. Memories

7.1 Features

- **Flash Program Memory**
 - One linear address space
 - In-System Programmable
 - Self-Programming and Bootloader support
 - Application Section for application code
 - Application Table Section for application code or data storage
 - Boot Section for application code or bootloader code
 - Separate lock bits and protection for all sections
 - Built in fast CRC check of a selectable flash program memory section
- **Data Memory**
 - One linear address space
 - Single cycle access from CPU
 - SRAM
 - EEPROM
 - Byte and page accessible
 - Optional memory mapping for direct load and store
 - I/O Memory
 - Configuration and Status registers for all peripherals and modules
 - 16 bit-accessible General Purpose Register for global variables or flags
 - Bus arbitration
 - Safe and deterministic handling of CPU and DMA Controller priority
 - Separate buses for SRAM, EEPROM, I/O Memory and External Memory access
 - Simultaneous bus access for CPU and DMA Controller
- **Production Signature Row Memory for factory programmed data**
 - Device ID for each microcontroller device type
 - Serial number for each device
 - Oscillator calibration bytes
 - ADC, DAC and temperature sensor calibration data
- **User Signature Row**
 - One flash page in size
 - Can be read and written from software
 - Content is kept after chip erase

7.2 Overview

The AVR architecture has two main memory spaces, the Program Memory and the Data Memory. In addition, the XMEGA A3B features an EEPROM Memory for non-volatile data storage. All three memory spaces are linear and require no paging. The available memory size configurations are shown in ["Ordering Information" on page 2](#). In addition each device has a Flash memory signature row for calibration data, device identification, serial number etc.

Non-volatile memory spaces can be locked for further write or read/write operations. This prevents unrestricted access to the application software.

7.3 In-System Programmable Flash Program Memory

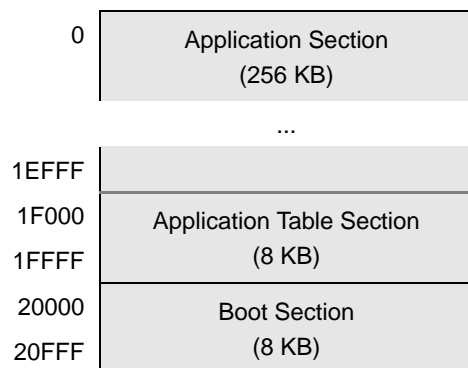
The XMEGA A3B devices contain On-chip In-System Programmable Flash memory for program storage, see [Figure 7-1 on page 9](#). Since all AVR instructions are 16- or 32-bits wide, each Flash address location is 16 bits.

The Program Flash memory space is divided into Application and Boot sections. Both sections have dedicated Lock Bits for setting restrictions on write or read/write operations. The Store Program Memory (SPM) instruction must reside in the Boot Section when used to write to the Flash memory.

A third section inside the Application section is referred to as the Application Table section which has separate Lock bits for storage of write or read/write protection. The Application Table section can be used for storing non-volatile data or application software.

Figure 7-1. Flash Program Memory (Hexadecimal address)

Word Address



The Application Table Section and Boot Section can also be used for general application software.

7.4 Data Memory

The Data Memory consists of the I/O Memory, EEPROM and SRAM memories, all within one linear address space, see [Figure 7-2 on page 9](#). To simplify development, the memory map for all devices in the family is identical and with empty, reserved memory space for smaller devices.

Figure 7-2. Data Memory Map (Hexadecimal address)

Byte Address

ATxmega256A3B

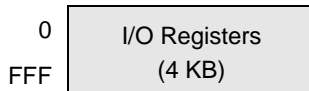
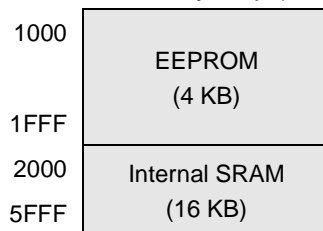


Figure 7-2. Data Memory Map (Hexadecimal address)

7.4.1 I/O Memory

All peripherals and modules are addressable through I/O memory locations in the data memory space. All I/O memory locations can be accessed by the Load (LD/LDS/LDD) and Store (ST/STS/STD) instructions, transferring data between the 32 general purpose registers in the CPU and the I/O Memory.

The IN and OUT instructions can address I/O memory locations in the range 0x00 - 0x3F directly.

I/O registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. The value of single bits can be checked by using the SBIS and SBIC instructions on these registers.

The I/O memory address for all peripherals and modules in XMEGA A3B is shown in the ["Peripheral Module Address Map" on page 55](#).

7.4.2 SRAM Data Memory

The XMEGA A3B devices have internal SRAM memory for data storage.

7.4.3 EEPROM Data Memory

The XMEGA A3B devices have internal EEPROM memory for non-volatile data storage. It is addressable either in a separate data space or it can be memory mapped into the normal data memory space. The EEPROM memory supports both byte and page access.

7.5 Production Signature Row

The Production Signature Row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules.

The production signature row also contains a device ID that identify each microcontroller device type, and a serial number that is unique for each manufactured device. The device ID for the available XMEGA A3 devices is shown in [Table 7-1 on page 12](#). The serial number consist of the production LOT number, wafer number, and wafer coordinates for the device.

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The production signature row can not be written or erased, but it can be read from both application software and external programming.

Table 7-1. .Device ID bytes for XMEGA A3B device.

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega256A3B	43	98	1E

7.7 User Signature Row

The User Signature Row is a separate memory section that is fully accessible (read and write) from application software and external programming. The user signature row is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial numbers or identification numbers, random number seeds etc. This section is not erased by Chip Erase commands that erase the Flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase session and on-chip debug sessions.

7.8 Flash and EEPROM Page Size

The Flash Program Memory and EEPROM data memory are organized in pages. The pages are word accessible for the Flash and byte accessible for the EEPROM.

[Table 7-2 on page 13](#) shows the Flash Program Memory organization. Flash write and erase operations are performed on one page at the time, while reading the Flash is done one byte at the time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

Table 7-2. Number of words and Pages in the Flash.

Devices	Flash Size	Page Size (words)	FWORD	FPAGE	Application		Boot	
					Size	No of Pages	Size	No of Pages
ATxmega256A3B	256 KB + 8 KB	256	Z[8:1]	Z[18:9]	256 KB	512	8 KB	16

[Table 7-3 on page 13](#) shows EEPROM memory organization for the XMEGA A3B devices. EEPROM write and erase operations can be performed one page or one byte at the time, while reading the EEPROM is done one byte at the time. For EEPROM access the NVM Address Register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

Table 7-3. Number of Bytes and Pages in the EEPROM.

Devices	EEPROM Size	Page Size (Bytes)	E2BYTE	E2PAGE	No of Pages
ATxmega256A3B	4 KB	32	ADDR[4:0]	ADDR[11:5]	128

8. DMAC - Direct Memory Access Controller

8.1 Features

- **Allows High-speed data transfer**
 - From memory to peripheral
 - From memory to memory
 - From peripheral to memory
 - From peripheral to peripheral
- **4 Channels**
- **From 1 byte and up to 16M bytes transfers in a single transaction**
- **Multiple addressing modes for source and destination address**
 - Increment
 - Decrement
 - Static
- **1, 2, 4, or 8 byte Burst Transfers**
- **Programmable priority between channels**

8.2 Overview

The XMEGA A3B has a Direct Memory Access (DMA) Controller to move data between memories and peripherals in the data space. The DMA controller uses the same data bus as the CPU to transfer data.

It has 4 channels that can be configured independently. Each DMA channel can perform data transfers in blocks of configurable size from 1 to 64K bytes. A repeat counter can be used to repeat each block transfer for single transactions up to 16M bytes. Each DMA channel can be configured to access the source and destination memory address with incrementing, decrementing or static addressing. The addressing is independent for source and destination address. When the transaction is complete the original source and destination address can automatically be reloaded to be ready for the next transaction.

The DMAC can access all the peripherals through their I/O memory registers, and the DMA may be used for automatic transfer of data to/from communication modules, as well as automatic data retrieval from ADC conversions, data transfer to DAC conversions, or data transfer to or from port pins. A wide range of transfer triggers are available from the peripherals, Event System and software. Each DMA channel has different transfer triggers.

To allow for continuous transfers, two channels can be interlinked so that the second takes over the transfer when the first is finished and vice versa.

The DMA controller can read from memory mapped EEPROM, but it cannot write to the EEPROM or access the Flash.

9. Event System

9.1 Features

- Inter-peripheral communication and signalling with minimum latency
- CPU and DMA independent operation
- 8 Event Channels allows for up to 8 signals to be routed at the same time
- Events can be generated by
 - Timer/Counters (TCxn)
 - Real Time Counter (RTC)
 - Analog to Digital Converters (ADCx)
 - Analog Comparators (ACx)
 - Ports (PORTx)
 - System Clock (Clk_{sys})
 - Software (CPU)
- Events can be used by
 - Timer/Counters (TCxn)
 - Analog to Digital Converters (ADCx)
 - Digital to Analog Converters (DACx)
 - Ports (PORTx)
 - DMA Controller (DMAC)
 - IR Communication Module (IRCOM)
- The same event can be used by multiple peripherals for synchronized timing
- Advanced Features
 - Manual Event Generation from software (CPU)
 - Quadrature Decoding
 - Digital Filtering
- Functions in Active and Idle mode

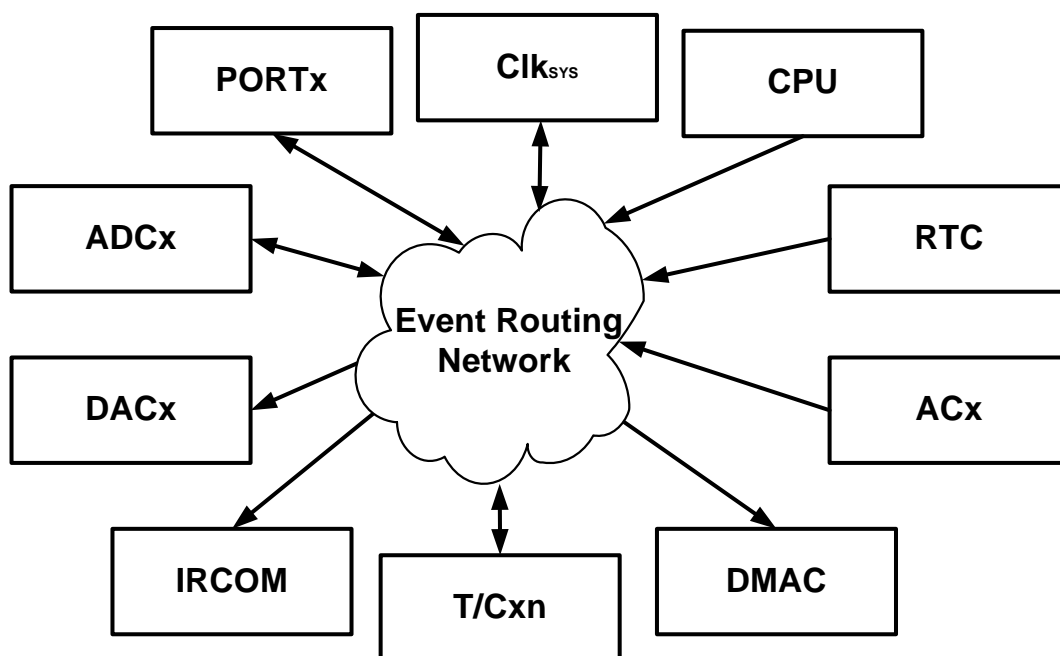
9.2 Overview

The Event System is a set of features for inter-peripheral communication. It enables the possibility for a change of state in one peripheral to automatically trigger actions in one or more peripherals. What changes in a peripheral that will trigger actions in other peripherals are configurable by software. It is a simple, but powerful system as it allows for autonomous control of peripherals without any use of interrupts, CPU or DMA resources.

The indication of a change in a peripheral is referred to as an event, and is usually the same as the interrupt conditions for that peripheral. Events are passed between peripherals using a dedicated routing network called the Event Routing Network. [Figure 9-1 on page 16](#) shows a basic block diagram of the Event System with the Event Routing Network and the peripherals to which it is connected. This highly flexible system can be used for simple routing of signals, pin functions or for sequencing of events.

The maximum latency is two CPU clock cycles from when an event is generated in one peripheral, until the actions are triggered in one or more other peripherals.

The Event System is functional in both Active and Idle modes.

Figure 9-1. Event system block diagram.

The Event Routing Network can directly connect together ADCs, DACs, Analog Comparators (ACx), I/O ports (PORTx), the Real-time Counter (RTC), Timer/Counters (T/C) and the IR Communication Module (IRCOM). Events can also be generated from software (CPU).

All events from all peripherals are always routed into the Event Routing Network. This consists of eight multiplexers where each can be configured in software to select which event to be routed into that event channel. All eight event channels are connected to the peripherals that can use events, and each of these peripherals can be configured to use events from one or more event channels to automatically trigger a software selectable action.

10. System Clock and Clock options

10.1 Features

- **Fast start-up time**
- **Safe run-time clock switching**
- **Internal Oscillators:**
 - **32 MHz run-time calibrated RC oscillator**
 - **2 MHz run-time calibrated RC oscillator**
 - **32.768 kHz calibrated RC oscillator**
 - **32 kHz Ultra Low Power (ULP) oscillator**
- **External clock options**
 - **0.4 - 16 MHz Crystal Oscillator**
 - **32 kHz Crystal Oscillator**
 - **External clock**
- **PLL with internal and external clock options with 2 to 31x multiplication**
- **Clock Prescalers with 2 to 2048x division**
- **Fast peripheral clock running at 2 and 4 times the CPU clock speed**
- **Automatic Run-Time Calibration of internal oscillators**
- **Crystal Oscillator failure detection**

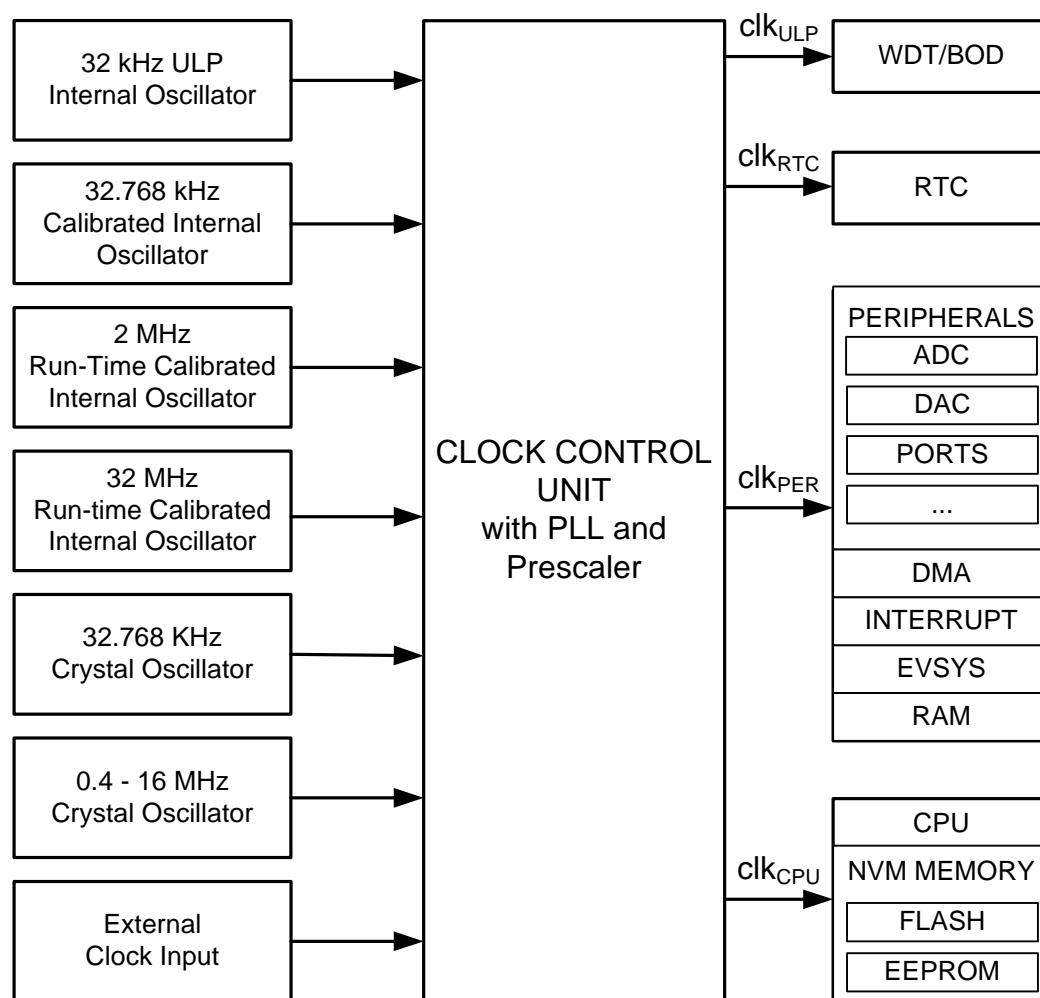
10.2 Overview

XMEGA A3B has an advanced clock system, supporting a large number of clock sources. It incorporates both integrated oscillators, external crystal oscillators and resonators. A high frequency Phase Locked Loop (PLL) and clock prescalers can be controlled from software to generate a wide range of clock frequencies from the clock source input.

It is possible to switch between clock sources from software during run-time. After reset the device will always start up running from the 2 Mhz internal oscillator.

A calibration feature is available, and can be used for automatic run-time calibration of the internal 2 MHz and 32 MHz oscillators. This reduce frequency drift over voltage and temperature.

A Crystal Oscillator Failure Monitor can be enabled to issue a Non-Maskable Interrupt and switch to internal oscillator if the external oscillator fails. [Figure 10-1 on page 18](#) shows the principal clock system in XMEGA A3B.

Figure 10-1. Clock system overview


Each clock source is briefly described in the following sub-sections.

10.3 Clock Options

10.3.1 32 kHz Ultra Low Power Internal Oscillator

The 32 kHz Ultra Low Power (ULP) Internal Oscillator is a very low power consumption clock source. It is used for the Watchdog Timer, Brown-Out Detection and as an asynchronous clock source for the Real Time Counter. This oscillator cannot be used as the system clock source, and it cannot be directly controlled from software.

10.3.2 32.768 kHz Calibrated Internal Oscillator

The 32.768 kHz Calibrated Internal Oscillator is a high accuracy clock source that can be used as the system clock source or as an asynchronous clock source for the Real Time Counter. It is calibrated during production to provide a default frequency which is close to its nominal frequency.

10.3.3 32.768 kHz Crystal Oscillator

The 32.768 kHz Crystal Oscillator is a low power driver for an external watch crystal. It can be used as system clock source or as asynchronous clock source for the Real Time Counter.

10.3.4 0.4 - 16 MHz Crystal Oscillator

The 0.4 - 16 MHz Crystal Oscillator is a driver intended for driving both external resonators and crystals ranging from 400 kHz to 16 MHz.

10.3.5 2 MHz Run-time Calibrated Internal Oscillator

The 2 MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator. It is calibrated during production to provide a default frequency which is close to its nominal frequency. The oscillator can use the 32 kHz Calibrated Internal Oscillator or the 32 kHz Crystal Oscillator as a source for calibrating the frequency run-time to compensate for temperature and voltage drift hereby optimizing the accuracy of the oscillator.

10.3.6 32 MHz Run-time Calibrated Internal Oscillator

The 32 MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator. It is calibrated during production to provide a default frequency which is close to its nominal frequency. The oscillator can use the 32 kHz Calibrated Internal Oscillator or the 32 kHz Crystal Oscillator as a source for calibrating the frequency run-time to compensate for temperature and voltage drift hereby optimizing the accuracy of the oscillator.

10.3.7 External Clock input

The external clock input gives the possibility to connect a clock from an external source.

10.3.8 PLL with Multiplication factor 2 - 31x

The PLL provides the possibility of multiplying a frequency by any number from 2 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

11. Power Management and Sleep Modes

11.1 Features

- 5 sleep modes
 - Idle
 - Power-down
 - Power-save
 - Standby
 - Extended standby
- Power Reduction registers to disable clocks to unused peripherals

11.2 Overview

The XMEGA A3B provides various sleep modes tailored to reduce power consumption to a minimum. All sleep modes are available and can be entered from Active mode. In Active mode the CPU is executing application code. The application code decides when and what sleep mode to enter. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to Active mode.

In addition, Power Reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen and there is no power consumption from that peripheral. This reduces the power consumption in Active mode and Idle sleep mode.

11.3 Sleep Modes

11.3.1 Idle Mode

In Idle mode the CPU and Non-Volatile Memory are stopped, but all peripherals including the Interrupt Controller, Event System and DMA Controller are kept running. Interrupt requests from all enabled interrupts will wake the device.

11.3.2 Power-down Mode

In Power-down mode all system clock sources, and the asynchronous Real Time Counter (RTC) clock source, are stopped. This allows operation of asynchronous modules only. The only interrupts that can wake up the MCU are the Two Wire Interface address match interrupts, and asynchronous port interrupts, e.g pin change.

11.3.3 Power-save Mode

Power-save mode is identical to Power-down, with one exception: If the RTC is enabled, it will keep running during sleep and the device can also wake up from RTC interrupts.

11.3.4 Standby Mode

Standby mode is identical to Power-down with the exception that all enabled system clock sources are kept running, while the CPU, Peripheral and RTC clocks are stopped. This reduces the wake-up time when external crystals or resonators are used.

11.3.5 Extended Standby Mode

Extended Standby mode is identical to Power-save mode with the exception that all enabled system clock sources are kept running while the CPU and Peripheral clocks are stopped. This reduces the wake-up time when external crystals or resonators are used.

12. System Control and Reset

12.1 Features

- Multiple reset sources for safe operation and device reset
 - Power-On Reset
 - External Reset
 - Watchdog Reset
 - The Watchdog Timer runs from separate, dedicated oscillator
 - Brown-Out Reset
 - Accurate, programmable Brown-Out levels
 - JTAG Reset
 - PDI reset
 - Software reset
- Asynchronous reset
 - No running clock in the device is required for reset
- Reset status register

12.2 Resetting the AVR

During reset, all I/O registers are set to their initial values. The SRAM content is not reset. Application execution starts from the Reset Vector. The instruction placed at the Reset Vector should be an Absolute Jump (JMP) instruction to the reset handling routine. By default the Reset Vector address is the lowest Flash program memory address, '0', but it is possible to move the Reset Vector to the first address in the Boot Section.

The I/O ports of the AVR are immediately tri-stated when a reset source goes active.

The reset functionality is asynchronous, so no running clock is required to reset the device.

After the device is reset, the reset source can be determined by the application by reading the Reset Status Register.

12.3 Reset Sources

12.3.1 Power-On Reset

The MCU is reset when the supply voltage VCC is below the Power-on Reset threshold voltage.

12.3.2 External Reset

The MCU is reset when a low level is present on the RESET pin.

12.3.3 Watchdog Reset

The MCU is reset when the Watchdog Timer period expires and the Watchdog Reset is enabled. The Watchdog Timer runs from a dedicated oscillator independent of the System Clock. For more details see ["WDT - Watchdog Timer" on page 23](#).

12.3.4 Brown-Out Reset

The MCU is reset when the supply voltage VCC is below the Brown-Out Reset threshold voltage and the Brown-out Detector is enabled. The Brown-out threshold voltage is programmable.

12.3.5 JTAG reset

The MCU is reset as long as there is a logic one in the Reset Register in one of the scan chains of the JTAG system. Refer to IEEE 1149.1 (JTAG) Boundary-scan for details.

12.3.6 PDI reset

The MCU can be reset through the Program and Debug Interface (PDI).

12.3.7 Software reset

The MCU can be reset by the CPU writing to a special I/O register through a timed sequence.

12.4 WDT - Watchdog Timer

12.4.1 Features

- **11 selectable timeout periods, from 8 ms to 8s.**
- **Two operation modes**
 - **Standard mode**
 - **Window mode**
- **Runs from the 1 kHz output of the 32 kHz Ultra Low Power oscillator**
- **Configuration lock to prevent unwanted changes**

12.4.2 Overview

The XMEGA A3B has a Watchdog Timer (WDT). The WDT will run continuously when turned on and if the Watchdog Timer is not reset within a software configurable time-out period, the microcontroller will be reset. The Watchdog Reset (WDR) instruction must be run by software to reset the WDT, and prevents microcontroller reset.

The WDT has a Window mode. In this mode the WDR instruction must be run within a specified period called a window. Application software can set the minimum and maximum limits for this window. If the WDR instruction is not executed inside the window limits, the microcontroller will be reset.

A protection mechanism using a timed write sequence is implemented in order to prevent unwanted enabling, disabling or change of WDT settings.

For maximum safety, the WDT also has an Always-on mode. This mode is enabled by programming a fuse. In Always-on mode, application software can not disable the WDT.

13. Battery Backup System

13.1 Features

- Battery Backup voltage supply from dedicated V_{BAT} power pin for:
 - One Ultra Low-power 32-bit Real Time Counter
 - One 32.768 kHz crystal oscillator with failure detection monitor
 - Two Backup Registers
- Typical power consumption of 500nA with Real Time Counter (RTC) running
- Automatic switching from main power to battery backup power at:
 - Brown-Out Detection (BOD) reset
- Automatic switching from battery backup power to main power:
 - Device reset after Brown-Out Reset (BOR) is released
 - Device reset after Power-On Reset (POR) and BOR is released

13.2 Overview

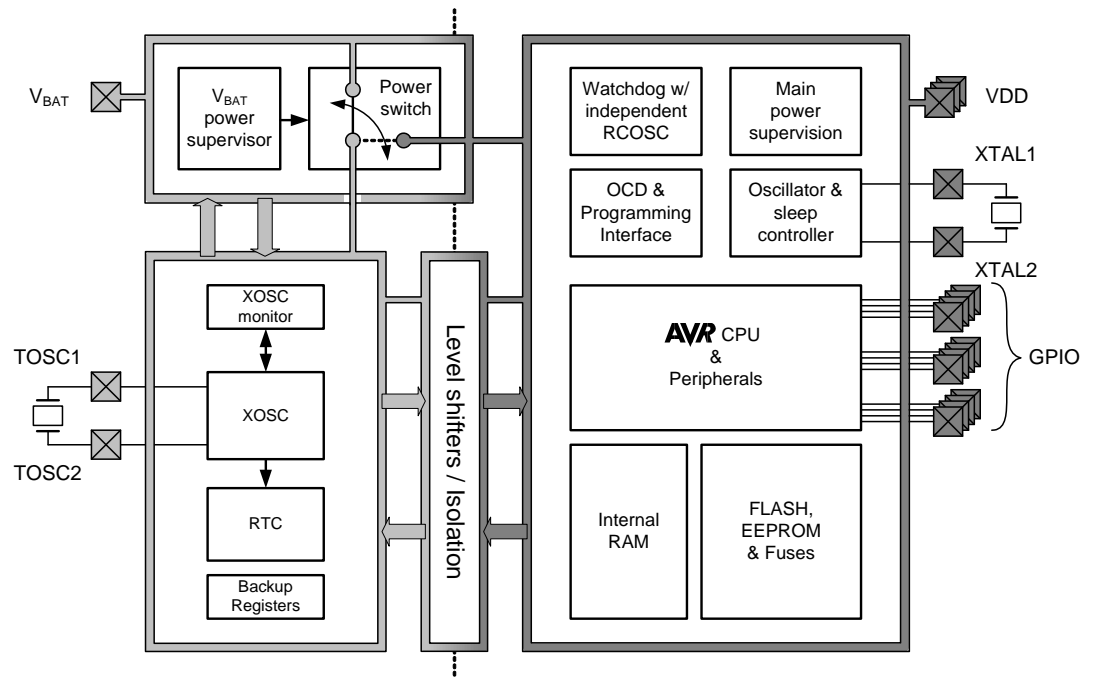
The AVR XMEGA family is already running in an ultra low leakage process with power-save current consumption below 2 μ A with RTC, BOD and watchdog enabled. Still, for some applications where time keeping is important, the system would have one main battery or power source used for day to day tasks, and one backup battery power for the time keeping functionality. The Battery Backup System includes functionality that enable automatic power switching between main power and a battery backup power. [Figure 13-1 on page 25](#) shows an overview of the system.

The Battery Backup Module support connection of a backup battery to the dedicated V_{BAT} power pin. This will ensure power to the 32-bit Real Time Counter, a 32.768 kHz crystal oscillator with failure detection monitor and two backup registers, when the main battery or power source is unavailable.

Upon main power loss the device will automatically detect this and the Battery Backup Module will switch to be powered from the V_{BAT} pin. After main power has been restored and both main POR and BOR are released, the Battery Backup Module will automatically switch back to be powered from main power again.

The 32-bit Real Time Counter (RTC) must be clocked from the 1 Hz output of a 32.768 kHz crystal oscillator connected between the TOSC1 and TOSC2 pins when running from V_{BAT} . For more details on the 32-bit RTC refer to the “RTC32 - 32-bit Real Time Counter” section in the XMEGA A Manual.

Figure 13-1. Battery Backup Module and its power domain implementation



14. PMIC - Programmable Multi-level Interrupt Controller

14.1 Features

- Separate interrupt vector for each interrupt
- Short, predictable interrupt response time
- Programmable Multi-level Interrupt Controller
 - 3 programmable interrupt levels
 - Selectable priority scheme within low level interrupts (round-robin or fixed)
 - Non-Maskable Interrupts (NMI)
- Interrupt vectors can be moved to the start of the Boot Section

14.2 Overview

XMEGA A3B has a Programmable Multi-level Interrupt Controller (PMIC). All peripherals can define three different priority levels for interrupts; high, medium or low. Medium level interrupts may interrupt low level interrupt service routines. High level interrupts may interrupt both low- and medium level interrupt service routines. Low level interrupts have an optional round robin scheme to make sure all interrupts are serviced within a certain amount of time.

The built in oscillator failure detection mechanism can issue a Non-Maskable Interrupt (NMI).

14.3 Interrupt vectors

When an interrupt is serviced, the program counter will jump to the interrupt vector address. The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the XMEGA A3B devices are shown in [Table 14-1](#). Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA A manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in [Table 14-1](#). The program address is the word address.

Table 14-1. Reset and Interrupt Vectors

Program Address (Base Address)	Source	Interrupt Description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal Oscillator Failure Interrupt vector (NMI)
0x004	PORTC_INT_base	Port C Interrupt base
0x008	PORTR_INT_base	Port R Interrupt base
0x00C	DMA_INT_base	DMA Controller Interrupt base
0x014	RTC32_INT_base	32-bit Real Time Counter Interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C Interrupt base
0x01C	TCC0_INT_base	Timer/Counter 0 on port C Interrupt base
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x038	USARTC1_INT_base	USART 1 on port C Interrupt base
0x03E	AES_INT_vect	AES Interrupt vector

Table 14-1. Reset and Interrupt Vectors (Continued)

Program Address (Base Address)	Source	Interrupt Description
0x040	NVM_INT_base	Non-Volatile Memory Interrupt base
0x044	PORTB_INT_base	Port B Interrupt base
0x048	ACB_INT_base	Analog Comparator on Port B Interrupt base
0x04E	ADCB_INT_base	Analog to Digital Converter on Port B Interrupt base
0x056	PORTE_INT_base	Port E Interrupt base
0x05A	TWIE_INT_base	Two-Wire Interface on Port E Interrupt base
0x05E	TCE0_INT_base	Timer/Counter 0 on port E Interrupt base
0x06A	TCE1_INT_base	Timer/Counter 1 on port E Interrupt base
0x074	USARTE0_INT_base	USART 0 on port E Interrupt base
0x080	PORTD_INT_base	Port D Interrupt base
0x084	PORTA_INT_base	Port A Interrupt base
0x088	ACA_INT_base	Analog Comparator on Port A Interrupt base
0x08E	ADCA_INT_base	Analog to Digital Converter on Port A Interrupt base
0x09A	TCD0_INT_base	Timer/Counter 0 on port D Interrupt base
0x0A6	TCD1_INT_base	Timer/Counter 1 on port D Interrupt base
0x0AE	SPID_INT_vector	SPI on port D Interrupt vector
0x0B0	USARTD0_INT_base	USART 0 on port D Interrupt base
0x0B6	USARTD1_INT_base	USART 1 on port D Interrupt base
0x0D0	PORTF_INT_base	Port F INT base
0x0D8	TCF0_INT_base	Timer/Counter 0 on port F Interrupt base
0x0EE	USARTF0_INT_base	USART 0 on port F Interrupt base

15. I/O Ports

15.1 Features

- Selectable input and output configuration for each pin individually
- Flexible pin configuration through dedicated Pin Configuration Register
- Synchronous and/or asynchronous input sensing with port interrupts and events
 - Sense both edges
 - Sense rising edges
 - Sense falling edges
 - Sense low level
- Asynchronous wake-up from all input sensing configurations
- Two port interrupts with flexible pin masking
- Highly configurable output driver and pull settings:
 - Totem-pole
 - Pull-up/-down
 - Wired-AND
 - Wired-OR
 - Bus-keeper
 - Inverted I/O
- Optional Slew rate control
- Configuration of multiple pins in a single operation
- Read-Modify-Write (RMW) support
- Toggle/clear/set registers for Output and Direction registers
- Clock output on port pin
- Event Channel 7 output on port pin
- Mapping of port registers (virtual ports) into bit accessible I/O memory space

15.2 Overview

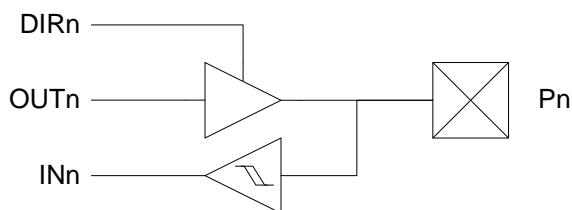
The XMEGA A3B devices have flexible General Purpose I/O Ports. A port consists of up to 8 pins, ranging from pin 0 to pin 7. The ports implement several functions, including synchronous/asynchronous input sensing, pin change interrupts and configurable output settings. All functions are individual per pin, but several pins may be configured in a single operation.

15.3 I/O configuration

All port pins (Pn) have programmable output configuration. In addition, all port pins have an inverted I/O function. For an input, this means inverting the signal between the port pin and the pin register. For an output, this means inverting the output signal between the port register and the port pin. The inverted I/O function can be used also when the pin is used for alternate functions. The port pins also have configurable slew rate limitation to reduce electromagnetic emission.

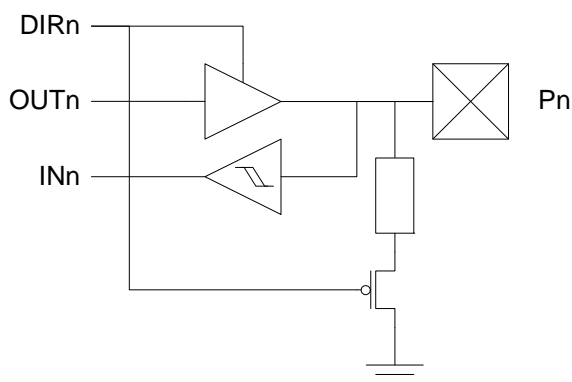
15.3.1 Push-pull

Figure 15-1. I/O configuration - Totem-pole



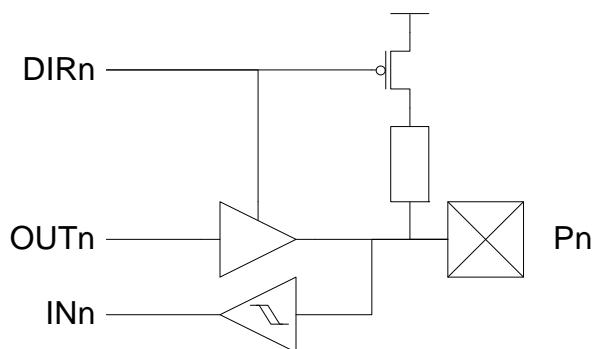
15.3.2 Pull-down

Figure 15-2. I/O configuration - Totem-pole with pull-down (on input)



15.3.3 Pull-up

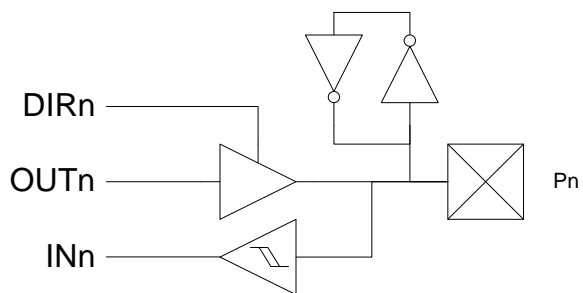
Figure 15-3. I/O configuration - Totem-pole with pull-up (on input)



15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 15-4. I/O configuration - Totem-pole with bus-keeper



15.3.5 Others

Figure 15-5. Output configuration - Wired-OR with optional pull-down

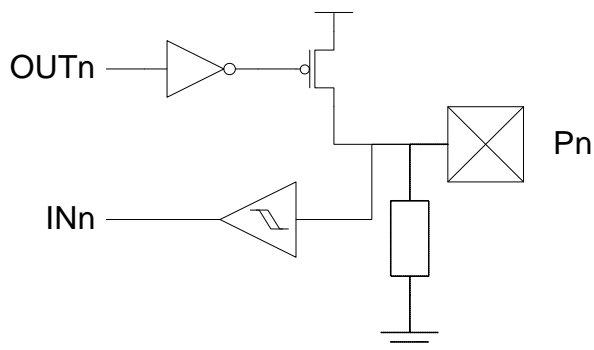
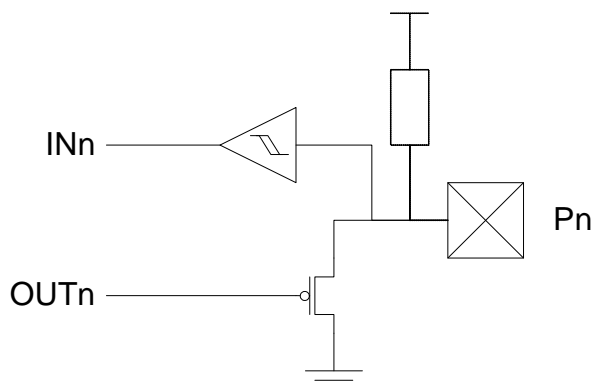


Figure 15-6. I/O configuration - Wired-AND with optional pull-up

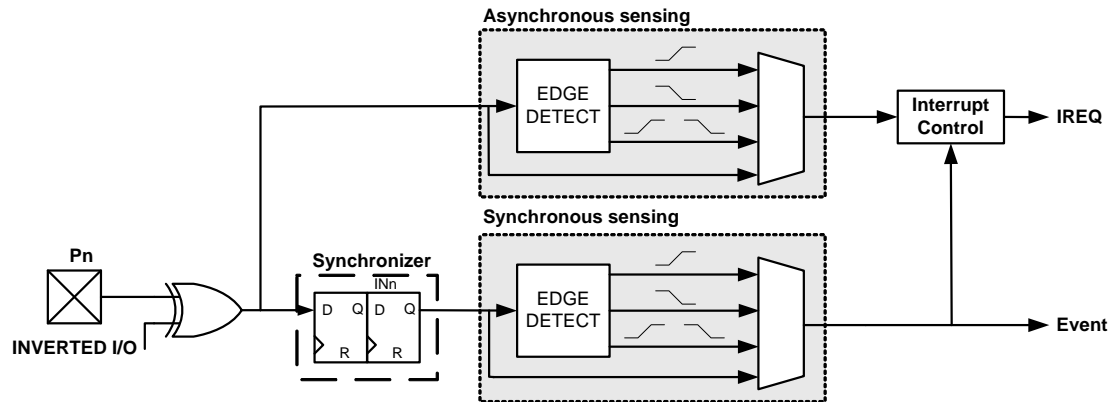


15.4 Input sensing

- Sense both edges
- Sense rising edges
- Sense falling edges
- Sense low level

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in [Figure 15-7 on page 31](#).

Figure 15-7. Input sensing system overview



When a pin is configured with inverted I/O the pin value is inverted before the input sensing.

15.5 Port Interrupt

Each port has two interrupts with separate priority and interrupt vector. All pins on the port can be individually selected as source for each of the interrupts. The interrupts are then triggered according to the input sense configuration for each pin configured as source for the interrupt.

15.6 Alternate Port Functions

In addition to the input/output functions on all port pins, most pins have alternate functions. This means that other modules or peripherals connected to the port can use the port pins for their functions, such as communication or pulse-width modulation. ["Pinout and Pin Functions" on page 50](#) shows which modules on peripherals that enables alternate functions on a pin, and what alternate functions that is available on a pin.

16. T/C - 16-bit Timer/Counter with PWM

16.1 Features

- **Seven 16-bit Timer/Counters**
 - Four Timer/Counters of type 0
 - Three Timer/Counters of type 1
- **Four Compare or Capture (CC) Channels in Timer/Counter 0**
- **Two Compare or Capture (CC) Channels in Timer/Counter 1**
- **Double Buffered Timer Period Setting**
- **Double Buffered Compare or Capture Channels**
- **Waveform Generation:**
 - Single Slope Pulse Width Modulation
 - Dual Slope Pulse Width Modulation
 - Frequency Generation
- **Input Capture:**
 - Input Capture with Noise Cancelling
 - Frequency capture
 - Pulse width capture
 - 32-bit input capture
- **Event Counter with Direction Control**
- **Timer Overflow and Timer Error Interrupts and Events**
- **One Compare Match or Capture Interrupt and Event per CC Channel**
- **Supports DMA Operation**
- **Hi-Resolution Extension (Hi-Res)**
- **Advanced Waveform Extension (AWEX)**

16.2 Overview

XMEGA A3B has seven Timer/Counters, four Timer/Counter 0 and three Timer/Counter 1. The difference between them is that Timer/Counter 0 has four Compare/Capture channels, while Timer/Counter 1 has two Compare/Capture channels.

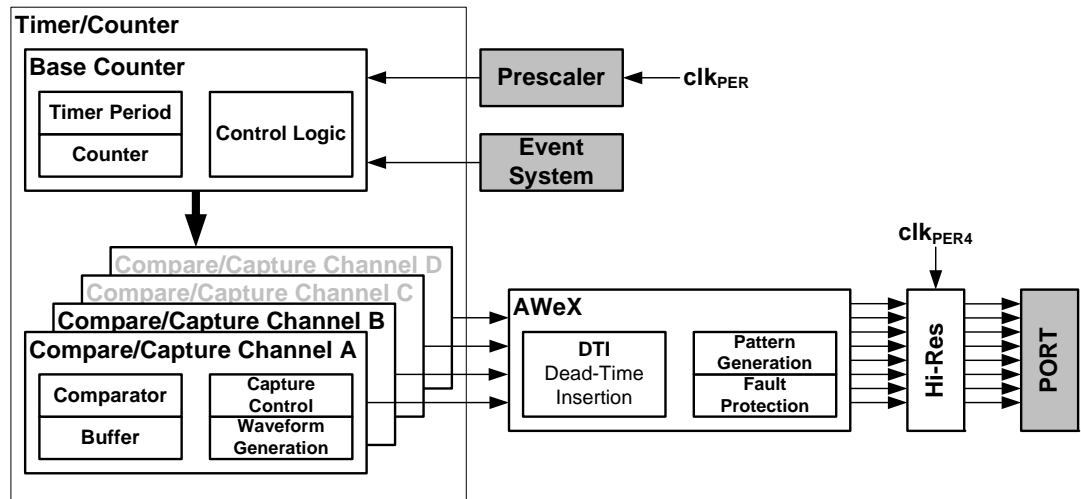
The Timer/Counters (T/C) are 16-bit and can count any clock, event or external input in the microcontroller. A programmable prescaler is available to get a useful T/C resolution. Updates of Timer and Compare registers are double buffered to ensure glitch free operation. Single slope PWM, dual slope PWM and frequency generation waveforms can be generated using the Compare Channels.

Through the Event System, any input pin or event in the microcontroller can be used to trigger input capture, hence no dedicated pins are required for this. The input capture has a noise canceller to avoid incorrect capture of the T/C, and can be used to do frequency and pulse width measurements.

A wide range of interrupt or event sources are available, including T/C Overflow, Compare match and Capture for each Compare/Capture channel in the T/C.

PORTC, PORTD and PORTE each has one Timer/Counter 0 and one Timer/Counter1. PORTE has one Timer/Counter 0. Notation of these are TCC0 (Time/Counter C0), TCC1, TCD0, TCD1, TCE0, TCE1 and TCF0, respectively.

Figure 16-1. Overview of a Timer/Counter and closely related peripherals



The Hi-Resolution Extension can be enabled to increase the waveform generation resolution by 2 bits (4x). This is available for all Timer/Counters. See ["Hi-Res - High Resolution Extension"](#) on [page 35](#) for more details.

The Advanced Waveform Extension can be enabled to provide extra and more advanced features for the Timer/Counter. This are only available for Timer/Counter 0. See ["AWEX - Advanced Waveform Extension"](#) on [page 34](#) for more details.

17. AWEX - Advanced Waveform Extension

17.1 Features

- **Output with complementary output from each Capture channel**
- **Four Dead Time Insertion (DTI) Units, one for each Capture channel**
- **8-bit DTI Resolution**
- **Separate High and Low Side Dead-Time Setting**
- **Double Buffered Dead-Time**
- **Event Controlled Fault Protection**
- **Single Channel Multiple Output Operation (for BLDC motor control)**
- **Double Buffered Pattern Generation**

17.2 Overview

The Advanced Waveform Extension (AWEX) provides extra features to the Timer/Counter in Waveform Generation (WG) modes. The AWEX enables easy and safe implementation of for example, advanced motor control (AC, BLDC, SR, and Stepper) and power control applications.

Any WG output from a Timer/Counter 0 is split into a complimentary pair of outputs when any AWEX feature is enabled. These output pairs go through a Dead-Time Insertion (DTI) unit that enables generation of the non-inverted Low Side (LS) and inverted High Side (HS) of the WG output with dead time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting. Optionally the final output can be inverted by using the invert I/O setting for the port pin.

The Pattern Generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the waveform generator output from Compare Channel A can be distributed to, and override all port pins. When the Pattern Generator unit is enabled, the DTI unit is bypassed.

The Fault Protection unit is connected to the Event System. This enables any event to trigger a fault condition that will disable the AWEX output. Several event channels can be used to trigger fault on several different conditions.

The AWEX is available for TCC0. The notation is AWEXC.

18. Hi-Res - High Resolution Extension

18.1 Features

- **Increases Waveform Generator resolution by 2-bits (4x)**
- **Supports Frequency, single- and dual-slope PWM operation**
- **Supports the AWEX when this is enabled and used for the same Timer/Counter**

18.2 Overview

The Hi-Resolution (Hi-Res) Extension is able to increase the resolution of the waveform generation output by a factor of 4. When enabled for a Timer/Counter, the Fast Peripheral clock running at four times the CPU clock speed will be as input to the Timer/Counter.

The High Resolution Extension can also be used when an AWEX is enabled and used with a Timer/Counter.

XMEGA A3B devices have four Hi-Res Extensions that each can be enabled for each Timer/Counter pair on PORTC, PORTD, PORTE and PORTF. The notation of these are HIRESC, HIRESD, HIRESE and HIRESF, respectively.

19. RTC32 - 32-bit Real-Time Counter

19.1 Features

- 32-bit resolution
- One 32-bit Compare register
- One 32-bit Period register
- Clear Timer on overflow
- Optional Interrupt/ Event on overflow and compare match
- Selectable clock reference
 - 1.024 kHz
 - 1 Hz
- Isolated V_{BAT} power domain with dynamic switch over from/to V_{CC} power domain¹

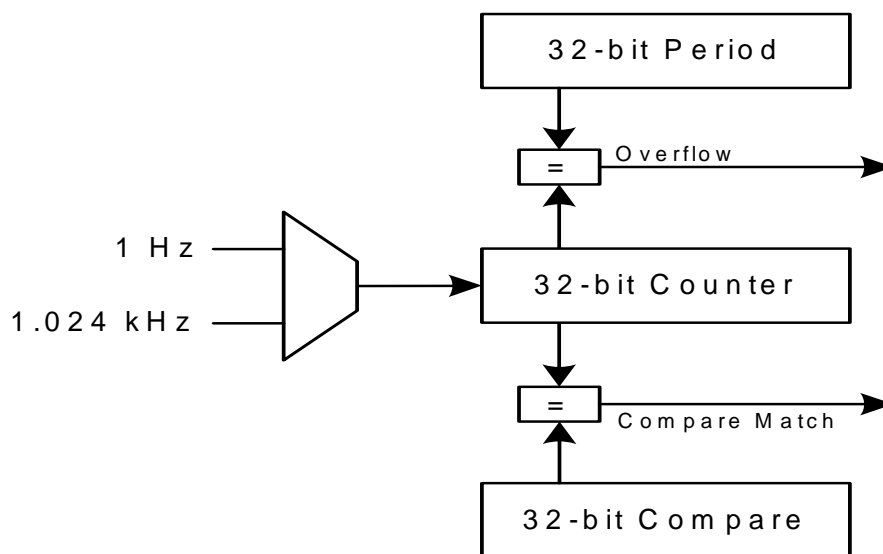
19.1.1 Overview

The 32-bit Real Time Counter (RTC) is a 32-bit counter, counting reference clock cycles and giving an event and/or an interrupt request when it reaches a configurable compare and/or top value. The reference clock is generated from a high accuracy 32.768 kHz crystal, and the design is optimized for low power consumption. The RTC typically operate in low power sleep modes, keeping track of time and waking up the device at regular intervals.

The RTC input clock can be taken from a 1.024 kHz or 1 Hz prescaled output from the 32.768 kHz reference clock. The RTC will give a compare interrupt request and/or event when the counter value equals the Compare register value. The RTC will give an overflow interrupt request and/or event when the counter value equals the Period register value. Counter overflow will also reset the counter value to zero.

The 32-bit Real Time Counter (RTC) must be clocked from the 1 Hz output of a 32.768 kHz crystal oscillator connected between the TOSC1 and TOSC2 pins when running from V_{BAT} . For more details on the 32-bit RTC refer to the “32-bit Real Time Counter” section in the XMEGA A Manual.

Figure 19-1. Real Time Counter Overview



20. TWI - Two Wire Interface

20.1 Features

- **Two Identical TWI peripherals**
- **Simple yet Powerful and Flexible Communication Interface**
- **Both Master and Slave Operation Supported**
- **Device can Operate as Transmitter or Receiver**
- **7-bit Address Space Allows up to 128 Different Slave Addresses**
- **Multi-master Arbitration Support**
- **Up to 400 kHz Data Transfer Speed**
- **Slew-rate Limited Output Drivers**
- **Noise Suppression Circuitry Rejects Spikes on Bus Lines**
- **Fully Programmable Slave Address with General Call Support**
- **Address Recognition Causes Wake-up when in Sleep Mode**
- **I²C and System Management Bus (SMBus) compatible**

20.2 Overview

The Two-Wire Interface (TWI) is a bi-directional wired-AND bus with only two lines, the clock (SCL) line and the data (SDA) line. The protocol makes it possible to interconnect up to 128 individually addressable devices. Since it is a multi-master bus, one or more devices capable of taking control of the bus can be connected.

The only external hardware needed to implement the bus is a single pull-up resistor for each of the TWI bus lines. Mechanisms for resolving bus contention are inherent in the TWI protocol.

PORTC and PORTE, each has one TWI. Notation of these peripherals are TWIC, and TWIE, respectively.

21. SPI - Serial Peripheral Interface

21.1 Features

- Two Identical SPI peripherals
- Full-duplex, Three-wire Synchronous Data Transfer
- Master or Slave Operation
- LSB First or MSB First Data Transfer
- Seven Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wake-up from Idle Mode
- Double Speed (CK/2) Master SPI Mode

21.2 Overview

The Serial Peripheral Interface (SPI) allows high-speed full-duplex, synchronous data transfer between different devices. Devices can communicate using a master-slave scheme, and data is transferred both to and from the devices simultaneously.

PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID, respectively.

22. USART

22.1 Features

- Six Identical USART peripherals
- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Master or Slave Clocked Synchronous Operation
- High-resolution Arithmetic Baud Rate Generator
- Supports Serial Frames with 5, 6, 7, 8, or 9 Data Bits and 1 or 2 Stop Bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Noise Filtering Includes False Start Bit Detection and Digital Low Pass Filter
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete
- Multi-processor Communication Mode
- Double Speed Asynchronous Communication Mode
- Master SPI mode for SPI communication
- IrDA support through the IRCOM module

22.2 Overview

The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication module. The USART supports full duplex communication, and both asynchronous and clocked synchronous operation. The USART can also be set in Master SPI mode to be used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both direction, enabling continued data transmission without any delay between frames. There are separate interrupt vectors for receive and transmit complete, enabling fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

One USART can use the IRCOM module to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2 kbps.

PORTC and PORTD each has two USARTs, while PORTE and PORTF each has one USART. Notation of these peripherals are USARTC0, USARTC1, USARTD0, USARTD1, USARTE0 and USARTF0, respectively.

23. IRCOM - IR Communication Module

23.1 Features

- Pulse modulation/demodulation for infrared communication
- Compatible to IrDA 1.4 physical for baud rates up to 115.2 kbps
- Selectable pulse modulation scheme
 - 3/16 of baud rate period
 - Fixed pulse period, 8-bit programmable
 - Pulse modulation disabled
- Built in filtering
- Can be connected to and used by one USART at the time

23.2 Overview

XMEGA A3B contains an Infrared Communication Module (IRCOM) for IrDA communication with baud rates up to 115.2 kbps. This supports three modulation schemes: 3/16 of baud rate period, fixed programmable pulse time based on the Peripheral Clock speed, or pulse modulation disabled. There is one IRCOM available which can be connected to any USART to enable infrared pulse coding/decoding for that USART.

24. Crypto Engine

24.1 Features

- **Data Encryption Standard (DES) CPU instruction**
- **Advanced Encryption Standard (AES) Crypto module**
- **DES Instruction**
 - **Encryption and Decryption**
 - **Single-cycle DES instruction**
 - **Encryption/Decryption in 16 clock cycles per 8-byte block**
- **AES Crypto Module**
 - **Encryption and Decryption**
 - **Support 128-bit keys**
 - **Support XOR data load mode to the State memory for Cipher Block Chaining**
 - **Encryption/Decryption in 375 clock cycles per 16-byte block**

24.2 Overview

The Advanced Encryption Standard (AES) and Data Encryption Standard (DES) are two commonly used encryption standards. These are supported through an AES peripheral module and a DES CPU instruction. All communication interfaces and the CPU can optionally use AES and DES encrypted communication and data storage.

DES is supported by a DES instruction in the AVR XMEGA CPU. The 8-byte key and 8-byte data blocks must be loaded into the Register file, and then DES must be executed 16 times to encrypt/decrypt the data block.

The AES Crypto Module encrypts and decrypts 128-bit data blocks with the use of a 128-bit key. The key and data must be loaded into the key and state memory in the module before encryption/decryption is started. It takes 375 peripheral clock cycles before the encryption/decryption is done and decrypted/encrypted data can be read out, and an optional interrupt can be generated. The AES Crypto Module also has DMA support with transfer triggers when encryption/decryption is done and optional auto-start of encryption/decryption when the state memory is fully loaded.

25. ADC - 12-bit Analog to Digital Converter

25.1 Features

- Two ADCs with 12-bit resolution
- 2 Msps sample rate for each ADC
- Signed and Unsigned conversions
- 4 result registers with individual input channel control for each ADC
- 8 single ended inputs for each ADC
- 8x4 differential inputs for each ADC
- 4 internal inputs:
 - Integrated Temperature Sensor
 - DAC Output
 - VCC voltage divided by 10
 - Bandgap voltage
- Software selectable gain of 2, 4, 8, 16, 32 or 64
- Software selectable resolution of 8- or 12-bit.
- Internal or External Reference selection
- Event triggered conversion for accurate timing
- DMA transfer of conversion results
- Interrupt/Event on compare result

25.2 Overview

XMEGA A3B devices have two Analog to Digital Converters (ADC), see [Figure 25-1 on page 43](#). The two ADC modules can be operated simultaneously, individually or synchronized.

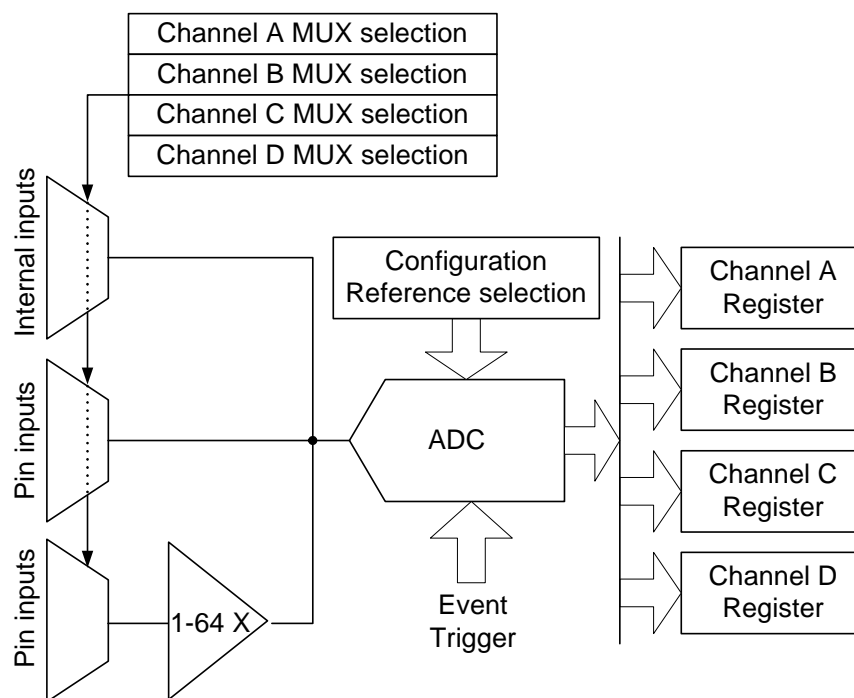
The ADC converts analog voltages to digital values. The ADC has 12-bit resolution and is capable of converting up to 2 million samples per second. The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements an optional gain stage is available to increase the dynamic range. In addition several internal signal inputs are available. The ADC can provide both signed and unsigned results.

This is a pipeline ADC. A pipeline ADC consists of several consecutive stages, where each stage convert one part of the result. The pipeline design enables high sample rate at low clock speeds, and remove limitations on samples speed versus propagation delay. This also means that a new analog voltage can be sampled and a new ADC measurement started while other ADC measurements are ongoing.

ADC measurements can either be started by application software or an incoming event from another peripheral in the device. Four different result registers with individual input selection (MUX selection) are provided to make it easier for the application to keep track of the data. Each result register and MUX selection pair is referred to as an ADC Channel. It is possible to use DMA to move ADC results directly to memory or peripherals when conversions are done.

Both internal and external analog reference voltages can be used. An accurate internal 1.0V reference is available.

An integrated temperature sensor is available and the output from this can be measured with the ADC. The output from the DAC, VCC/10 and the Bandgap voltage can also be measured by the ADC.

Figure 25-1. ADC overview

Each ADC has four MUX selection registers with a corresponding result register. This means that four channels can be sampled within 1.5 μ s without any intervention by the application other than starting the conversion. The results will be available in the result registers.

The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.5 μ s for 12-bit to 2.5 μ s for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional '1' or '0' padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA and PORTB each have one ADC. Notation of these peripherals are ADCA and ADCB, respectively.

26. DAC - 12-bit Digital to Analog Converter

26.1 Features

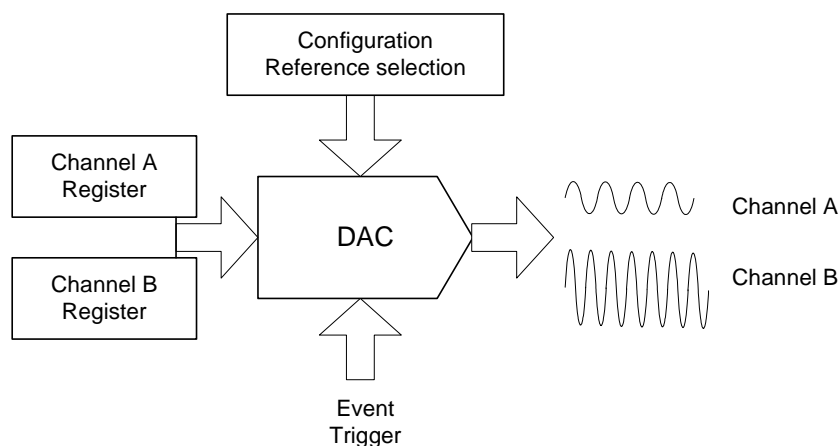
- One DAC with 12-bit resolution
- Up to 1 Msps conversion rate for each DAC
- Flexible conversion range
- Multiple trigger sources
- 1 continuous output or 2 Sample and Hold (S/H) outputs for each DAC
- Built-in offset and gain calibration
- High drive capabilities
- Low Power Mode

26.2 Overview

The XMEGA A3B devices features two 12-bit, 1 Msps DACs with built-in offset and gain calibration, see [Figure 26-1 on page 44](#).

A DAC converts a digital value into an analog signal. The DAC may use an internal 1.1 voltage as the upper limit for conversion, but it is also possible to use the supply voltage or any applied voltage in-between. The external reference input is shared with the ADC reference input.

Figure 26-1. DAC overview



Each DAC has one continuous output with high drive capabilities for both resistive and capacitive loads. It is also possible to split the continuous time channel into two Sample and Hold (S/H) channels, each with separate data conversion registers.

A DAC conversion may be started from the application software by writing the data conversion registers. The DAC can also be configured to do conversions triggered by the Event System to have regular timing, independent of the application software. DMA may be used for transferring data from memory locations to DAC data registers.

The DAC has a built-in calibration system to reduce offset and gain error when loading with a calibration value from software.

PORTB has one DAC. Notation of this is DACB.

27. AC - Analog Comparator

27.1 Features

- Four Analog Comparators
- Selectable Power vs. Speed
- Selectable hysteresis
 - 0, 20 mV, 50 mV
- Analog Comparator output available on pin
- Flexible Input Selection
 - All pins on the port
 - Output from the DAC
 - Bandgap reference voltage.
 - Voltage scaler that can perform a 64-level scaling of the internal VCC voltage.
- Interrupt and event generation on
 - Rising edge
 - Falling edge
 - Toggle
- Window function interrupt and event generation on
 - Signal above window
 - Signal inside window
 - Signal below window

27.2 Overview

XMEGA A3B features four Analog Comparators (AC). An Analog Comparator compares two voltages, and the output indicates which input is largest. The Analog Comparator may be configured to give interrupt requests and/or events upon several different combinations of input change.

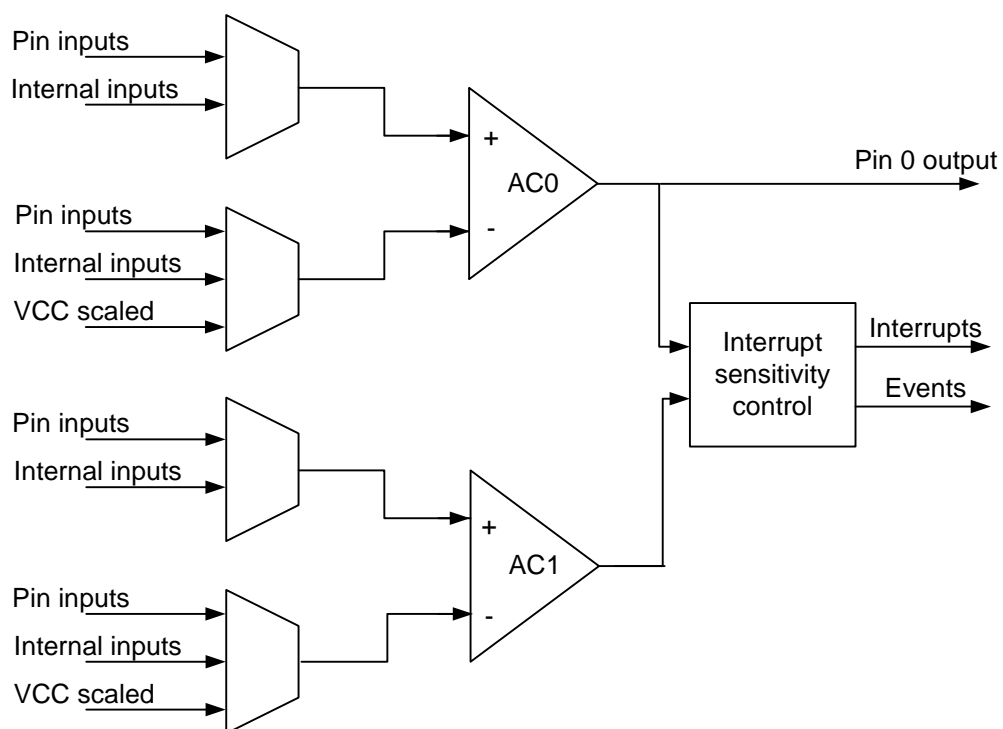
Both hysteresis and propagation delays may be adjusted in order to find the optimal operation for each application.

A wide range of input selection is available, both external pins and several internal signals can be used.

The Analog Comparators are always grouped in pairs (AC0 and AC1) on each analog port. They have identical behavior but separate control registers.

Optionally, the state of the comparator is directly available on a pin.

PORTA and PORTB each have one AC pair. Notations are ACA and ACB, respectively.

Figure 27-1. Analog comparator overview

27.3 Input Selection

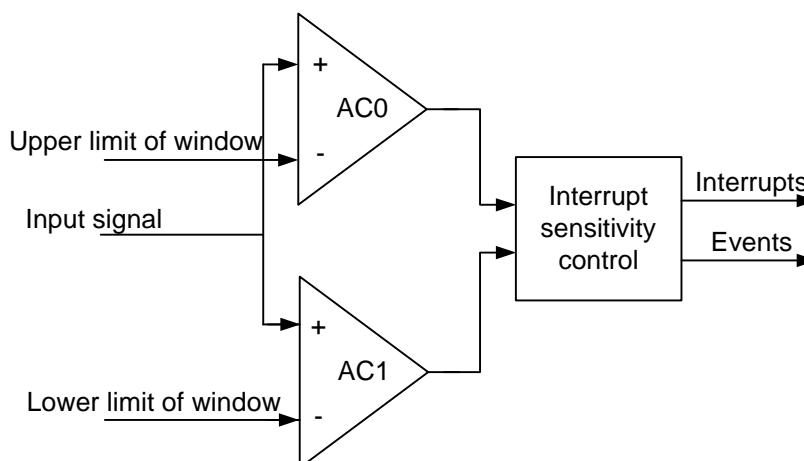
The Analog comparators have a very flexible input selection and the two comparators grouped in a pair may be used to realize a window function. One pair of analog comparators is shown in [Figure 27-1 on page 46](#).

- Input selection from pin
 - Pin 0, 1, 2, 3, 4, 5, 6 selectable to positive input of analog comparator
 - Pin 0, 1, 3, 5, 7 selectable to negative input of analog comparator
- Internal signals available on positive analog comparator inputs
 - Output from 12-bit DAC
- Internal signals available on negative analog comparator inputs
 - 64-level scaler of the VCC, available on negative analog comparator input
 - Bandgap voltage reference
 - Output from 12-bit DAC

27.4 Window Function

The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in [Figure 27-2](#).

Figure 27-2. Analog comparator window function



28. OCD - On-chip Debug

28.1 Features

- Complete Program Flow Control
 - Go, Stop, Reset, Step into, Step over, Step out, Run-to-Cursor
- Debugging on C and high-level language source code level
- Debugging on Assembler and disassembler level
- 1 dedicated program address or source level breakpoint for AVR Studio / debugger
- 4 Hardware Breakpoints
- Unlimited Number of User Program Breakpoints
- Unlimited Number of User Data Breakpoints, with break on:
 - Data location read, write or both read and write
 - Data location content equal or not equal to a value
 - Data location content is greater or less than a value
 - Data location content is within or outside a range
 - Bits of a data location are equal or not equal to a value
- Non-Intrusive Operation
 - No hardware or software resources in the device are used
- High Speed Operation
 - No limitation on debug/programming clock frequency versus system clock frequency

28.2 Overview

The XMEGA A3B has a powerful On-Chip Debug (OCD) system that - in combination with Atmel's development tools - provides all the necessary functions to debug an application. It has support for program and data breakpoints, and can debug an application from C and high level language source code level, as well as assembler and disassembler level. It has full Non-Intrusive Operation and no hardware or software resources in the device are used. The ODC system is accessed through an external debugging tool which connects to the JTAG or PDI physical interfaces. Refer to ["Program and Debug Interfaces" on page 49](#).

29. Program and Debug Interfaces

29.1 Features

- **PDI - Program and Debug Interface (Atmel proprietary 2-pin interface)**
- **JTAG Interface (IEEE std. 1149.1 compliant)**
- **Boundary-scan capabilities according to the IEEE Std. 1149.1 (JTAG)**
- **Access to the OCD system**
- **Programming of Flash, EEPROM, Fuses and Lock Bits**

29.2 Overview

The programming and debug facilities are accessed through the JTAG and PDI physical interfaces. The PDI physical uses one dedicated pin together with the Reset pin, and no general purpose pins are used. JTAG uses four general purpose pins on PORTB.

29.3 JTAG interface

The JTAG physical layer handles the basic low-level serial communication over four I/O lines named TMS, TCK, TDI, and TDO. It complies to the IEEE Std. 1149.1 for test access port and boundary scan.

29.4 PDI - Program and Debug Interface

The PDI is an Atmel proprietary protocol for communication between the microcontroller and Atmel's development tools.

30. Pinout and Pin Functions

The pinout of XMEGA A3B is shown in ["Pinout/Block Diagram" on page 2](#). In addition to general I/O functionality, each pin may have several functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the alternate pin functions can be used at time.

30.1 Alternate Pin Function Description

The tables below shows the notation for all pin functions available and describes its function.

30.1.1 Operation/Power Supply

VCC	Digital supply voltage
AVCC	Analog supply voltage
VBAT	Battery Backup Module supply voltage
GND	Ground

30.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

30.1.3 Analog functions

ACn	Analog Comparator input pin n
AC0OUT	Analog Comparator 0 Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
AREF	Analog Reference input pin

30.1.4 Timer/Counter and AWEX functions

OCnx	Output Compare Channel x for Timer/Counter n
$\overline{\text{OCxn}}$	Inverted Output Compare Channel x for Timer/Counter n

30.1.5 Communication functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled
SDAIN	Serial Data In for TWI when external driver interface is enabled
SDAOUT	Serial Data Out for TWI when external driver interface is enabled

XCKn	Transfer Clock for USART n
RxDn	Receiver Data for USART n
TxDn	Transmitter Data for USART n
\overline{SS}	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI

30.1.6 Oscillators, Clock and Event

TOSCn	Timer Oscillator pin n
XTALn	Input/Output for inverting Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel 0 Output

30.1.7 Debug/System functions

\overline{RESET}	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin
TCK	JTAG Test Clock
TDI	JTAG Test Data In
TDO	JTAG Test Data Out
TMS	JTAG Test Mode Select

30.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

Table 30-1. Port A - Alternate functions

PORT A	PIN #	INTERRUPT	ADCA POS	ADCA NEG	ADCA GAINPOS	ADCA GAINNEG	ACA POS	ACA NEG	ACA OUT	REFA
GND	60									
AVCC	61									
PA0	62	SYNC	ADC0	ADC0	ADC0		AC0	AC0		AREF
PA1	63	SYNC	ADC1	ADC1	ADC1		AC1	AC1		
PA2	64	SYNC/ASYNC	ADC2	ADC2	ADC2		AC2			
PA3	1	SYNC	ADC3	ADC3	ADC3		AC3	AC3		
PA4	2	SYNC	ADC4		ADC4	ADC4	AC4			
PA5	3	SYNC	ADC5		ADC5	ADC5	AC5	AC5		
PA6	4	SYNC	ADC6		ADC6	ADC6	AC6			
PA7	5	SYNC	ADC7		ADC7	ADC7		AC7	AC0OUT	

Table 30-2. Port B - Alternate functions

PORT B	PIN #	INTERRUPT	ADCB POS	ADCB NEG	ADCB GAINPOS	ADCB GAINNEG	ACB POS	ACB NEG	ACB OUT	DACB	REFB	JTAG
PB0	6	SYNC	ADC0	ADC0	ADC0		AC0	AC0			AREF	
PB1	7	SYNC	ADC1	ADC1	ADC1		AC1	AC1				
PB2	8	SYNC/ASYNC	ADC2	ADC2	ADC2		AC2			DAC0		
PB3	9	SYNC	ADC3	ADC3	ADC3		AC3	AC3		DAC1		
PB4	10	SYNC	ADC4		ADC4	ADC4	AC4					TMS
PB5	11	SYNC	ADC5		ADC5	ADC5	AC5	AC5				TDI
PB6	12	SYNC	ADC6		ADC6	ADC6	AC6					TCK
PB7	13	SYNC	ADC7		ADC7	ADC7		AC7	AC0OUT			TDO

Table 30-3. Port C - Alternate functions

PORT C	PIN #	INTERRUPT	TCC0	AWEXC	TCC1	USARTC0	USARTC1	SPIC	TWIC	CLOCKOUT	EVENTOUT
GND	14										
AVCC	15										
PC0	16	SYNC	OC0A	OC0A					SDA/SDA_IN		
PC1	17	SYNC	OC0B	OC0A		XCK0			SCL/SCL_IN		
PC2	18	SYNC/ASYNC	OC0C	OC0B		RXD0			SDA_OUT		
PC3	19	SYNC	OC0D	OC0B		TXD0			SCL_OUT		
PC4	20	SYNC		OC0C	OC1A			SS			
PC5	21	SYNC		OC0C	OC1B		XCK1	MOSI			
PC6	22	SYNC		OC0D			RXD1	MISO			
PC7	23	SYNC		OC0D			TXD1	SCK		CLKOUT	EVOUT

Table 30-4. Port D - Alternate functions

PORT D	PIN #	INTERRUPT	TCD0	TCD1	USARTD0	USARTD1	SPID	CLOCKOUT	EVENTOUT
GND	24								
VCC	25								
PD0	26	SYNC	OC0A						
PD1	27	SYNC	OC0B		XCK0				
PD2	28	SYNC/ASYNC	OC0C		RXD0				
PD3	29	SYNC	OC0D		TXD0				
PD4	30	SYNC		OC1A			\overline{SS}		
PD5	31	SYNC		OC1B		XCK1	MOSI		
PD6	32	SYNC				RXD1	MISO		
PD7	33	SYNC				TXD1	SCK	CLKOUT	EVOUT

Table 30-5. Port E - Alternate functions

PORT E	PIN #	INTERRUPT	TCE0	TCE1	USARTE0	TWIE
GND	34					
VCC	35					
PE0	36	SYNC	OC0A			SDA/SDA_IN
PE1	37	SYNC	OC0B		XCK0	SCL/SCL_IN
PE2	38	SYNC/ASYNC	OC0C		RXD0	SDA_OUT
PE3	39	SYNC	OC0D		TXD0	SCL_OUT
PE4	40	SYNC		OC1A		
PE5	41	SYNC		OC1B		
TOSC2	42					
TOSC1	43					

Table 30-6. Port F - Alternate functions

PORT F	PIN #	INTERRUPT	TCF0	USARTF0
GND	44			
VCC	45			
PF0	46	SYNC	OC0A	
PF1	47	SYNC	OC0B	XCK0
PF2	48	SYNC/ASYNC	OC0C	RXD0
PF3	49	SYNC	OC0D	TXD0
PF4	50	SYNC	OC0A	
VBAT	51			
GND	52	SYNC		
VCC	53	SYNC		
PF6	54			
PF7	55			

Table 30-7. Port R- Alternate functions

PORT R	PIN #	INTERRUPT	PDI	XTAL
PDI	56		PDI_DATA	
RESET	57		PDI_CLK	
PRO	58	SYNC		XTAL2
PR1	59	SYNC		XTAL1

31. Peripheral Module Address Map

The address maps show the base address for each peripheral and module in XMEGA A3B. For complete register description and summary for each peripheral module, refer to the XMEGA A Manual.

Base Address	Name	Description
0x0000	GPIO	General Purpose IO Registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock Control
0x0048	SLEEP	Sleep Controller
0x0050	OSC	Oscillator Control
0x0060	DFLLRC32M	DFLL for the 32 MHz Internal RC Oscillator
0x0068	DFLLRC2M	DFLL for the 2 MHz RC Oscillator
0x0070	PR	Power Reduction
0x0078	RST	Reset Controller
0x0080	WDT	Watch-Dog Timer
0x0090	MCU	MCU Control
0x00A0	PMIC	Programmable Multilevel Interrupt Controller
0x00B0	PORTCFG	Port Configuration
0x00C0	AES	AES Module
0x00F0	VBAT	VBAT Battery Backup Module
0x0100	DMA	DMA Controller
0x0180	EVSYS	Event System
0x01C0	NVM	Non Volatile Memory (NVM) Controller
0x0200	ADCA	Analog to Digital Converter on port A
0x0240	ADCB	Analog to Digital Converter on port B
0x0320	DACB	Digital to Analog Converter on port B
0x0380	ACA	Analog Comparator pair on port A
0x0390	ACB	Analog Comparator pair on port B
0x0420	RTC32	32-bit Real Time Counter
0x0480	TWIC	Two Wire Interface on port C
0x04A0	TWIE	Two Wire Interface on port E
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C
0x0660	PORTD	Port D
0x0680	PORTE	Port E
0x06A0	PORTF	Port F
0x07E0	PORTR	Port R
0x0800	TCC0	Timer/Counter 0 on port C
0x0840	TCC1	Timer/Counter 1 on port C
0x0880	AWEXC	Advanced Waveform Extension on port C
0x0890	HIRES	High Resolution Extension on port C
0x08A0	USARTC0	USART 0 on port C
0x08B0	USARTC1	USART 1 on port C
0x08C0	SPIC	Serial Peripheral Interface on port C
0x08F8	IRCOM	Infrared Communication Module
0x0900	TCD0	Timer/Counter 0 on port D
0x0940	TCD1	Timer/Counter 1 on port D
0x0990	HIRES	High Resolution Extension on port D
0x09A0	USARTD0	USART 0 on port D
0x09B0	USARTD1	USART 1 on port D
0x09C0	SPID	Serial Peripheral Interface on port D
0x0A00	TCE0	Timer/Counter 0 on port E
0x0A40	TCE1	Timer/Counter 1 on port E
0x0A80	AWEXE	Advanced Waveform Extension on port E
0x0A90	HIRES	High Resolution Extension on port E
0x0AA0	USARTE0	USART 0 on port E
0x0B00	TCF0	Timer/Counter 0 on port F
0x0B90	HIRES	High Resolution Extension on port F
0x0BA0	USARTF0	USART 0 on port F

32. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	$Rd \leftarrow Rd + Rr$	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	$Rd \leftarrow Rd + 1:Rd + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	$Rd \leftarrow Rd - Rr$	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	$Rd \leftarrow Rd - K$	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	$Rd \leftarrow Rd - K - C$	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	$Rd + 1:Rd \leftarrow Rd + 1:Rd - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	$Rd \leftarrow Rd \bullet Rr$	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	$Rd \leftarrow Rd \bullet K$	Z,N,V,S	1
OR	Rd, Rr	Logical OR	$Rd \leftarrow Rd \vee Rr$	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	$Rd \leftarrow Rd \oplus Rr$	Z,N,V,S	1
COM	Rd	One's Complement	$Rd \leftarrow \$FF - Rd$	Z,C,N,V,S	1
NEG	Rd	Two's Complement	$Rd \leftarrow \$00 - Rd$	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (\$FFh - K)$	Z,N,V,S	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V,S	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V,S	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V,S	1
SER	Rd	Set Register	$Rd \leftarrow \$FF$	None	1
MUL	Rd,Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr (UU)$	Z,C	2
MULS	Rd,Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr (SS)$	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr (SU)$	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr << 1 (UU)$	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	$R1:R0 \leftarrow Rd \times Rr << 1 (SS)$	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr << 1 (SU)$	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 \leftarrow Encrypt(R15:R0, K) else if (H = 1) then R15:R0 \leftarrow Decrypt(R15:R0, K)		1/2
Branch Instructions					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow 0$	None	2
EIJMP		Extended Indirect Jump to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow EIND$	None	2
JMP	k	Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Call Subroutine	$PC \leftarrow PC + k + 1$	None	2 / 3 ⁽¹⁾
ICALL		Indirect Call to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow 0$	None	2 / 3 ⁽¹⁾
EICALL		Extended Indirect Call to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow EIND$	None	3 ⁽¹⁾

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CALL	k	call Subroutine	$PC \leftarrow k$	None	3 / 4 ⁽¹⁾
RET		Subroutine Return	$PC \leftarrow STACK$	None	4 / 5 ⁽¹⁾
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4 / 5 ⁽¹⁾
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) $PC \leftarrow PC + 2$ or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	$Rd - Rr$	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	$Rd - K$	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) $PC \leftarrow PC + 2$ or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) $PC \leftarrow PC + 2$ or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) $PC \leftarrow PC + 2$ or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) = 1) $PC \leftarrow PC + 2$ or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if ($N \oplus V = 0$) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if ($N \oplus V = 1$) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then $PC \leftarrow PC + k + 1$	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then $PC \leftarrow PC + k + 1$	None	1 / 2
Data Transfer Instructions					
MOV	Rd, Rr	Copy Register	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Pair	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LDS	Rd, k	Load Direct from data space	$Rd \leftarrow (k)$	None	2 ⁽¹⁾⁽²⁾
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	1 ⁽¹⁾⁽²⁾
LD	Rd, X+	Load Indirect and Post-Increment	$Rd \leftarrow (X)$ $X \leftarrow X + 1$	None	1 ⁽¹⁾⁽²⁾
LD	Rd, -X	Load Indirect and Pre-Decrement	$X \leftarrow X - 1$ $Rd \leftarrow (X)$	None	2 ⁽¹⁾⁽²⁾
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	1 ⁽¹⁾⁽²⁾
LD	Rd, Y+	Load Indirect and Post-Increment	$Rd \leftarrow (Y)$ $Y \leftarrow Y + 1$	None	1 ⁽¹⁾⁽²⁾

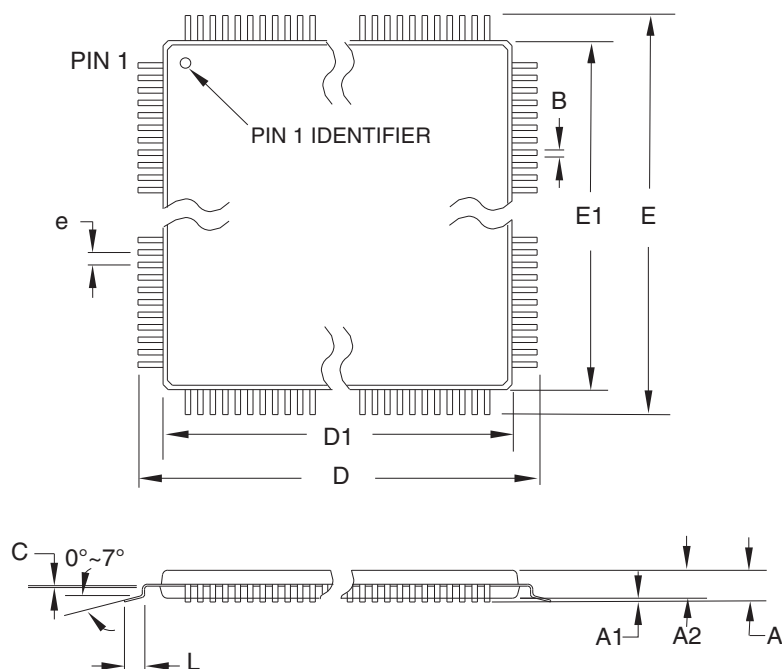
Mnemonics	Operands	Description	Operation	Flags	#Clocks
LD	Rd, -Y	Load Indirect and Pre-Decrement	$Y \leftarrow Y - 1$ $Rd \leftarrow (Y)$	None	2 ⁽¹⁾⁽²⁾
LDD	Rd, Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2 ⁽¹⁾⁽²⁾
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	1 ⁽¹⁾⁽²⁾
LD	Rd, Z+	Load Indirect and Post-Increment	$Rd \leftarrow (Z)$, $Z \leftarrow Z + 1$	None	1 ⁽¹⁾⁽²⁾
LD	Rd, -Z	Load Indirect and Pre-Decrement	$Z \leftarrow Z - 1$, $Rd \leftarrow (Z)$	None	2 ⁽¹⁾⁽²⁾
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2 ⁽¹⁾⁽²⁾
STS	k, Rr	Store Direct to Data Space	$(k) \leftarrow Rr$	None	2 ⁽¹⁾
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	1 ⁽¹⁾
ST	X+, Rr	Store Indirect and Post-Increment	$(X) \leftarrow Rr$, $X \leftarrow X + 1$	None	1 ⁽¹⁾
ST	-X, Rr	Store Indirect and Pre-Decrement	$X \leftarrow X - 1$, $(X) \leftarrow Rr$	None	2 ⁽¹⁾
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	1 ⁽¹⁾
ST	Y+, Rr	Store Indirect and Post-Increment	$(Y) \leftarrow Rr$, $Y \leftarrow Y + 1$	None	1 ⁽¹⁾
ST	-Y, Rr	Store Indirect and Pre-Decrement	$Y \leftarrow Y - 1$, $(Y) \leftarrow Rr$	None	2 ⁽¹⁾
STD	Y+q, Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2 ⁽¹⁾
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	1 ⁽¹⁾
ST	Z+, Rr	Store Indirect and Post-Increment	$(Z) \leftarrow Rr$, $Z \leftarrow Z + 1$	None	1 ⁽¹⁾
ST	-Z, Rr	Store Indirect and Pre-Decrement	$Z \leftarrow Z - 1$	None	2 ⁽¹⁾
STD	Z+q, Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2 ⁽¹⁾
LPM		Load Program Memory	$R0 \leftarrow (Z)$	None	3
LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	$Rd \leftarrow (Z)$, $Z \leftarrow Z + 1$	None	3
ELPM		Extended Load Program Memory	$R0 \leftarrow (RAMPZ:Z)$	None	3
ELPM	Rd, Z	Extended Load Program Memory	$Rd \leftarrow (RAMPZ:Z)$	None	3
ELPM	Rd, Z+	Extended Load Program Memory and Post-Increment	$Rd \leftarrow (RAMPZ:Z)$, $Z \leftarrow Z + 1$	None	3
SPM		Store Program Memory	$(RAMPZ:Z) \leftarrow R1:R0$	None	-
SPM	Z+	Store Program Memory and Post-Increment by 2	$(RAMPZ:Z) \leftarrow R1:R0$, $Z \leftarrow Z + 2$	None	-
IN	Rd, A	In From I/O Location	$Rd \leftarrow I/O(A)$	None	1
OUT	A, Rr	Out To I/O Location	$I/O(A) \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	1 ⁽¹⁾
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2 ⁽¹⁾
Bit and Bit-test Instructions					
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n)$, $Rd(0) \leftarrow 0$, $C \leftarrow Rd(7)$	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1)$, $Rd(7) \leftarrow 0$, $C \leftarrow Rd(0)$	Z,C,N,V	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C,$ $Rd(n+1) \leftarrow Rd(n),$ $C \leftarrow Rd(7)$	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C,$ $Rd(n) \leftarrow Rd(n+1),$ $C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftrightarrow Rd(7..4)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	$I/O(A, b) \leftarrow 1$	None	1
CBI	A, b	Clear Bit in I/O Register	$I/O(A, b) \leftarrow 0$	None	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Two's Complement Overflow	$V \leftarrow 1$	V	1
CLV		Clear Two's Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half Carry Flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear Half Carry Flag in SREG	$H \leftarrow 0$	H	1
MCU Control Instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

- Notes:
1. Cycle times for Data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.
 2. One extra cycle must be added when accessing Internal SRAM.

33. Packaging information

33.1 64A



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.30	—	0.45	
C	0.09	—	0.20	
L	0.45	—	0.75	
e	0.80 TYP			

Notes:

1. This package conforms to JEDEC reference MS-026, Variation AEB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001



2325 Orchard Parkway
San Jose, CA 95131

TITLE

64A, 64-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness,
0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

DRAWING NO.

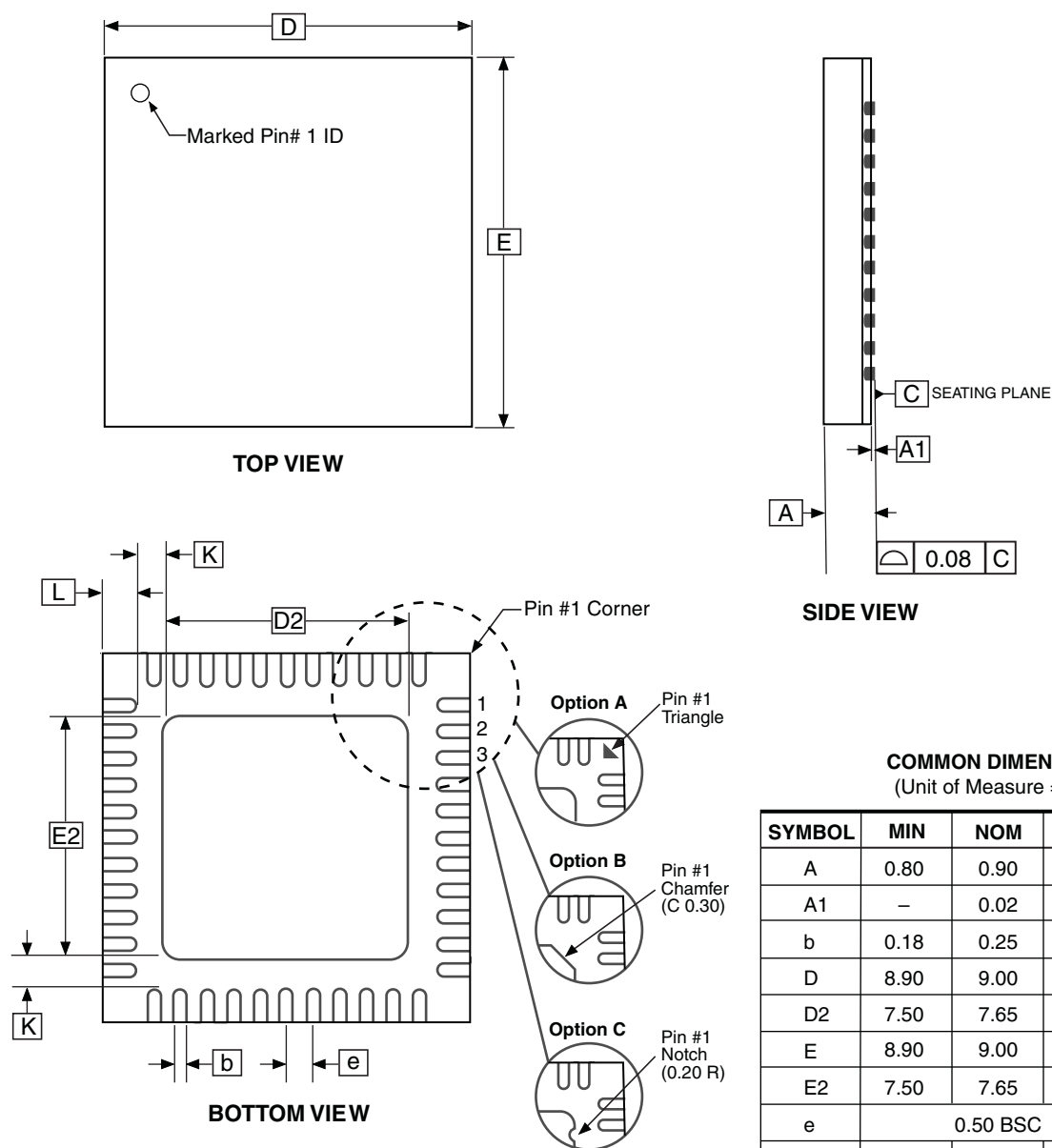
64A

REV.

B



33.2 64M2



Note: 1. JEDEC Standard MO-220, (SAW Singulation) Fig. 1, VMMD.
2. Dimension and tolerance conform to ASMEY14.5M-1994.

5/25/06



2325 Orchard Parkway
San Jose, CA 95131

TITLE

64M2, 64-pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm,
7.65 mm Exposed Pad, Micro Lead Frame Package (MLF)

DRAWING NO.

64M2

REV.

D



34. Electrical Characteristics - TBD

34.1 Absolute Maximum Ratings*

Operating Temperature.....	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with respect to Ground..	-0.5V to $V_{CC}+0.5V$
Maximum Operating Voltage	3.6V
DC Current per I/O Pin	20.0 mA
DC Current V_{CC} and GND Pins.....	200.0 mA

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

34.2 DC Characteristics

$T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 1.8V$ to $3.6V$ (unless otherwise noted)

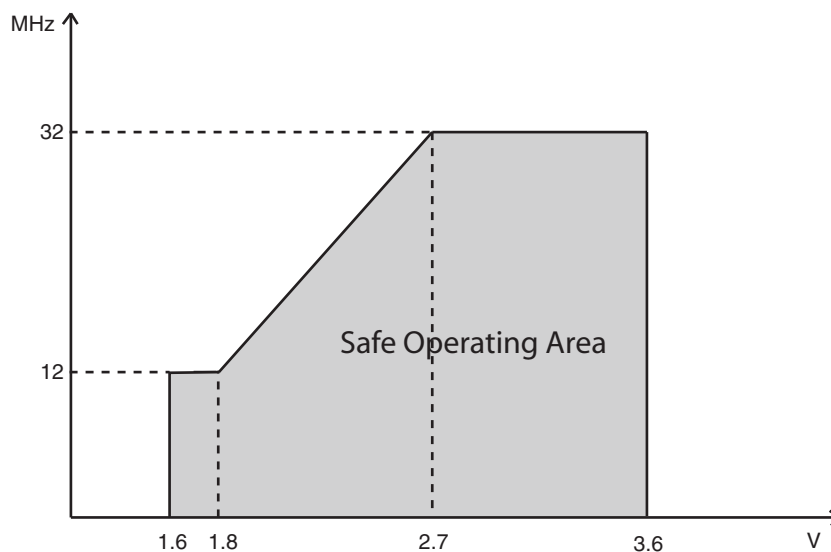
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage, except XTAL1 pin					V
V_{IL1}	Input Low Voltage, XTAL1 pins					V
V_{IH}	Input High Voltage, except XTAL1 pin					V
V_{IH1}	Input High Voltage, XTAL1 pin					V
V_{OL}	Output Low Voltage					
V_{OH}	Output High Voltage					
I_{IL}	Input Leakage Current I/O Pin					μA
I_{IH}	Input Leakage Current I/O Pin					μA
R_{RST}	Reset Pull-up Resistor					$k\Omega$
R_{PU}	I/O Pin Pull-up Resistor					$k\Omega$
I_{CC}	Power Supply Current	Active 32 MHz				mA
		Active 20 MHz				mA
		Active 8MHz				mA
		Idle 32 MHz				mA
		Idle 20 MHz				mA
	Power-down mode	WDT disabled				μA
		WDT slow sampling				μA
		WDT fast sampling				

Note: 1. “Max” means the highest value where the pin is guaranteed to be read as low
2. “Min” means the lowest value where the pin is guaranteed to be read as high

34.3 Speed

The maximum frequency of the XMEGA A3B devices is depending on V_{CC} . As shown in [Figure 34-1 on page 63](#) the Frequency vs. V_{CC} curve is linear between $1.8V < V_{CC} < 2.7V$.

Figure 34-1. Maximum Frequency vs. V_{CC}



34.4 ADC Characteristics – TBD

Table 34-1. ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution					LSB
	Integral Non-Linearity (INL)					LSB
	Differential Non-Linearity (DNL)					LSB
	Gain Error					LSB
	Offset Error					LSB
	Conversion Time					μs
	ADC Clock Frequency					MHz
	DC Supply Voltage					mA
	Source Impedance					Ω
	Start-up time					μs
AVCC	Analog Supply Voltage		$V_{CC} - 0.3$		$V_{CC} + 0.3$	V

Table 34-2. ADC Gain Stage Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Gain					
	Input Capacitance					pF
	Offset Error					mV
	Gain Error					%
	Signal Range					V
	DC Supply Current					mA
	Start-up time					# clk cycles

34.5 DAC Characteristics – TBD

Table 34-3. DAC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution					LSB
	Integral Non-Linearity (INL)					LSB
	Differential Non-Linearity (DNL)					LSB
	Gain Error					LSB
	Offset Error					LSB
	Calibrated Gain/Offset Error					LSB
	Output Range					V
	Output Settling Time					μs
	Output Capacitance					nF
	Output Resistance					kΩ
	Reference Input Voltage					V
	Reference Input Capacitance					pF
	Reference Input Resistance					kΩ
	Current Consumption					mA
	Start-up time					μs

34.6 Analog Comparator Characteristics – TBD

Table 34-4. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Offset					mV
	Hysteresis	No				mV
		Low				
		High				
	Propagation Delay	High Speed mode				ns
		Low power mode				
	Current Consumption	High Speed mode				μA
		Low power mode				
	Start-up time					μs

35. Typical Characteristics - TBD

36. Errata

36.1 ATxmega256A3B

36.1.1 rev. A

- Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously
- DAC is nonlinear and inaccurate if the external reference is above 2.4V or $V_{CC} - 0.6V$
- ADC gain stage output range is limited to 2.4V
- Sampled BOD in Active mode will cause noise when bandgap is used as reference
- Flash Power Reduction Mode can not be enabled when entering sleep mode
- JTAG enable does not override Analog Comparator B output
- Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V
- DAC refresh may be blocked in S/H mode
- BOD will be enabled after any reset
- Both DFLLs and both oscillators has to be enabled for one to work
- Operating frequency and voltage limitations

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for the another AC, the first comparator will be affected for up to 1 us and could potentially give a wrong comparison result.

Problem fix/Workaround

If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. DAC is nonlinear and inaccurate if the external reference is above 2.4V or $V_{CC}-0.6V$

Using the DAC with a reference voltage above 2.4V or $V_{CC}-0.6V$ give inaccurate output in the top 25% of the output range:

- ± 30 LSB for continuous mode
- ± 200 LSB for Sample and Hold mode

Problem fix/Workaround

None, avoid using a voltage reference above 2.4V or $V_{CC}-0.6V$.

3. ADC gain stage output range is limited to 2.4 V

The amplified output of the ADC gain stage will never go above 2.4 V, hence the differential input will only give correct output when below 2.4 V/gain. For the available gain settings, this gives a differential input range of:

- 1x gain: 2.4 V
- 2x gain: 1.2 V
- 4x gain: 0.6 V
- 8x gain: 300 mV

- 16x gain: 150 mV
- 32x gain: 75 mV
- 64x gain: 38 mV

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4 V in order to get a correct result, or keep ADC voltage reference below 2.4 V.

4. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC and Analog Comparator.

Problem fix/Workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

5. Flash Power Reduction Mode can not be enabled when entering sleep mode

If Flash Power Reduction Mode is enabled when a deep sleep mode, the device will only wake up on every fourth wake-up request.

If Flash Power Reduction Mode is enabled when entering Idle sleep mode, the wake-up time will vary with up to 16 CPU clock cycles.

Problem fix/Workaround

Disable Flash Power Reduction mode before entering sleep mode.

6. JTAG enable does not override Analog Comparator B output

When JTAG is enabled this will not override the Analog Comparator B (ACB) output, AC0OUT on pin 7 if this is enabled.

Problem fix/Workaround

AC0OUT for ACB should not be enabled when JTAG is used. Use only analog comparator output for ACA when JTAG is used, or use the PDI as debug interface.

7. Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V

The ADC cannot be used to do bandgap measurements when V_{CC} is below 2.7V.

Problem fix/Workaround

If internal voltages must be measured when V_{CC} is below 2.7V, measure the internal 1.00V reference instead of the bandgap.

8. DAC refresh may be blocked in S/H mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workaround

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

9 BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the VCC voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until VCC is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

10 Both DFLLs and both oscillators has to be enabled for one to work

In order to use the automatic runtime calibration for the 2 MHz or the 32MHz internal oscillators, the DFLL for both oscillators and both oscillators has to be enabled for one to work.

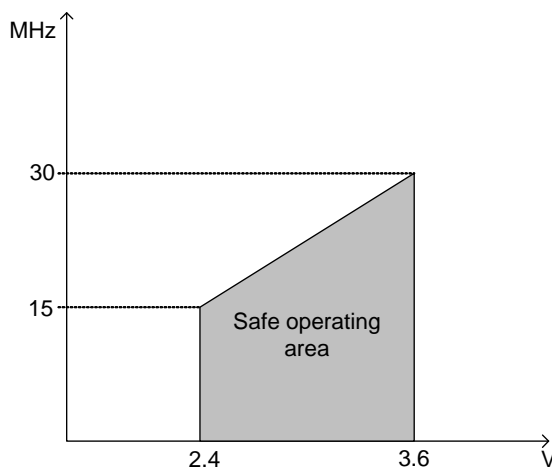
Problem fix/Workaround

Enabled both the DFLLs and both oscillators when using automatic runtime calibration for one of the internal oscillators.

11 Operating Frequency and Voltage Limitation

To ensure correct operation, there is a limit on operating frequency and voltage. [Figure 36-1 on page 69](#) shows the safe operating area.

Figure 36-1. Operating Frequency and Voltage Limitation

**Problem fix/Workaround**

None, avoid using the device outside these frequency and voltage limitations.

37. Datasheet Revision History

37.1 8116B - 12/08

1. Added "[Errata](#)" on [page 67](#) for ATxmega256A3B rev A.

37.2 8116A - 11/08

1. Initial version.

Table of Contents

	Features	1
	Typical Applications	1
1	Ordering Information	2
2	Pinout/Block Diagram	2
3	Overview	3
	3.1Block Diagram	4
4	Resources	5
	4.1Recommended reading	5
5	Disclaimer	5
6	AVR CPU	6
	6.1Features	6
	6.2Overview	6
	6.3Register File	7
	6.4ALU - Arithmetic Logic Unit	7
	6.5Program Flow	7
7	Memories	8
	7.1Features	8
	7.2Overview	8
	7.3In-System Programmable Flash Program Memory	9
	7.4Data Memory	9
	7.5Production Signature Row	11
	7.6Production Signature Row	12
	7.7User Signature Row	12
	7.8Flash and EEPROM Page Size	13
8	DMAC - Direct Memory Access Controller	14
	8.1Features	14
	8.2Overview	14
9	Event System	15
	9.1Features	15
	9.2Overview	15
10	System Clock and Clock options	17

10.1Features	17
10.2Overview	17
10.3Clock Options	18
11 Power Management and Sleep Modes	20
11.1Features	20
11.2Overview	20
11.3Sleep Modes	20
12 System Control and Reset	22
12.1Features	22
12.2Resetting the AVR	22
12.3Reset Sources	22
12.4WDT - Watchdog Timer	23
13 Battery Backup System	24
13.1Features	24
13.2Overview	24
14 PMIC - Programmable Multi-level Interrupt Controller	26
14.1Features	26
14.2Overview	26
14.3Interrupt vectors	26
15 I/O Ports	28
15.1Features	28
15.2Overview	28
15.3I/O configuration	28
15.4Input sensing	31
15.5Port Interrupt	31
15.6Alternate Port Functions	31
16 T/C - 16-bit Timer/Counter with PWM	32
16.1Features	32
16.2Overview	32
17 AWEX - Advanced Waveform Extension	34
17.1Features	34
17.2Overview	34
18 Hi-Res - High Resolution Extension	35

18.1	Features	35
18.2	Overview	35
19	<i>RTC32 - 32-bit Real-Time Counter</i>	36
19.1	Features	36
20	<i>TWI - Two Wire Interface</i>	37
20.1	Features	37
20.2	Overview	37
21	<i>SPI - Serial Peripheral Interface</i>	38
21.1	Features	38
21.2	Overview	38
22	<i>USART</i>	39
22.1	Features	39
22.2	Overview	39
23	<i>IRCOM - IR Communication Module</i>	40
23.1	Features	40
23.2	Overview	40
24	<i>Crypto Engine</i>	41
24.1	Features	41
24.2	Overview	41
25	<i>ADC - 12-bit Analog to Digital Converter</i>	42
25.1	Features	42
25.2	Overview	42
26	<i>DAC - 12-bit Digital to Analog Converter</i>	44
26.1	Features	44
26.2	Overview	44
27	<i>AC - Analog Comparator</i>	45
27.1	Features	45
27.2	Overview	45
27.3	Input Selection	47
27.4	Window Function	47
28	<i>OCD - On-chip Debug</i>	48
28.1	Features	48
28.2	Overview	48

29	<i>Program and Debug Interfaces</i>	49
29.1	Features	49
29.2	Overview	49
29.3	JTAG interface	49
29.4	PDI - Program and Debug Interface	49
30	<i>Pinout and Pin Functions</i>	50
30.1	Alternate Pin Function Description	50
30.2	Alternate Pin Functions	52
31	<i>Peripheral Module Address Map</i>	55
32	<i>Instruction Set Summary</i>	56
33	<i>Packaging information</i>	60
33.1	64A	60
33.2	64M2	61
34	<i>Electrical Characteristics - TBD</i>	62
34.1	Absolute Maximum Ratings*	62
34.2	DC Characteristics	62
34.3	Speed	63
34.4	ADC Characteristics – TBD	64
34.5	DAC Characteristics – TBD	65
34.6	Analog Comparator Characteristics – TBD	65
35	<i>Typical Characteristics - TBD</i>	66
36	<i>Errata</i>	67
36.1	ATxmega256A3B	67
37	<i>Datasheet Revision History</i>	70
37.1	18116B - 12/08	70
37.2	28116A - 11/08	70
	<i>Table of Contents</i>	<i>i</i>



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