





10/100/1000BASE-T CONTROLLER WITH INTEGRATED TRANSCEIVER

BCM5701 FEATURES

Single-chip solution for LAN on Motherboard (LOM) and network interface card (NIC) applications

- Integrated 10BASE-T/100BASE-TX/1000BASE-T transceivers
- 10/100/1000 tri-speed MAC
- Host interfaces
 - PCI v2.2, 32/64-bit, 33/66-MHz
- PCI-X v1.0, 64-bit, 133-MHz
- MII/GMII/TBI interfaces for external transceivers
- Ultra-deep, 96-KB on-chip packet buffer
- Dual high-speed RISC cores with 16-KB caches
- Programmable, in-line packet classification
- · SMBus controller
- On-chip power circuit controller and Wake on LAN power switching circuit

Performance features

- TCP, IP, UDP checksum
- TCP segmentation
- · CPU task offload
- Adaptive interrupts
- Ultra-deep, 96-KB packet buffer

Robust manageability

- PXE 2.0 remote boot
- Alert specification forum (ASF 1.0 support)
- · Wake-on LAN
- Statistics gathering (SNMP MIB II, Ethernet-like MIB, Ethernet MIB (802.3x, clause 30))
- Comprehensive diagnostic and configuration software suite
- ACPI 1.1a compliant (multiple power modes)
- · Wake on LAN

Advanced network features

- Priority queuing (802.1p Layer 2 priority encoding; support for four priority queues)
- Virtual LANs (802.1q VLAN tagging; support for up to 64 VLANs)
- Jumbo frames (9 KB)
- 802.3x flow control

Advanced server features

- Link aggregation (802.3ad, GEC/FEC, Smart Load BalancingTM (supports heterogeneous teams))
- · Heterogeneous, mixed-speed failover
- Hot-Plug PCI support

• Low-power, 0.18 μm CMOS design

- 300-pin HBGA package
- 3.3V I/Os (5V tolerant)
- JTAG

SUMMARY OF BENEFITS

- Industry's first 10/100/1000 MAC/PHY solution (power and space optimized for LOM and low profile NIC applications)
- Completely backward compatible:
 - To existing 10/100 network infrastructure
 - To existing PCI-based desktop and server platforms
- Futureproof
 - PCI-X interface, on-chip programmable CPUs, ASF support
- Performance focused (optimized for throughput and CPU utilization)
 - Adaptive interrupts
 - PCI-X eliminates PCI bottlenecks
 - Ultra-deep, 96-KB packet buffer lowers CPU utilization and averts PCI congestion
 - · CPU task offloads

Robust and highly manageable

- PXE 2.0, ACPI 1.1, Wake-on LAN, ASF 1.0
- Integrated cable testing (link quality, length, pair skew, pair polarity, pair swap)

Advanced features

- VLAN, priority queuing, jumbo frames
- RISC processors for advanced packet classification
- Server-class reliability, availability and performance features
 - · Link aggregation and load balancing
 - Switch dependent
 - 802.3ad (LACP), generic trunking (GEC/FEC)
 - Switch and NIC independent
 - Smart Load BalancingTM (unique technology that supports heterogeneous teams, and can operate with any switch)
 - Failover
 - Smart Load BalancingTM allows heterogeneous failover
 - Hot Plug PCI support

Low power for zero airflow implementations

- 0.18 µm CMOS design
- · Advanced Power Management

Space savings for LOM

- 300-pin HBGA package
- · No external memory
- Integrated power circuitry