

High-performance Regulator IC Series for PCs

# Ultra Low Dropout Linear Regulators for PC Chipsets with Power Good

## BD3512MUV (3A)



### ● Description

The BD3512MUV ultra low-dropout linear chipset regulator operates from a very low input supply, and offers ideal performance in low input voltage to low output voltage applications. It incorporates a built-in N-MOSFET power transistor to minimize the input-to-output voltage differential to the ON resistance ( $R_{ON}=100m\Omega$ ) level. By lowering the dropout voltage in this way, the regulator realizes high current output ( $I_{Omax}=3.0A$ ) with reduced conversion loss, and thereby obviates the switching regulator and its power transistor, choke coil, and rectifier diode. Thus, the BD3512MUV is designed to enable significant package profile downsizing and cost reduction. An external resistor allows the entire range of output voltage configurations between 0.65 and 2.7V, while the NRCS (soft start) function enables a controlled output voltage ramp-up, which can be programmed to whatever power supply sequence is required.

### ● Features

- 1) Internal high-precision reference voltage circuit ( $0.65V\pm1\%$ )
- 2) Built-in VCC undervoltage lockout circuit ( $VCC=3.80V$ )
- 3) NRCS (soft start) function reduces the magnitude of in-rush current
- 4) Internal Nch MOSFET driver offers low ON resistance ( $65m\Omega$  typ)
- 5) Built-in current limit circuit (3.0A min)
- 6) Built-in thermal shutdown (TSD) circuit (Timer latch)
- 7) Variable output (0.65~2.7V)
- 8) High-power package VQFN020V4040 :  $4.0\times4.0\times1.0(mm)$
- 9) Tracking function

### ● Applications

Notebook computers, Desktop computers, LCD-TV, DVD, Digital appliances

●Absolute maximum ratings (Ta=25°C)

| Parameter                    | Symbol             | Limit              | Unit |
|------------------------------|--------------------|--------------------|------|
| Input Voltage 1              | VCC                | 6.0 <sup>*1</sup>  | V    |
| Input Voltage 2              | VIN                | 6.0 <sup>*1</sup>  | V    |
| Input Voltage 3              | VCC                | 6.0 <sup>*1</sup>  | V    |
| Input Voltage 4              | VD                 | 1                  | V    |
| Maximum Output Current       | IO                 | 3 <sup>*1</sup>    | A    |
| Enable Input Voltage         | Ven                | 6.0                | V    |
| PGOOD Input Voltage          | V <sub>PGOOD</sub> | 6.0                | V    |
| Power Dissipation 1          | Pd1                | 0.34 <sup>*2</sup> | W    |
| Power Dissipation 2          | Pd2                | 0.70 <sup>*3</sup> | W    |
| Power Dissipation 3          | Pd3                | 1.21 <sup>*4</sup> | W    |
| Power Dissipation 4          | Pd4                | 3.56 <sup>*5</sup> | W    |
| Operating Temperature Range  | Topr               | -10~+100           | °C   |
| Storage Temperature Range    | Tstg               | -55~+125           | °C   |
| Maximum Junction Temperature | Tjmax              | +150               | °C   |

<sup>\*1</sup> Should not exceed Pd.

<sup>\*2</sup> Reduced by 2.7mW/°C for each increase in Ta ≥ 25°C (no heat sink)

<sup>\*3</sup> Reduced by 5.6mW for each increase in Ta of 1°C over 25°C. (when mounted on a board 74.2mm × 74.2mm × 1.6mm Glass-epoxy PCB.)  
:No substrate surface copper foil area.

<sup>\*4</sup> Reduced by 9.7mW for each increase in Ta of 1°C over 25°C. (when mounted on a board 74.2mm × 74.2mm × 1.6mm Glass-epoxy PCB.)  
:4 layers, substrate surface copper foil area 10.29mm<sup>2</sup>.

<sup>\*5</sup> Reduced by 28.5mW for each increase in Ta of 1°C over 25°C. (when mounted on a board 74.2mm × 74.2mm × 1.6mm Glass-epoxy PCB.)  
:4 layers, substrate surface copper foil area 5505mm<sup>2</sup>.

●Operating Voltage (Ta=25°C)

| Parameter                    | Symbol | Min. | Max.                | Unit |
|------------------------------|--------|------|---------------------|------|
| Input Voltage 1              | VCC    | 4.3  | 5.5                 | V    |
| Input Voltage 2              | VIN    | 0.7  | VCC-1 <sup>*6</sup> | V    |
| Input Voltage 3              | VCC    | 4.5  | 5.5                 | V    |
| Output Voltage Setting Range | Vo     | VFB  | 2.7                 | V    |
| Enable Input Voltage         | Ven    | -0.3 | 5.5                 | V    |

<sup>\*6</sup> VCC and VIN do not have to be implemented in the order listed.

★This product is not designed for use in radioactive environments.

●Electrical Characteristics (Unless otherwise specified, Ta=25°C, Vcc=5V, Ven=3V, VIN=1.7V, R1=3.9KΩ, R2=3.3KΩ)

| Parameter                                   | Symbol               | Limit                  |                        |                        | Unit | Condition                                               |
|---------------------------------------------|----------------------|------------------------|------------------------|------------------------|------|---------------------------------------------------------|
|                                             |                      | Min.                   | Typ.                   | Max.                   |      |                                                         |
| Bias Current                                | I <sub>cc</sub>      | -                      | 1.4                    | 2.2                    | mA   |                                                         |
| VCC Shutdown Mode Current                   | I <sub>ST</sub>      | -                      | 0                      | 10                     | μA   | V <sub>en</sub> =0V                                     |
| Maximum Output Current                      | I <sub>o</sub>       | 3.0                    | -                      | -                      | A    |                                                         |
| Output Voltage Temperature Coefficient      | T <sub>cvo</sub>     | -                      | 0.01                   | -                      | %/°C |                                                         |
| Feedback Voltage 1                          | V <sub>FB1</sub>     | 0.643                  | 0.650                  | 0.657                  | V    |                                                         |
| Feedback Voltage 2                          | V <sub>FB2</sub>     | 0.637                  | 0.650                  | 0.663                  | V    | I <sub>o</sub> =0 to 3A<br>T <sub>j</sub> =-10 to 100°C |
| Line Regulation 1                           | Reg. <sub>I1</sub>   | -                      | 0.1                    | 0.5                    | %/V  | V <sub>cc</sub> =4.3V to 5.5V                           |
| Line Regulation 2                           | Reg. <sub>I2</sub>   | -                      | 0.1                    | 0.5                    | %/V  | V <sub>IN</sub> =1.5V to 3.3V                           |
| Load Regulation                             | Reg. <sub>L</sub>    | -                      | 0.5                    | 10                     | mV   | I <sub>o</sub> =0 to 3A                                 |
| Minimum dropout voltage                     | dV <sub>o</sub>      | -                      | 65                     | 100                    | mV   | I <sub>o</sub> =1A, V <sub>IN</sub> =1.2V               |
| Standby Discharge Current                   | I <sub>den</sub>     | 1                      | -                      | -                      | mA   | V <sub>en</sub> =0V, V <sub>o</sub> =1V                 |
| [ENABLE]                                    |                      |                        |                        |                        |      |                                                         |
| Enable Pin Input Voltage High               | En <sub>hi</sub>     | 2                      | -                      | -                      | V    |                                                         |
| Enable Pin Input Voltage Low                | En <sub>low</sub>    | -0.2                   | -                      | 0.8                    | V    |                                                         |
| Enable Input Bias Current                   | I <sub>en</sub>      | -                      | 6                      | 10                     | μA   | V <sub>en</sub> =3V                                     |
| [FEEDBACK]                                  |                      |                        |                        |                        |      |                                                         |
| Feedback Pin Bias Current                   | I <sub>FB</sub>      | -100                   | 0                      | 100                    | nA   |                                                         |
| [NRCS]                                      |                      |                        |                        |                        |      |                                                         |
| NRCS Charge Current                         | I <sub>nrcs</sub>    | 14                     | 20                     | 26                     | μA   | V <sub>nrcs</sub> =0.5V                                 |
| NRCS Standby Voltage                        | V <sub>STB</sub>     | -                      | 0                      | 50                     | mV   | V <sub>en</sub> =0V                                     |
| [UVLO]                                      |                      |                        |                        |                        |      |                                                         |
| VCC Undervoltage Lockout Threshold Voltage  | V <sub>ccUVLO</sub>  | 3.5                    | 3.8                    | 4.1                    | V    | V <sub>cc</sub> :Sweep-up                               |
| VCC Undervoltage Lockout Hysteresis Voltage | V <sub>cchys</sub>   | 100                    | 160                    | 220                    | mV   | V <sub>cc</sub> :Sweep-down                             |
| VD Undervoltage Lockout Threshold Voltage   | V <sub>DUVLO</sub>   | V <sub>REF</sub> × 0.6 | V <sub>REF</sub> × 0.7 | V <sub>REF</sub> × 0.8 | V    | V <sub>D</sub> :Sweep-up                                |
| [SCP]                                       |                      |                        |                        |                        |      |                                                         |
| SCP Startup Voltage                         | V <sub>OSCP</sub>    | V <sub>o</sub> × 0.3   | V <sub>o</sub> × 0.4   | V <sub>o</sub> × 0.5   | V    |                                                         |
| SCP Threshold Voltage                       | V <sub>SCPTH</sub>   | 1.05                   | 1.15                   | 1.25                   | V    |                                                         |
| SCP Charge Current                          | I <sub>SCP</sub>     | 1.4                    | 2                      | 2.6                    | μA   |                                                         |
| SCP Standby Voltage                         | V <sub>SCPSTBY</sub> | -                      | -                      | 50                     | mV   |                                                         |
| [PGOOD]                                     |                      |                        |                        |                        |      |                                                         |
| Low-side Threshold Voltage                  | V <sub>THPGL</sub>   | V <sub>o</sub> × 0.87  | V <sub>o</sub> × 0.9   | V <sub>o</sub> × 0.93  | V    |                                                         |
| High-side Threshold Voltage                 | V <sub>THPGH</sub>   | V <sub>o</sub> × 1.07  | V <sub>o</sub> × 1.1   | V <sub>o</sub> × 1.13  | V    |                                                         |
| PGDLY Charge Current                        | I <sub>pgdly</sub>   | 1.4                    | 2.0                    | 2.6                    | μA   | ※                                                       |
| Ron                                         | R <sub>PG</sub>      | -                      | 0.1                    | -                      | kΩ   |                                                         |

※PGOOD delay time is determined as in formula below.

$$t_{pgdly} = \frac{C(pF) \times 1.23}{I_{pgdly} (\mu A)} (\mu sec)$$

●Reference Data

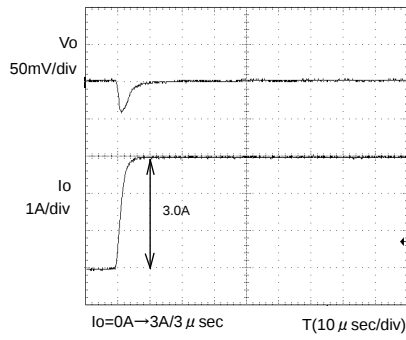


Fig.1 Transient Response  
(0→3A)  
Co=22 μ F, Cfb=1000pF

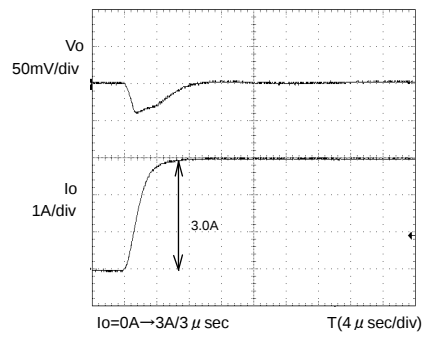


Fig.2 Transient Response  
(0→3A)  
Co=100 μ F

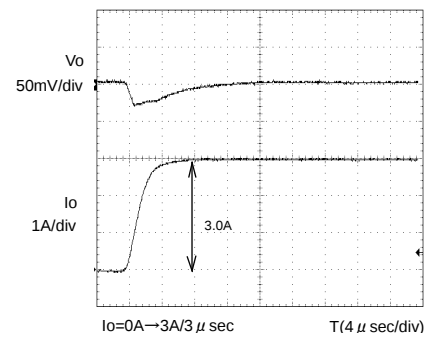


Fig.3 Transient Response  
(0→3A)  
Co=100 μ F, Cfb=1000pF

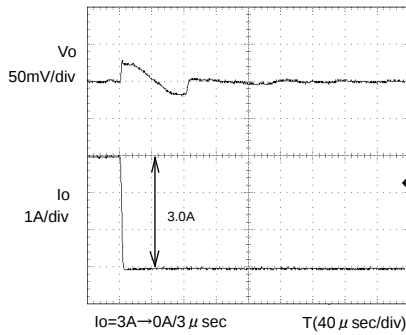


Fig.4 Transient Response  
(3→0A)  
Co=22 μ F, Cfb=1000pF

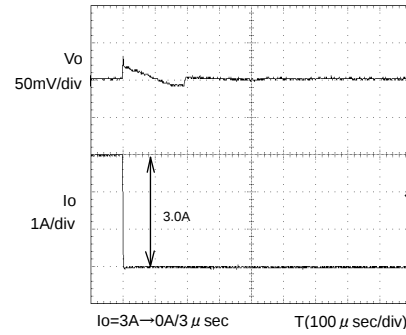


Fig.5 Transient Response  
(3→0A)  
Co=100 μ F

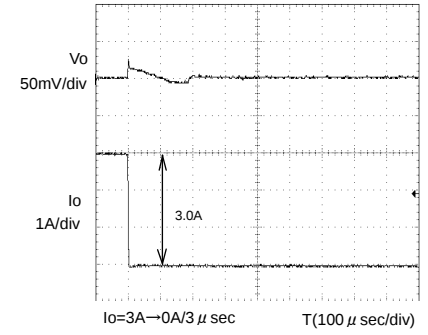


Fig.6 Transient Response  
(3→0A)  
Co=100 μ F, Cfb=1000pF

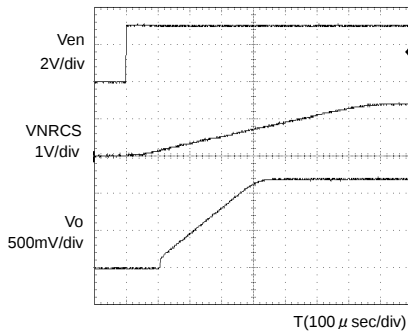


Fig.7 Waveform at output start

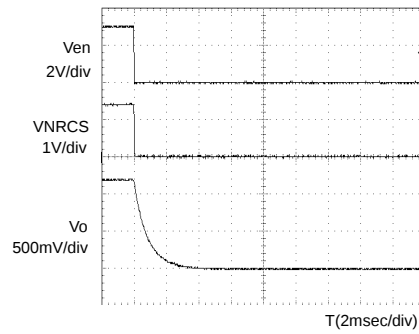


Fig.8 Waveform at output OFF

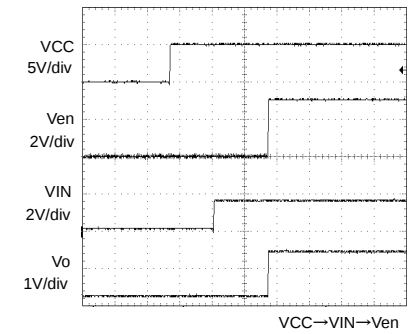


Fig.9 Input sequence

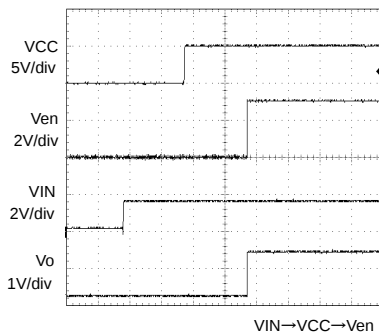


Fig.10 Input sequence

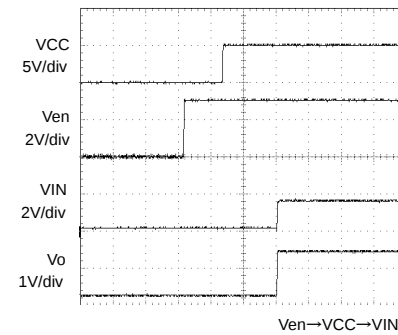


Fig.11 Input sequence

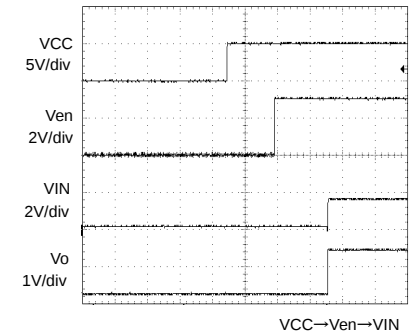


Fig.12 Input sequence

●Reference Data

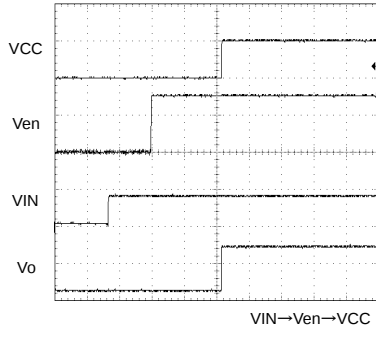


Fig.13 Input sequence

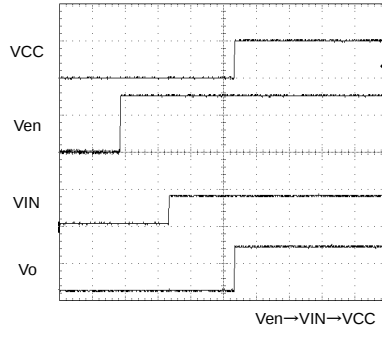


Fig.14 Input sequence

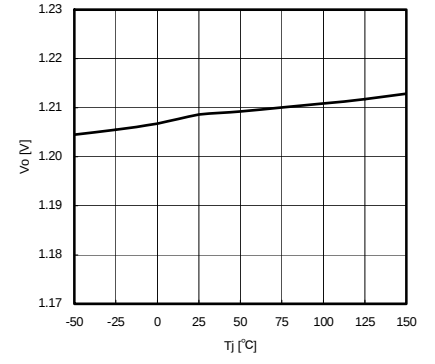


Fig.15 Tj-Vo

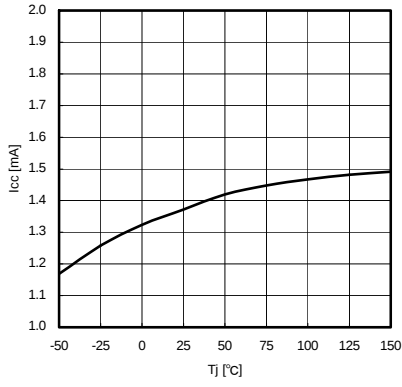


Fig.16 Tj-ICC

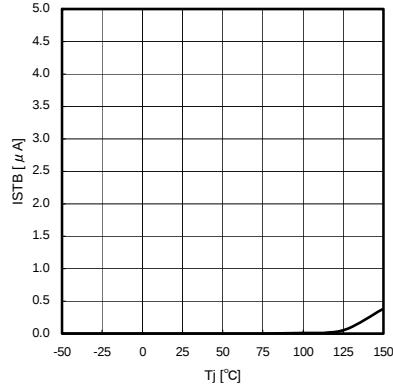


Fig.17 Tj-ISTB

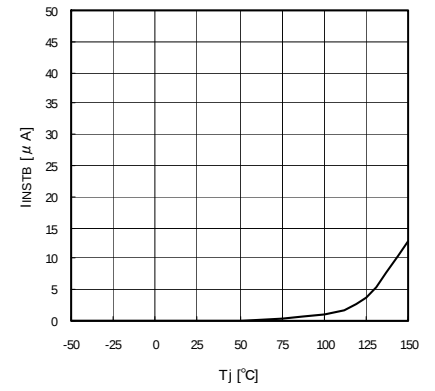


Fig.18 Tj-IINSTB

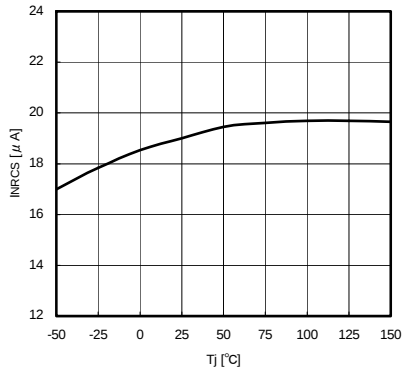


Fig.19 Tj-INRCS

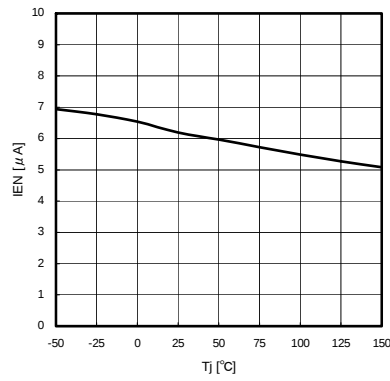


Fig.20 Tj-IEN

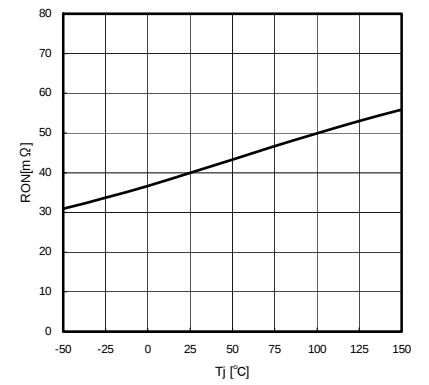


Fig.21 Tj- $R_{ON}$   
( $V_{CC}=5V/V_O=1.2V$ )

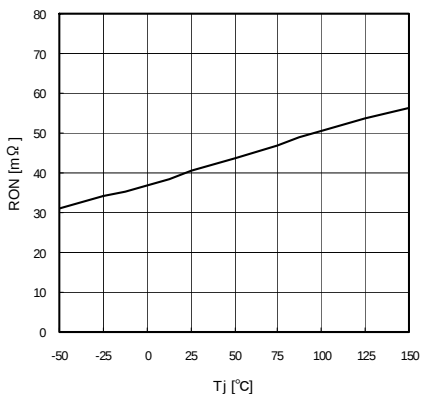


Fig.22 Tj- $R_{ON}$   
( $V_{CC}=5V/V_O=1.5V$ )

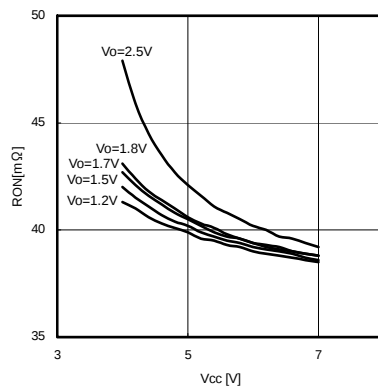
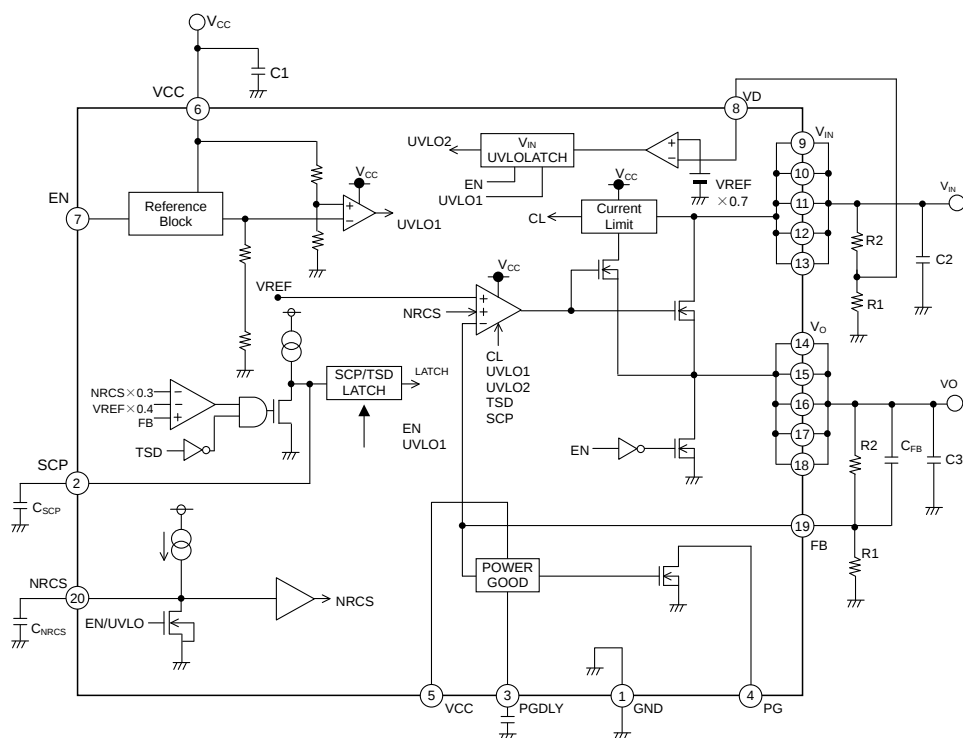
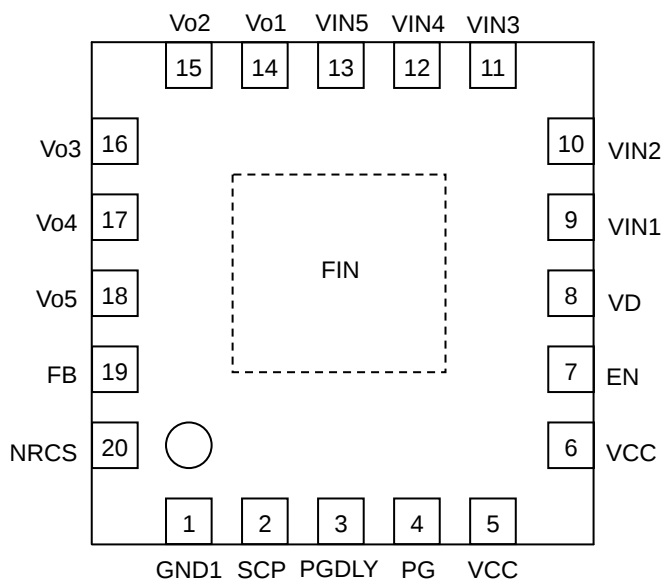


Fig.23  $V_{CC}$ - $R_{ON}$

- Block Diagram



## ● Pin Layout



## ●Pin Function Table

| PIN No. | PIN name | PIN Function                                               |
|---------|----------|------------------------------------------------------------|
| 1       | GND1     | Ground Pin 1                                               |
| 2       | SCP      | SCP Delay Time Setting Capacitor Connection Pin            |
| 3       | PGDLY    | PGOOD Delay Setting Capacitor Connection Pin               |
| 4       | PG       | Power Good Pin                                             |
| 5       | VCC      | Power Supply Pin                                           |
| 6       | VCC      | Power Supply Pin                                           |
| 7       | EN       | Enable Input Pin                                           |
| 8       | VD       | VIN Input Voltage Detect Pin                               |
| 9       | VIN1     | Input Voltage Pin 1                                        |
| 10      | VIN2     | Input Voltage Pin 2                                        |
| 11      | VIN3     | Input Voltage Pin 3                                        |
| 12      | VIN4     | Input Voltage Pin 4                                        |
| 13      | VIN5     | Input Voltage Pin 5                                        |
| 14      | Vo1      | Output Voltage Pin 1                                       |
| 15      | Vo2      | Output Voltage Pin 2                                       |
| 16      | Vo3      | Output Voltage Pin 3                                       |
| 17      | Vo4      | Output Voltage Pin 4                                       |
| 18      | Vo5      | Output Voltage Pin 5                                       |
| 19      | FB       | Reference Voltage Feedback Pin                             |
| 20      | NRCS     | In-rush Current Protection (NRCS) Capacitor Connection Pin |
| bottom  | FIN      | Connected to heatsink and GND                              |

\* Please short N.C to the GND line.

## ● Operation of Each Block

### • AMP

This is an error amp compares the reference voltage (0.65V) with  $V_O$  to drive the output Nch FET ( $R_{on}=50m\Omega$ ). Frequency optimization helps to realize rapid transient response, and to support the use of ceramic capacitors on the output. AMP input voltage ranges from GND to 2.7V, while the AMP output ranges from GND to  $V_{CC}$ . When EN is OFF, or when UVLO is active, output goes LOW and the output of the NchFET switches OFF.

### • EN

The EN block controls the regulator's ON/OFF state via the EN logic input pin. In the OFF position, circuit voltage is maintained at  $0\mu A$ , thus minimizing current consumption at standby. The FET is switched ON to enable discharge of the NRCS pin  $V_O$ , thereby draining the excess charge and preventing the IC on the load side from malfunctioning. Since no electrical connection is required (e.g. between the  $V_{CC}$  pin and the ESD prevention diode), module operation is independent of the input sequence.

### • UVLO

To prevent malfunctions that can occur during a momentary decrease in  $V_{CC}$ , the UVLO circuit switches the output OFF, and (like the EN block) discharges NRCS and  $V_O$ . Once the UVLO threshold voltage (TYP3.80V) is reached, the power-on reset is triggered and output continues.

### • CURRENT LIMIT

When output is ON, the current limit function monitors the internal IC output current against the parameter value. When current exceeds this level, the current limit module lowers the output current to protect the load IC. When the overcurrent state is eliminated, output voltage is restored to the parameter value.

### • NRCS (Non Rush Current on Start-up)

The soft start function enabled by connecting an external capacitor between the NRCS pin and ground. Output ramp-up can be set for any period up to the time the NRCS pin reaches  $V_{FB}$  (0.65V). During startup, the NRCS pin serves as a  $20\mu A$  (TYP) constant current source to charge the external capacitor. Capacitors with low susceptibility ( $0.001\mu F \sim 1\mu F$ ) to temperature are recommended, in order to assure a stable soft-start time.

### • TSD (Thermal Shut down)

The shutdown (TSD) circuit automatically is latched OFF when the chip temperature exceeds the threshold temperature after the programmed time period elapses, thus serving to protect the IC against "thermal runaway" and heat damage. Because the TSD circuit is intended to shut down the IC only in the presence of extreme heat, it is crucial that the  $T_j$  (max) parameter not be exceeded in the thermal design, in order to avoid potential problems with the TSD.

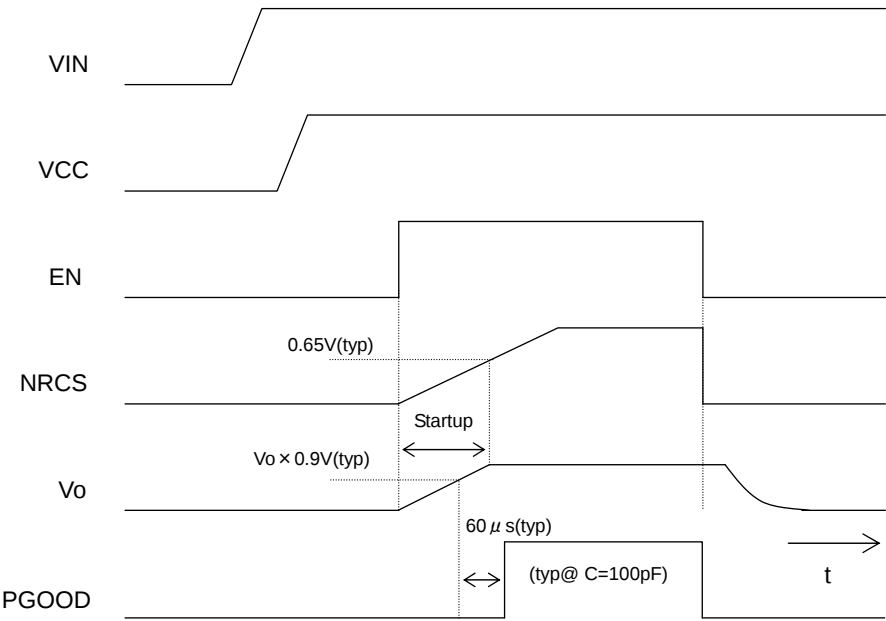
### • VIN

The  $V_{IN}$  line acts as the major current supply line, and is connected to the output NchFET drain. Since no electrical connection (such as between the  $V_{CC}$  pin and the ESD protection diode) is necessary,  $V_{IN}$  operates independent of the input sequence. However, since an output NchFET body diode exists between  $V_{IN}$  and  $V_O$ , a  $V_{IN}$ - $V_O$  electric (diode) connection is present. Note, therefore, that when output is switched ON or OFF, reverse current may flow to  $V_{IN}$  from  $V_O$ .

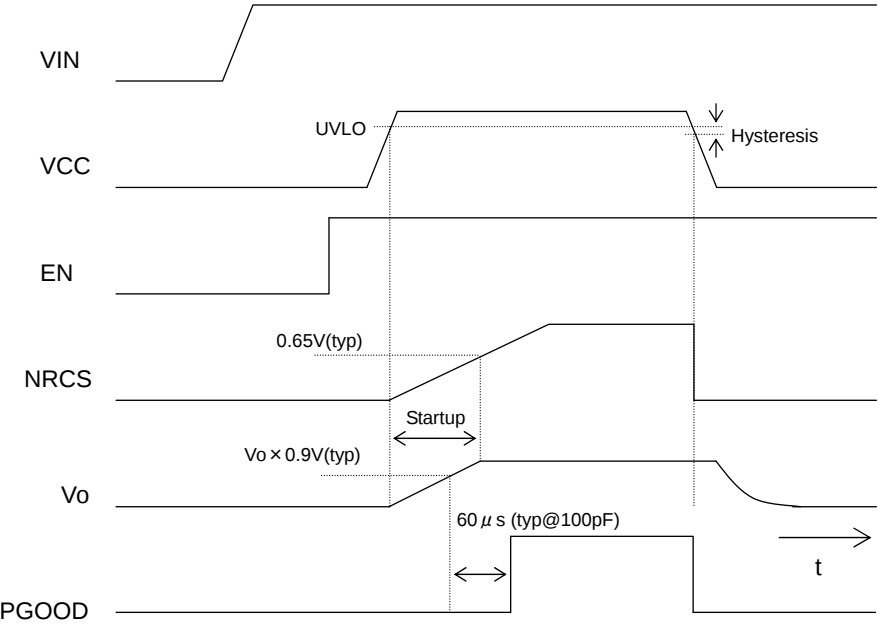
### • PGOOD

It outputs the status of the output voltage. This is open drain pin and connects to  $V_{CC}$  pin through the pull-up resistance ( $100k\Omega$  or so). When the output voltage range is  $V_O \times 0.9$  to  $V_O \times 1.1$ (TYP), the status is high.

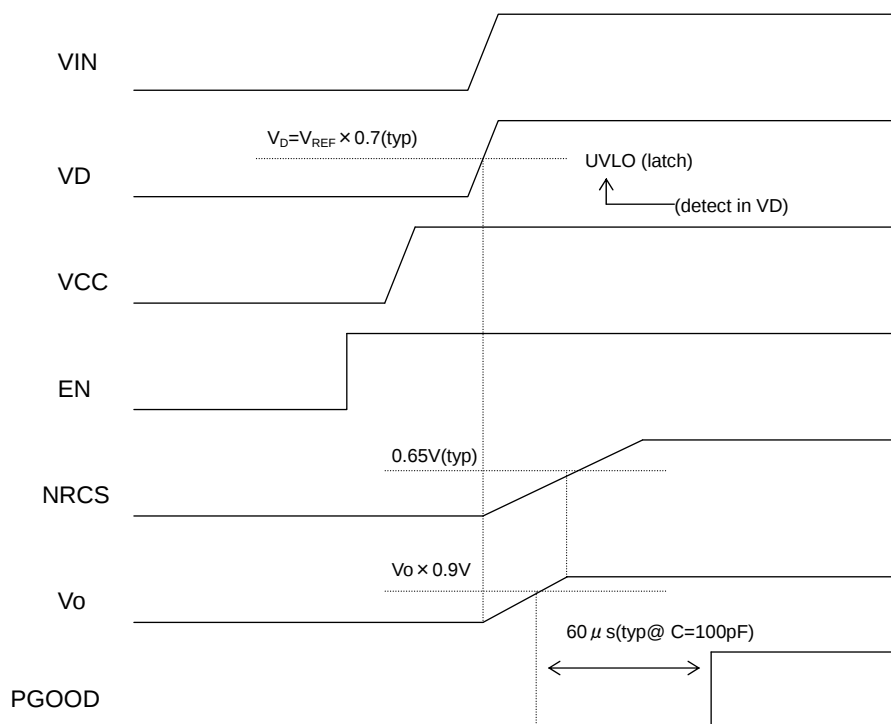
●Timing Chart  
EN ON/OFF



VCC ON/OFF

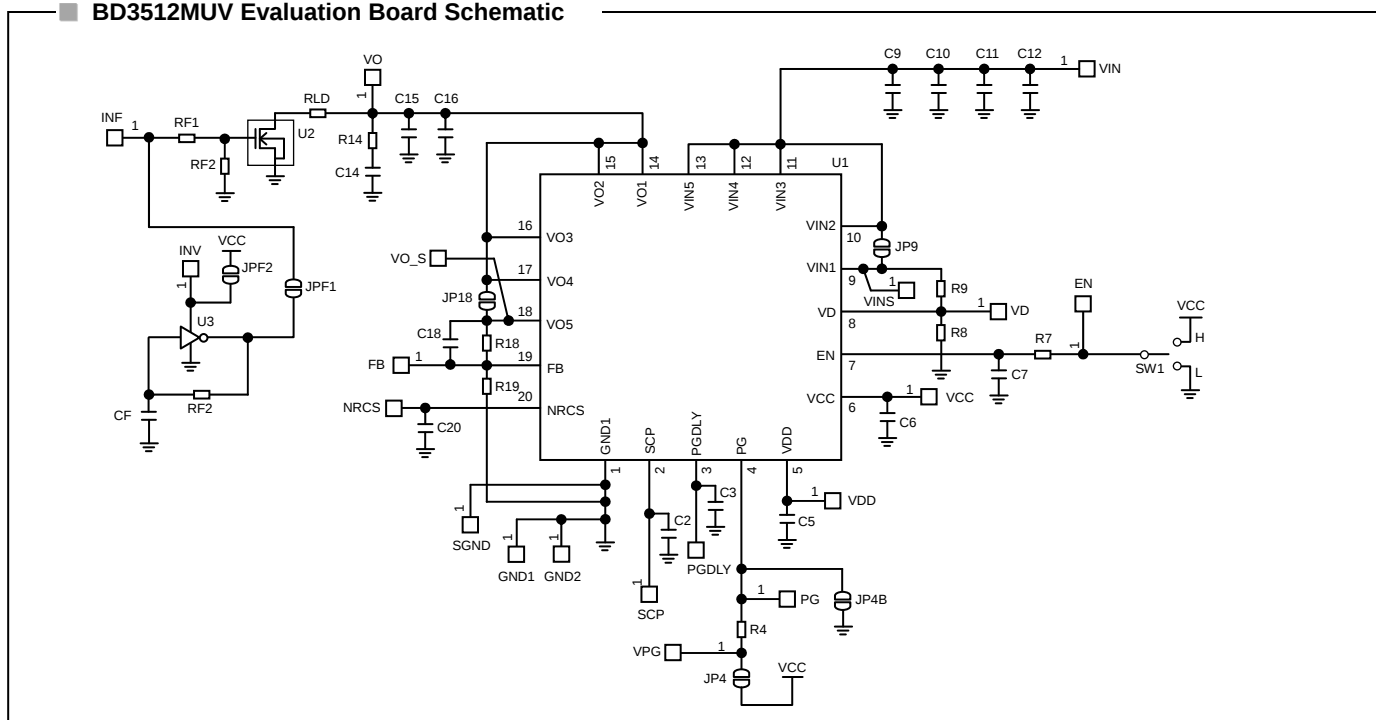


# VIN ON/OFF



## ●Evaluation Board

## BD3512MUV Evaluation Board Schematic



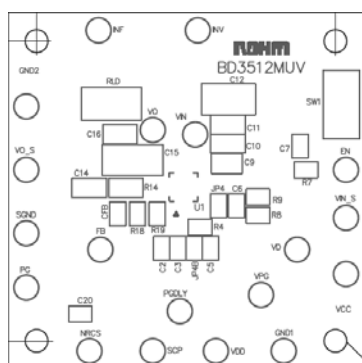
## ■ BD3512MUV Evaluation Board Standard Component List

| Component | Rating        | Manufacturer | Product Name      |
|-----------|---------------|--------------|-------------------|
| U1        | -             | ROHM         | BD3512MUV         |
| C2        | 100pF         | MURATA       | CRM1882C1H101JA01 |
| C3        | 100pF         | MURATA       | CRM1882C1H101JA01 |
| R4        | 100k $\Omega$ | ROHM         | MCR03EZPF1003     |
| C5        | 0.1uF         | KYOCERA      | CM05104K10A       |
| C6        | 1uF           | KYOCERA      | CM105B105K06A     |
| R7        | 0 $\Omega$    | -            | jumper            |

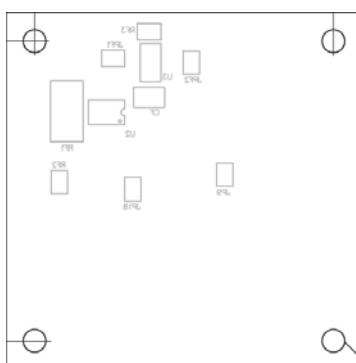
| Component | Rating | Manufacturer | Product Name      |
|-----------|--------|--------------|-------------------|
| R8        | 3.9kΩ  | ROHM         | MCR03EZPF3901     |
| R9        | 3.3kΩ  | ROHM         | MCR03EZPF3301     |
| C9        | 10uF   | KYOCERA      | CM21B106M06A      |
| C16       | 22uF   | KYOCERA      | CM316B226M06A     |
| R18       | 3.3kΩ  | ROHM         | MCR03EZPF3301     |
| R19       | 3.9kΩ  | ROHM         | MCR03EZPF3901     |
| V20       | 0.01uF | MURATA       | GRM188B11H102KA01 |

## ■ BD3512MUV Evaluation Board Layout

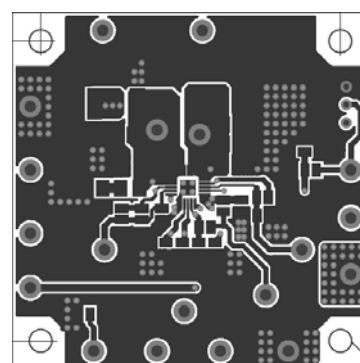
## Silk Screen (Top)



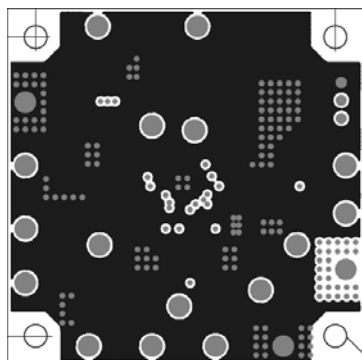
### Silk Screen (Bottom)



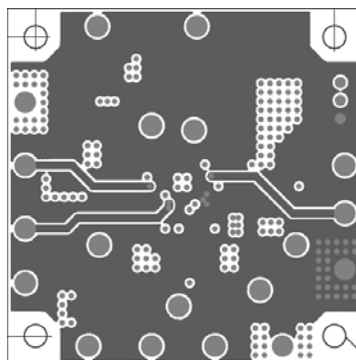
### TOP Layer



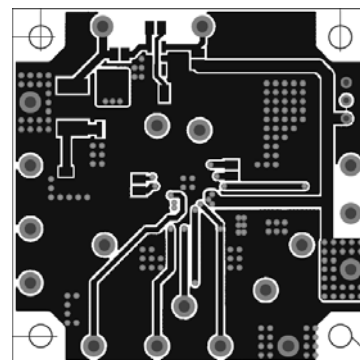
### Middle Layer\_1



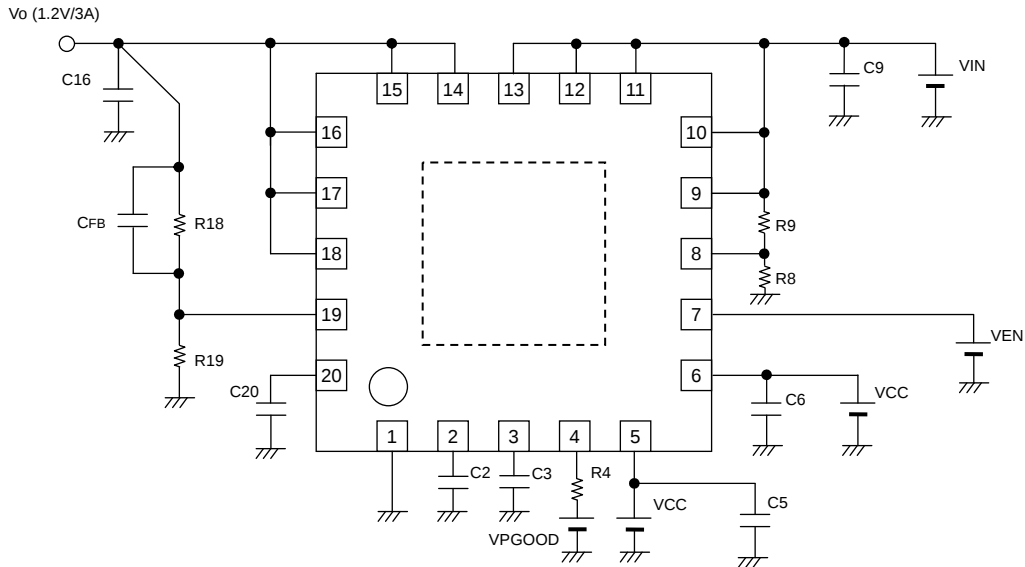
### Middle Layer\_2



### Bottom Layer



## ●Recommended Circuit Example



| Component | Recommended Value             | Programming Notes and Precautions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R18/R19   | 3.3k/3.9k                     | IC output voltage can be set with a configuration formula $V_{FB} \times (R18+R19)/R19$ using the values for the internal reference output voltage ( $V_{FB}$ ) and the output voltage resistors (R18, R19). Select resistance values that will avoid the impact of the FB bias current ( $\pm 100\text{nA}$ ). The recommended total resistance value is $10\text{K}\Omega$ .                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| R4        | 100k                          | This is the pull-up resistance for open drain pin. It is recommended to set the value about $100\text{k}\Omega$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| C16       | $22\mu\text{F}$               | To assure output voltage stability, please be certain the Vo1~Vo5 pins and the GND pins are connected. Output capacitors play a role in loop gain phase compensation and in mitigating output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series resistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a $22\mu\text{F}$ ceramic capacitor is recommended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. In light of this information, please confirm operation across a variety of temperature and load conditions. |
| C6/C5     | $1\mu\text{F}/0.1\mu\text{F}$ | Input capacitors reduce the output impedance of the voltage supply source connected to the (VCC) input pins. If the impedance of this power supply were to increase, input voltage (VCC) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR $1\mu\text{F} / 0.1\mu\text{F}$ capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.                                                                                                                                                                                                     |
| C9        | $10\mu\text{F}$               | Input capacitors reduce the output impedance of the voltage supply source connected to the (VIN) input pins. If the impedance of this power supply were to increase, input voltage (VIN) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR $10\mu\text{F}$ capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.                                                                                                                                                                                                                     |
| C20       | $0.01\mu\text{F}$             | The Non Rush Current on Startup (NRCS) function is built into the IC to prevent rush current from going through the load (VIN to VO) and impacting output capacitors at power supply start-up. Constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportionate to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportionate to this reference voltage. Capacitors with low susceptibility to temperature are recommended, in order to assure a stable soft-start time.                                                                                                                                                                                                                         |
| CFB       | $1000\text{pF}$               | This component is employed when the C16 capacitor causes, or may cause, oscillation. It provides more precise internal phase correction.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

## ●Heat Loss

Thermal design should allow operation within the following conditions. Note that the temperatures listed are the allowed temperature limits, and thermal design should allow sufficient margin from the limits.

1. Ambient temperature  $T_a$  can be no higher than 100 °C.
2. Chip junction temperature ( $T_j$ ) can be no higher than 150°C.

Chip junction temperature can be determined as follows:

- ① Calculation based on ambient temperature ( $T_a$ )

$$T_j = T_a + \theta_{j-a} \times W$$

<Reference values>

$\theta_{j-a}$ : VQFN020V4040 249.5°C/W IC only

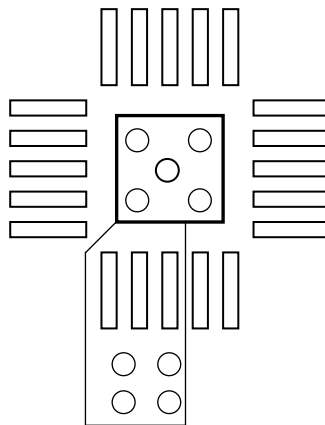
160.1°C/W 1-layer substrate (copper foil area : 0mm<sup>2</sup>)

82.6°C/W 4-layer substrate (copper foil area : 10.29mm<sup>2</sup>)

31.2°C/W 4-layer substrate (copper foil area : 5505mm<sup>2</sup>)

Substrate size: 74.2 × 74.2 × 1.6mm<sup>3</sup> (substrate with thermal via)

It is recommended to layout the VIA for heat radiation in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multilayer substrate). This package is so small (size: 2.9mm × 3.0mm) that it is not available to layout the VIA in the bottom of IC. Spreading the pattern and being increased the number of VIA like the figure below enable to get the superior heat radiation characteristic. (This figure is the image. It is recommended that the VIA size and the number is designed suitable for the actual situation.).



Most of the heat loss that occurs in the BD3512MUV is generated from the output Nch FET. Power loss is determined by the total  $V_{IN}$ - $V_o$  voltage and output current. Be sure to confirm the system input and output voltage and the output current conditions in relation to the heat dissipation characteristics of the  $V_{IN}$  and  $V_o$  in the design. Bearing in mind that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BD3512MUV) make certain to factor conditions such as substrate size into the thermal design.

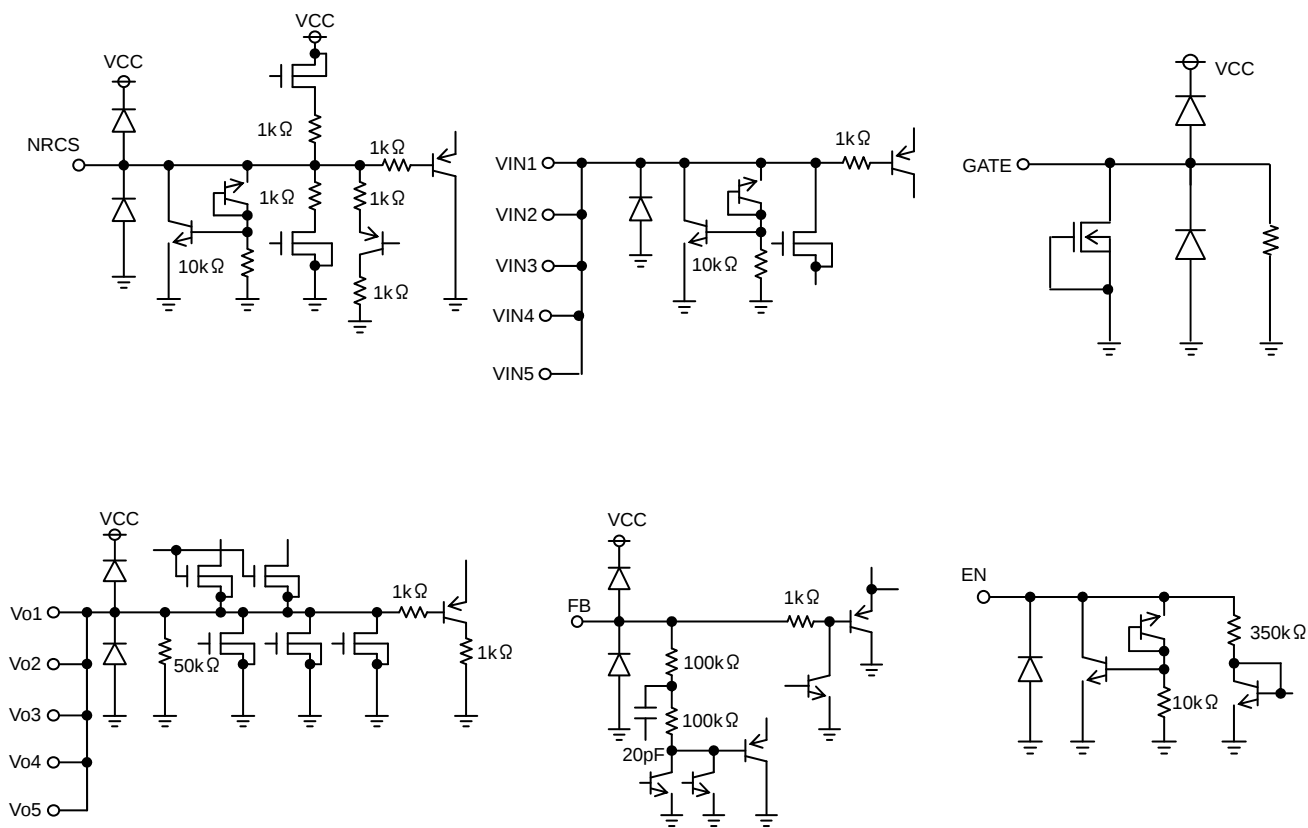
$$\text{Power consumption (W)} = \left\{ \text{Input voltage (V}_{IN}\text{)} - \text{Output voltage (V}_o\text{)} (V_o \doteq V_{REF}) \right\} \times I_o(\text{Ave})$$

Example) Where  $V_{IN}=1.5\text{V}$ ,  $V_o=1.25\text{V}$ ,  $I_o(\text{Ave}) = 4\text{A}$ ,

$$\text{Power consumption (W)} = \left\{ 1.5(\text{V}) - 1.2(\text{V}) \right\} \times 4.0(\text{A})$$

$$= 1.0(\text{W})$$

●Input-Output Equivalent Circuit Diagram



## ● Operation Notes

### 1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

### 2. Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

### 3. Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

### 4. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

### 5. Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

### 6. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

### 7. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

### 8. ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

### 9. Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

|           | TSD on temperature [°C] (typ.) | Hysteresis temperature [°C] (typ.) |
|-----------|--------------------------------|------------------------------------|
| BD3512MUV | 175                            | 15                                 |

### 10. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

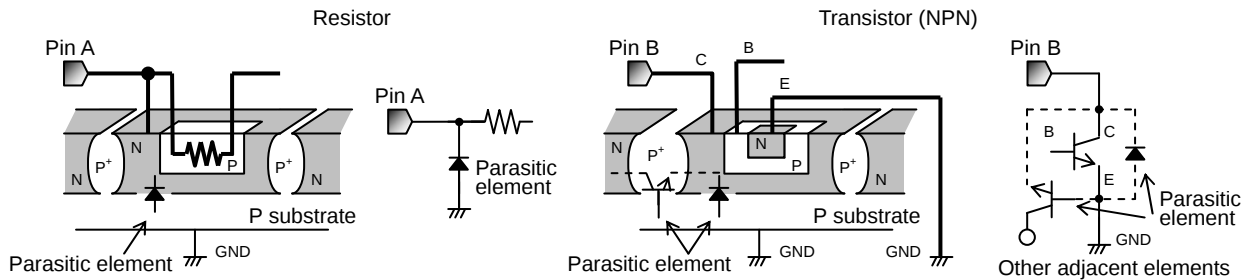
## 11. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When  $GND > Pin\ A$  and  $GND > Pin\ B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin\ B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



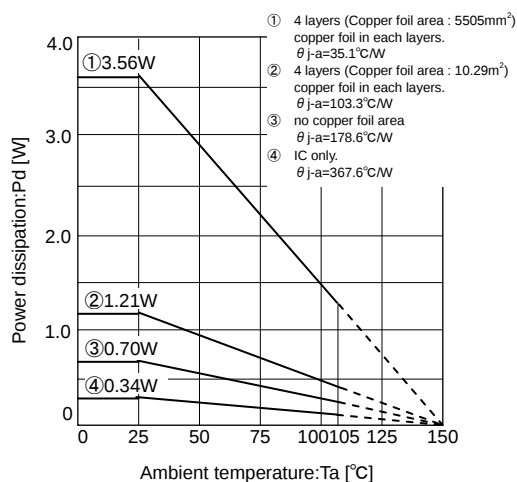
Example of IC structure

## 12. Ground Wiring Pattern.

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

## ●Heat Dissipation Characteristics

### ◎VQFN020V4040





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