

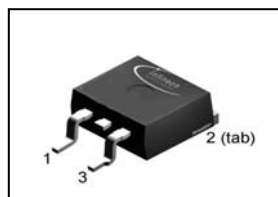
OptiMOS[®] -T Power-Transistor

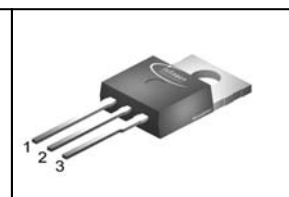
Features

- N-channel - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (lead free)
- Ultra low R_{DS(on)}
- Avalanche tested

Product Summary

V_{DS}	55	V
$R_{DS(on),max}$ (SMD version)	15.4	mΩ
I_D	45	A

PG-TO263-3-2

PG-TO262-3-1

PG-TO220-3-1


Type	Package	Ordering Code	Marking
IPB45N06S3-16	PG-TO263-3-2	SP0001-02224	3N0616
IPI45N06S3-16	PG-TO262-3-1	SP0001-02217	3N0616
IPP45N06S3-16	PG-TO220-3-1	SP0001-02218	3N0616



Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	45	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{2)}$	33	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	180	
Avalanche energy, single pulse ³⁾	E_{AS}	$I_D=27.5\text{ A}$	95	mJ
Drain gate voltage ²⁾	V_{DG}		55	
Gate source voltage ⁴⁾	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	65	W
Operating and storage temperature	T_J , T_{stg}		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}		-	-	2.3	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}		-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ⁵⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$	55	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=30\text{ }\mu\text{A}$	2.1	3	4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=25\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=25\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}^{1)}$	-	1	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}$, $I_D=23\text{ A}$	-	13.5	15.7	m Ω
		$V_{GS}=10\text{ V}$, $I_D=23\text{ A}$, SMD version	-	13.2	15.4	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	2980	-	pF
Output capacitance	C_{oss}		-	450	-	
Reverse transfer capacitance	C_{rss}		-	430	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=27.5\text{ V},$ $V_{GS}=10\text{ V}, I_D=45\text{ A},$ $R_G=22\ \Omega$	-	28	-	ns
Rise time	t_r		-	61	-	
Turn-off delay time	$t_{d(off)}$		-	26	-	
Fall time	t_f		-	68	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=11\text{ V}, I_D=45\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	23	-	nC
Gate to drain charge	Q_{gd}		-	10	-	
Gate charge total	Q_g		-	43	57	
Gate plateau voltage	$V_{plateau}$		-	7.2	-	V

Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ °C}$	-	-	45	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	180	
Diode forward voltage ²⁾	V_{SD}	$V_{GS}=0\text{ V}, I_F=45\text{ A},$ $T_J=25\text{ °C}$	-	1.1	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=27.5\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	-	-	ns
Reverse recovery charge ²⁾	Q_{rr}	$V_R=27.5\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	-	-	nC

¹⁾ Current is limited by bondwire; with an $R_{thJC} = 2.3\text{ K/W}$ the chip is able to carry 46A at 25°C. For detailed information see Application Note ANPS071E at www.infineon.com/optimos

²⁾ Defined by design. Not subject to production test.

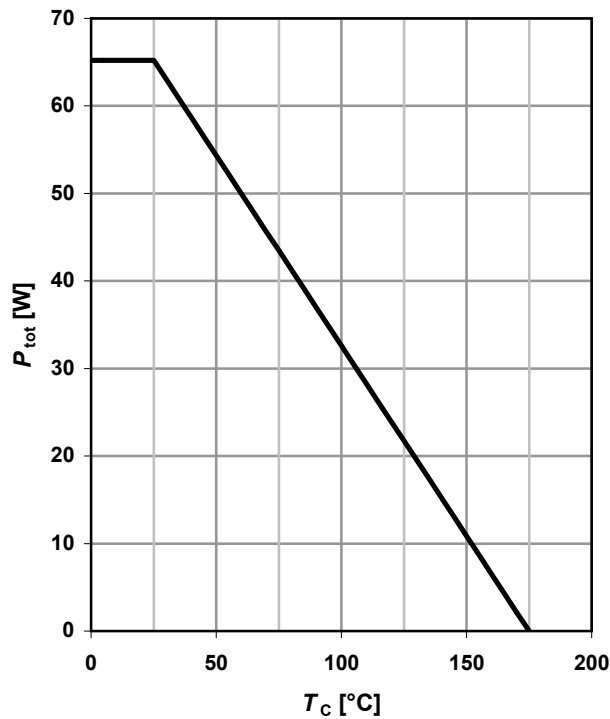
³⁾ See diagrams 12 and 13.

⁴⁾ Qualified at -5V and +20V.

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

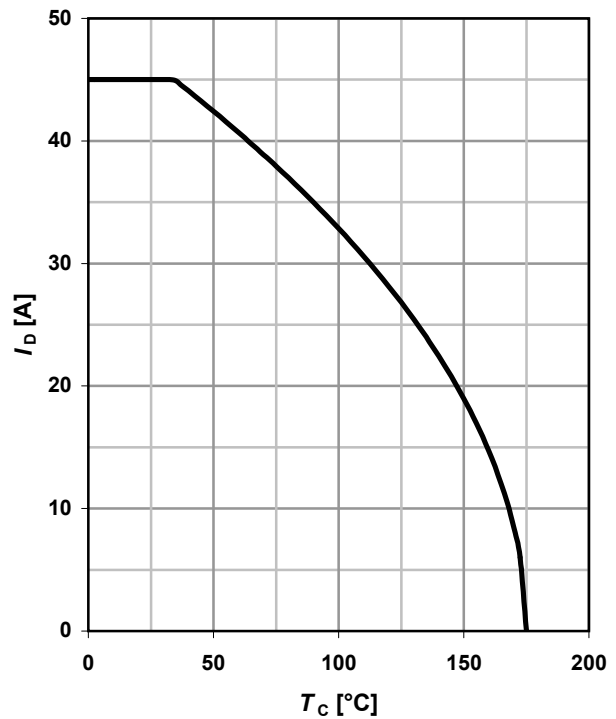
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

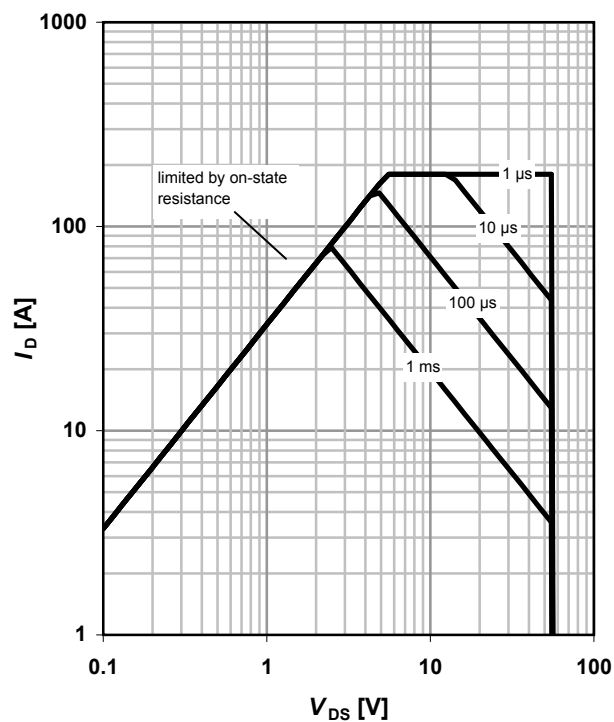
$$I_D = f(T_C); V_{\text{GS}} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0$$

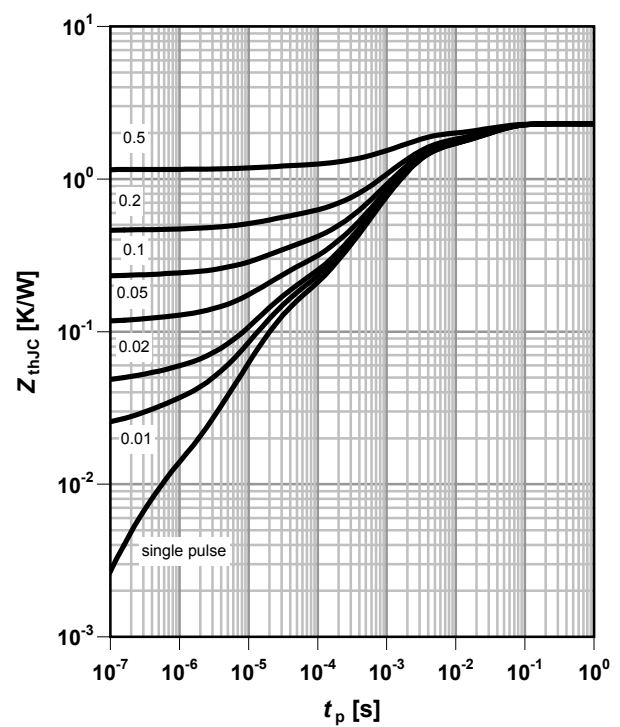
parameter: t_p



4 Max. transient thermal impedance

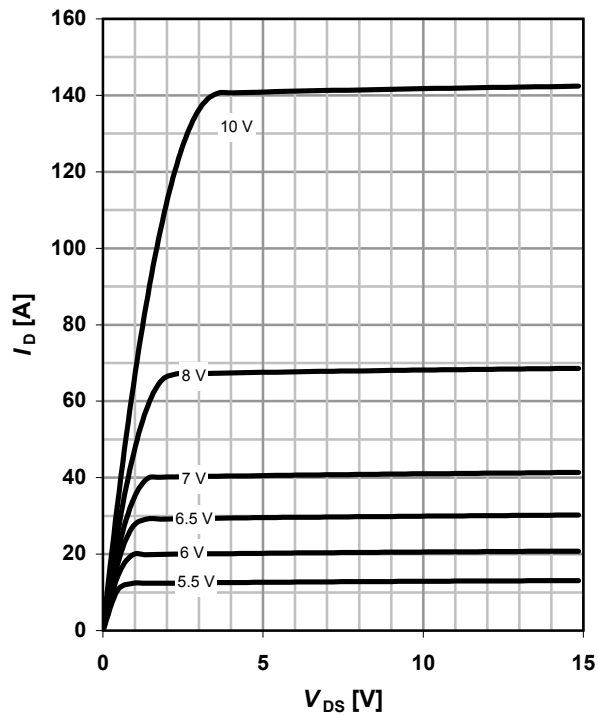
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p / T$



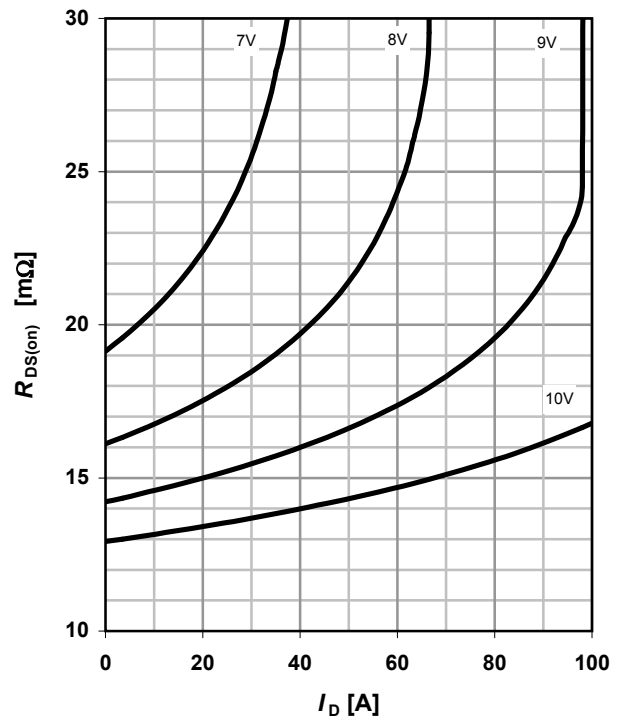
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS} , pulsed


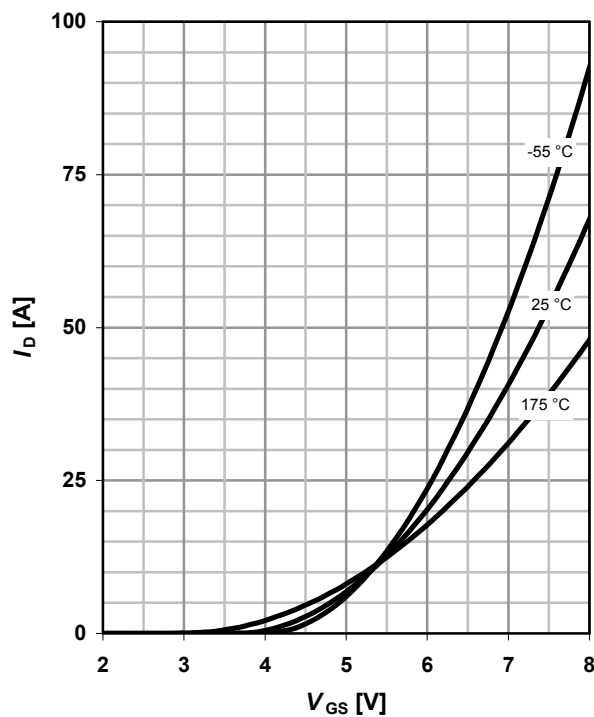
6 Typ. drain-source on resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

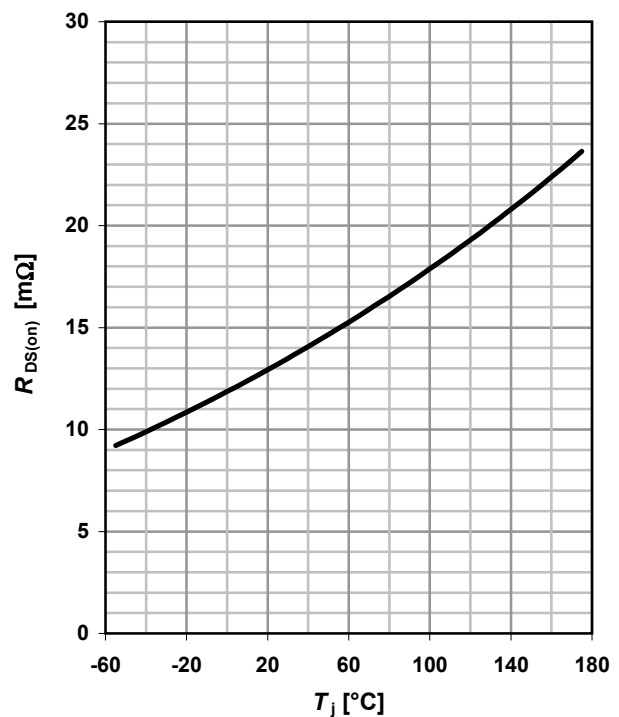
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 10\text{ V}$

parameter: T_j


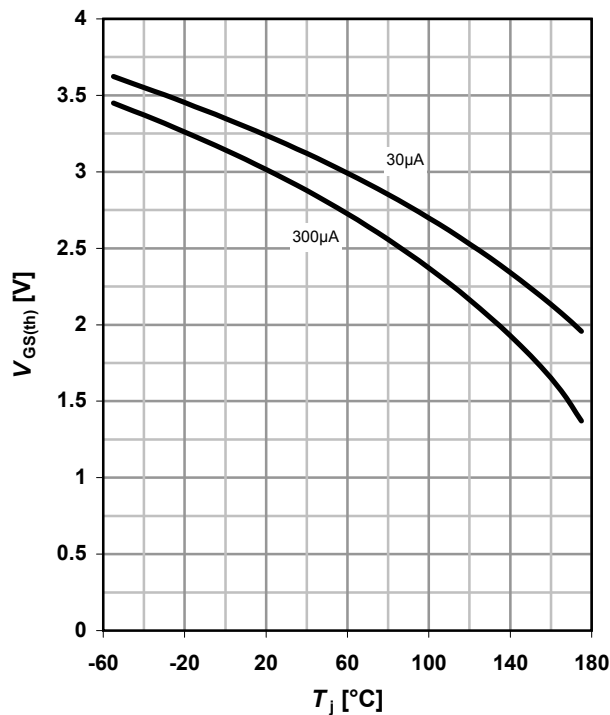
8 Drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = 20\text{ A}; V_{GS} = 10\text{ V}$


9 Typ. gate threshold voltage

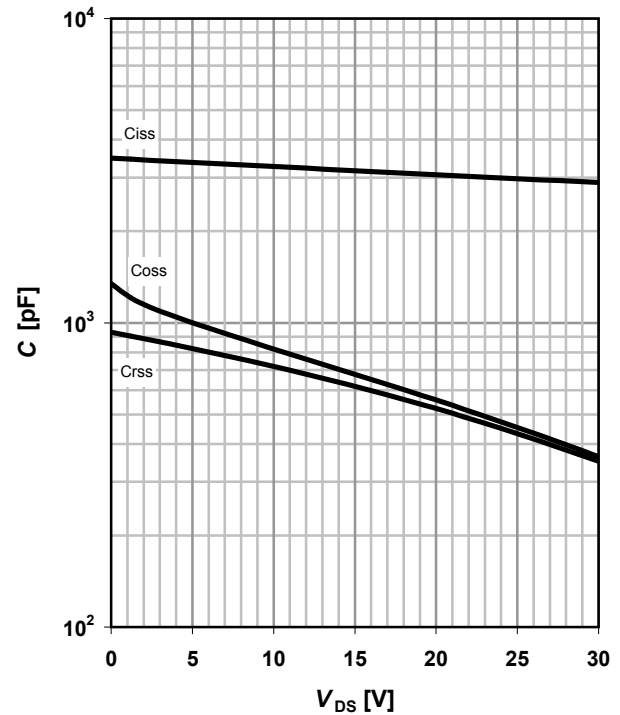
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

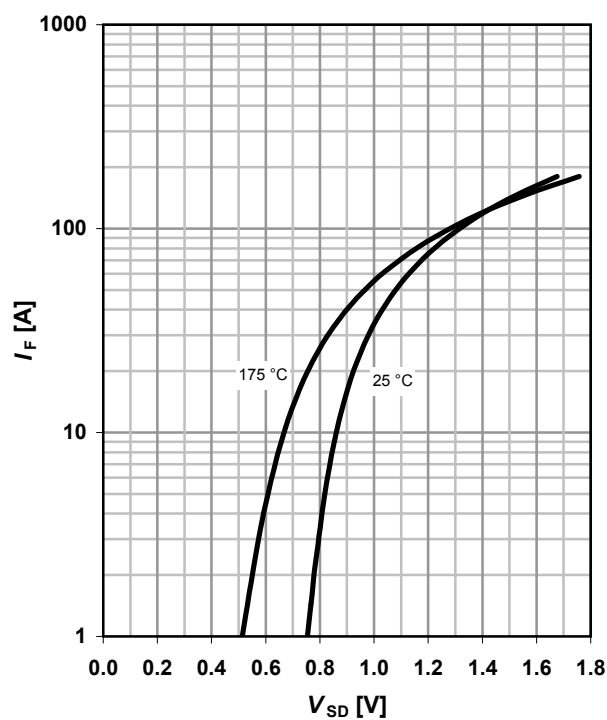
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Forward characteristics of reverse diode

$$I_F = f(V_{SD}), \text{ pulsed}$$

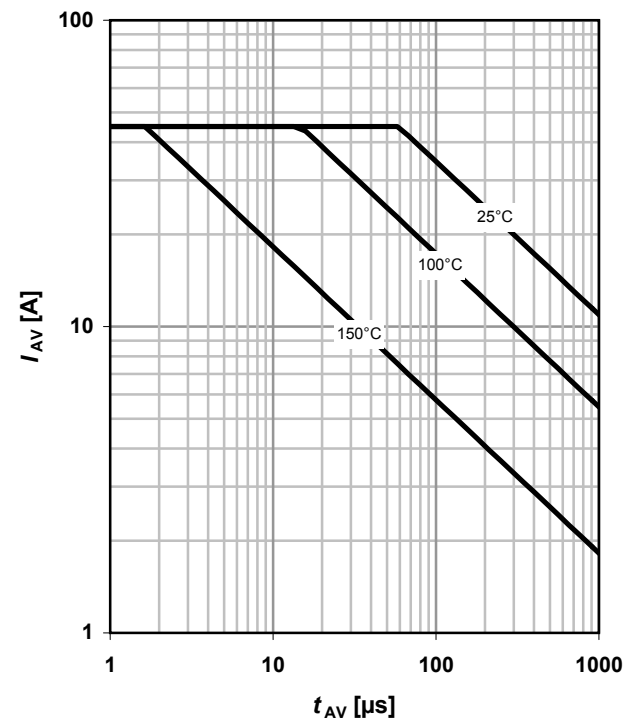
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

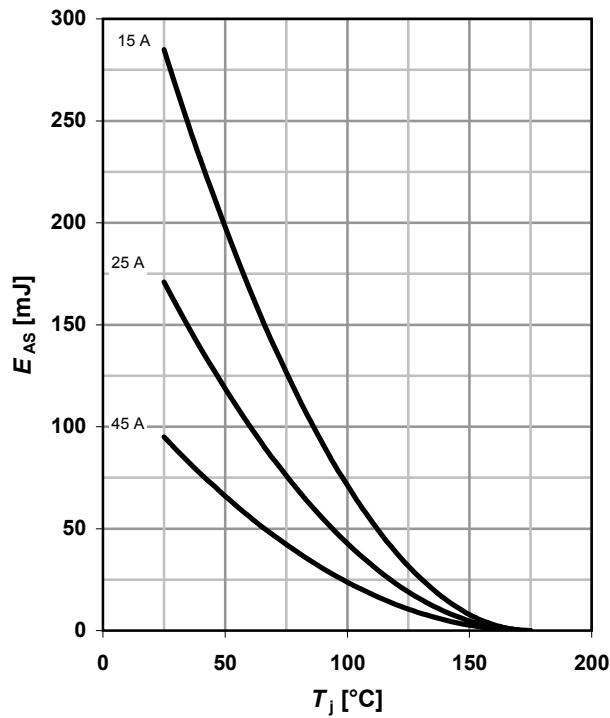
parameter: $T_{j(start)}$



13 Typ. avalanche energy

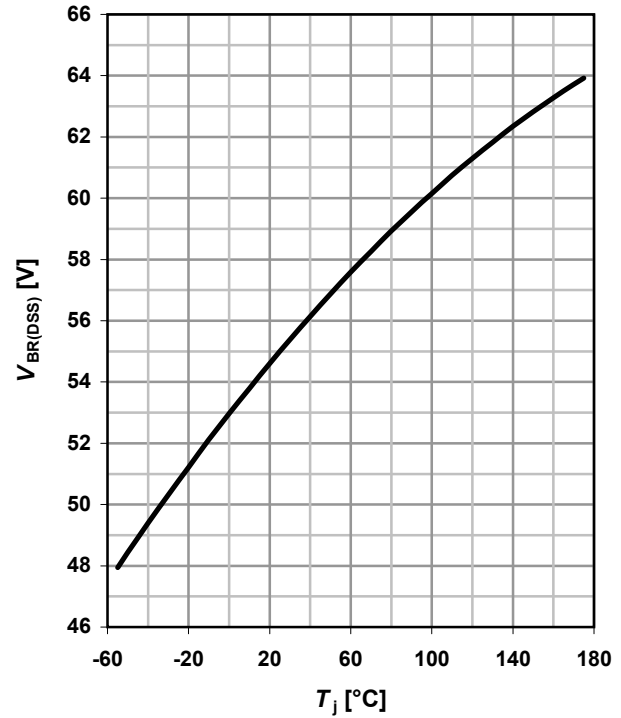
$$E_{AS}=f(T_j)$$

parameter: I_D



15 Drain-source breakdown voltage

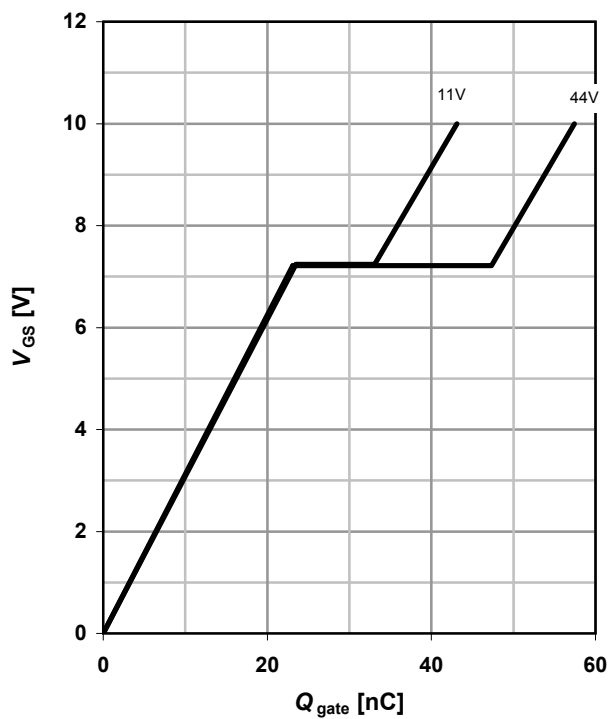
$$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$$



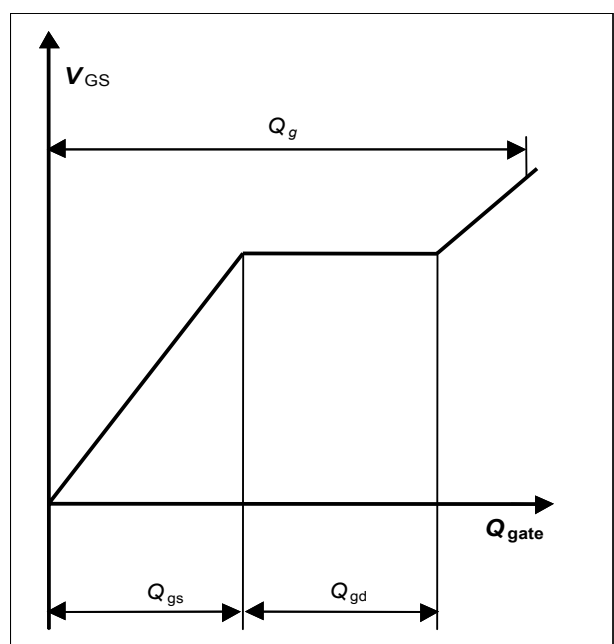
14 Typ. gate charge

$$V_{GS}=f(Q_{gate}); I_D=45 \text{ A pulsed}$$

parameter: V_{DD}

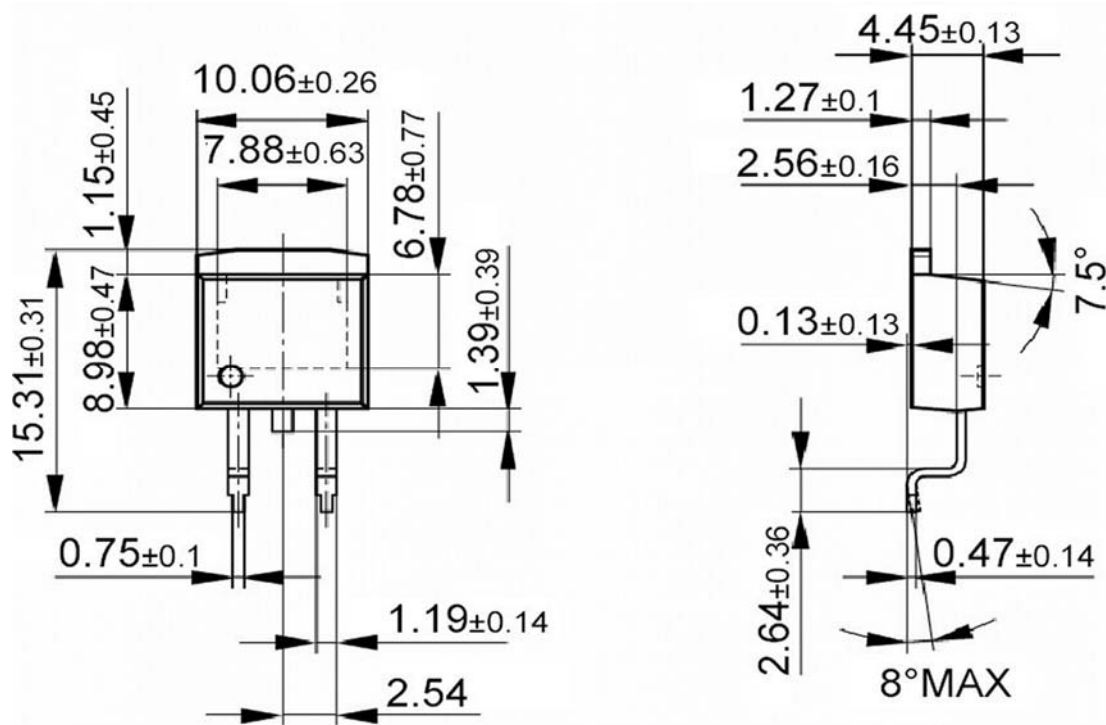


16 Gate charge waveforms



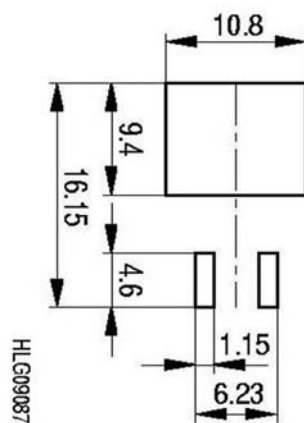
Package Outline

P-TO263-3-2: Outline

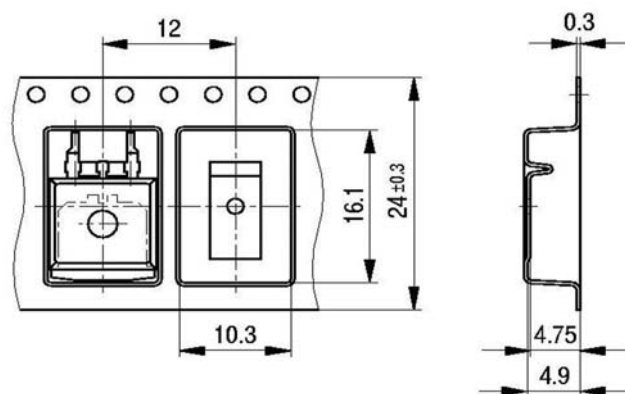


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Footprint



Packaging



Dimensions in mm

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