

BT1308 series D

Triacs logic level

Rev. 01 — 26 February 2008

Product data sheet

1. Product profile

1.1 General description

Passivated sensitive gate triacs in a SOT54 plastic package

1.2 Features

- Sensitive gate
- Direct interfacing to logic level ICs
- Gate triggering in four quadrants
- Direct interfacing to low-power gate drive circuits

1.3 Applications

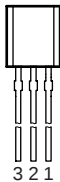
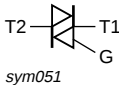
- General purpose switching and phase control
- Low-power AC fan speed control

1.4 Quick reference data

- $V_{DRM} \leq 400\text{ V}$ (BT1308-400D)
- $V_{DRM} \leq 600\text{ V}$ (BT1308-600D)
- $I_{TSM} \leq 9\text{ A}$ ($t = 20\text{ ms}$)
- $I_{GT} \leq 5\text{ mA}$
- $I_{GT} \leq 7\text{ mA}$ (T2–G+)
- $I_{T(RMS)} \leq 0.8\text{ A}$

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	main terminal 2 (T2)		
2	gate (G)		
3	main terminal 1 (T1)		
		SOT54 (TO-92)	

3. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
BT1308-400D	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54
BT1308-600D			

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage	BT1308-400D	-	400	V
		BT1308-600D	-	600	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{lead}} \leq 55\text{ °C}$; see Figure 4 and 5	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_j = 25\text{ °C}$ prior to surge; see Figure 2 and 3			
		$t = 20\text{ ms}$	-	9	A
		$t = 16.7\text{ ms}$	-	10	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$	-	0.32	A ² s
di_T/dt	rate of rise of on-state current	$I_{\text{TM}} = 1\text{ A}$; $I_G = 20\text{ mA}$; $di_G/dt = 0.2\text{ A}/\mu\text{s}$			
		T2+ G+	-	50	A/ μs
		T2+ G-	-	50	A/ μs
		T2- G-	-	50	A/ μs
		T2- G+	-	10	A/ μs
I_{GM}	peak gate current		-	1	A
P_{GM}	peak gate power		-	5	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	+150	°C
T_j	junction temperature		-	125	°C

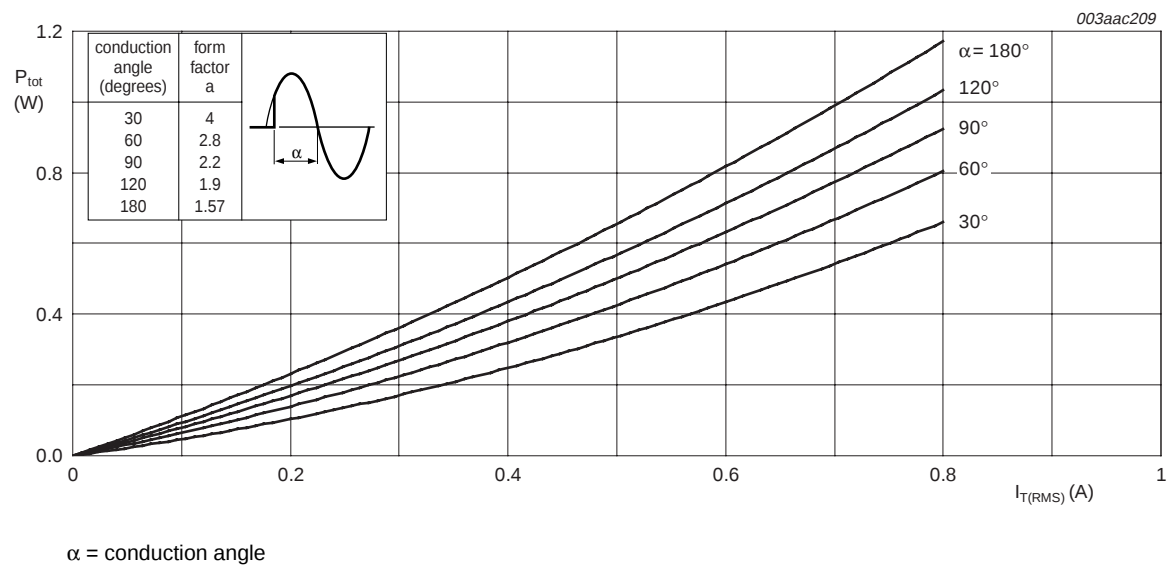


Fig 1. Total power dissipation as a function of RMS on-state current; maximum values

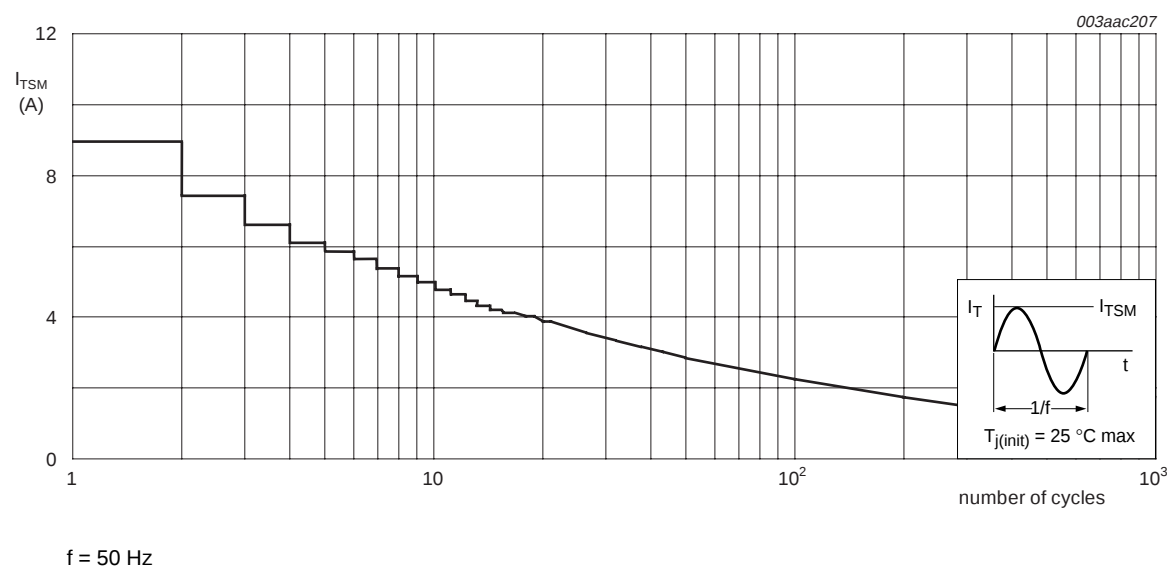


Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

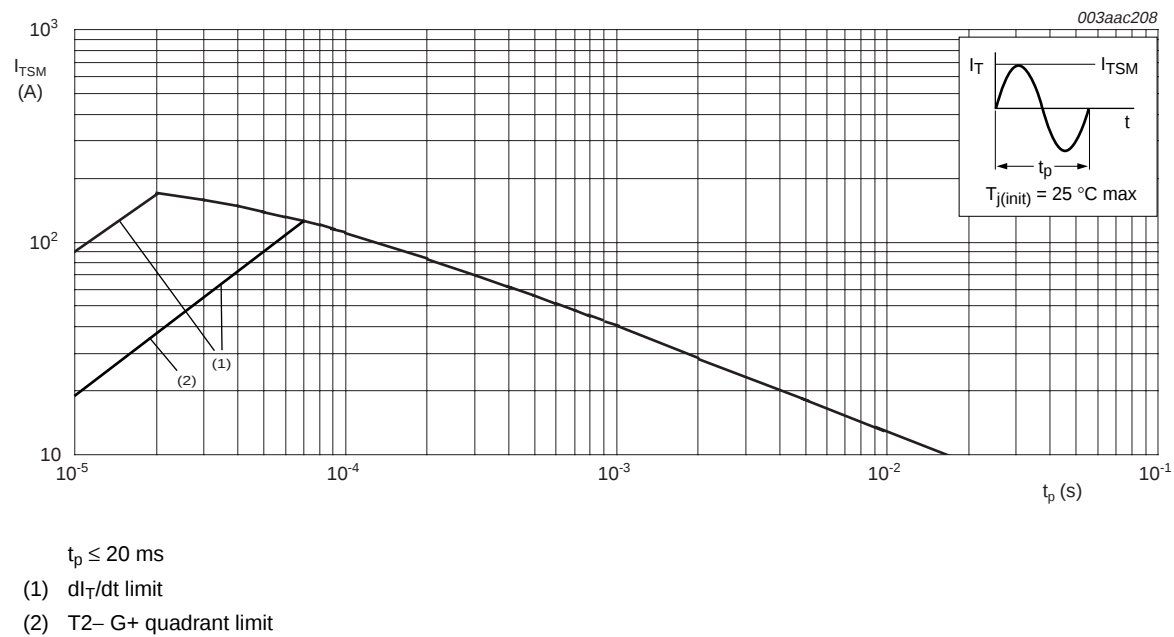


Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values

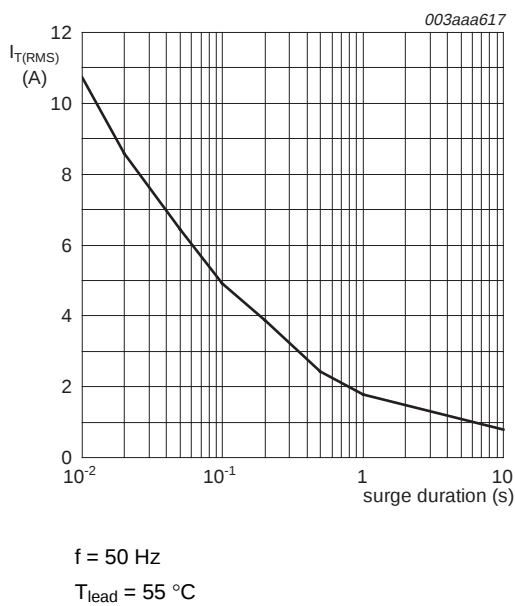


Fig 4. RMS on-state current as a function of surge duration; maximum values

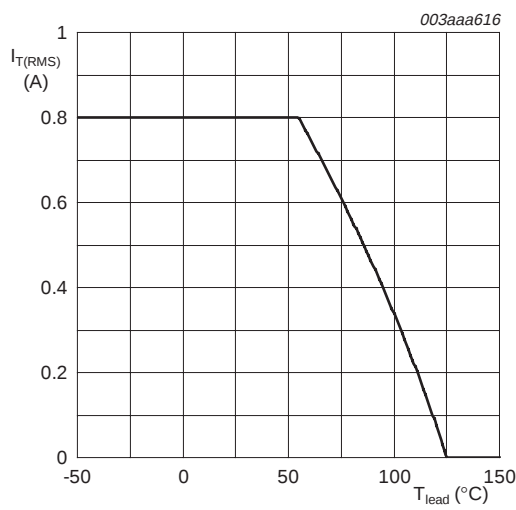
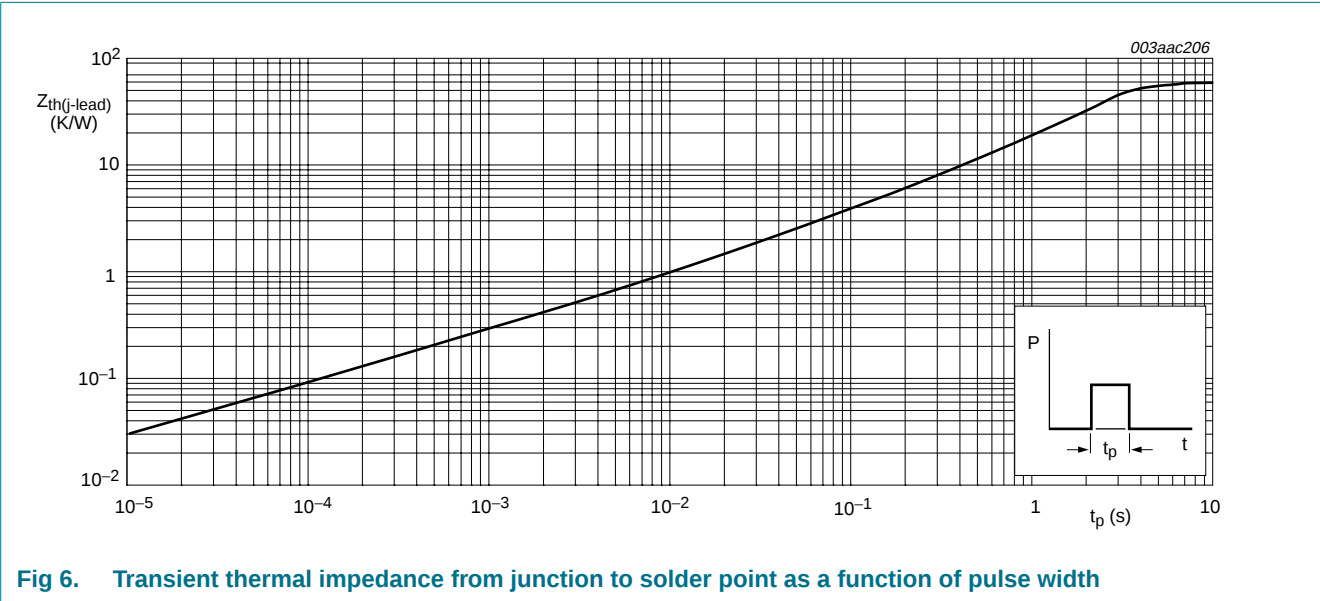


Fig 5. RMS on-state current as a function of lead temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	full cycle; printed-circuit board mounted; lead length 4 mm; see Figure 6	-	150	-	K/W

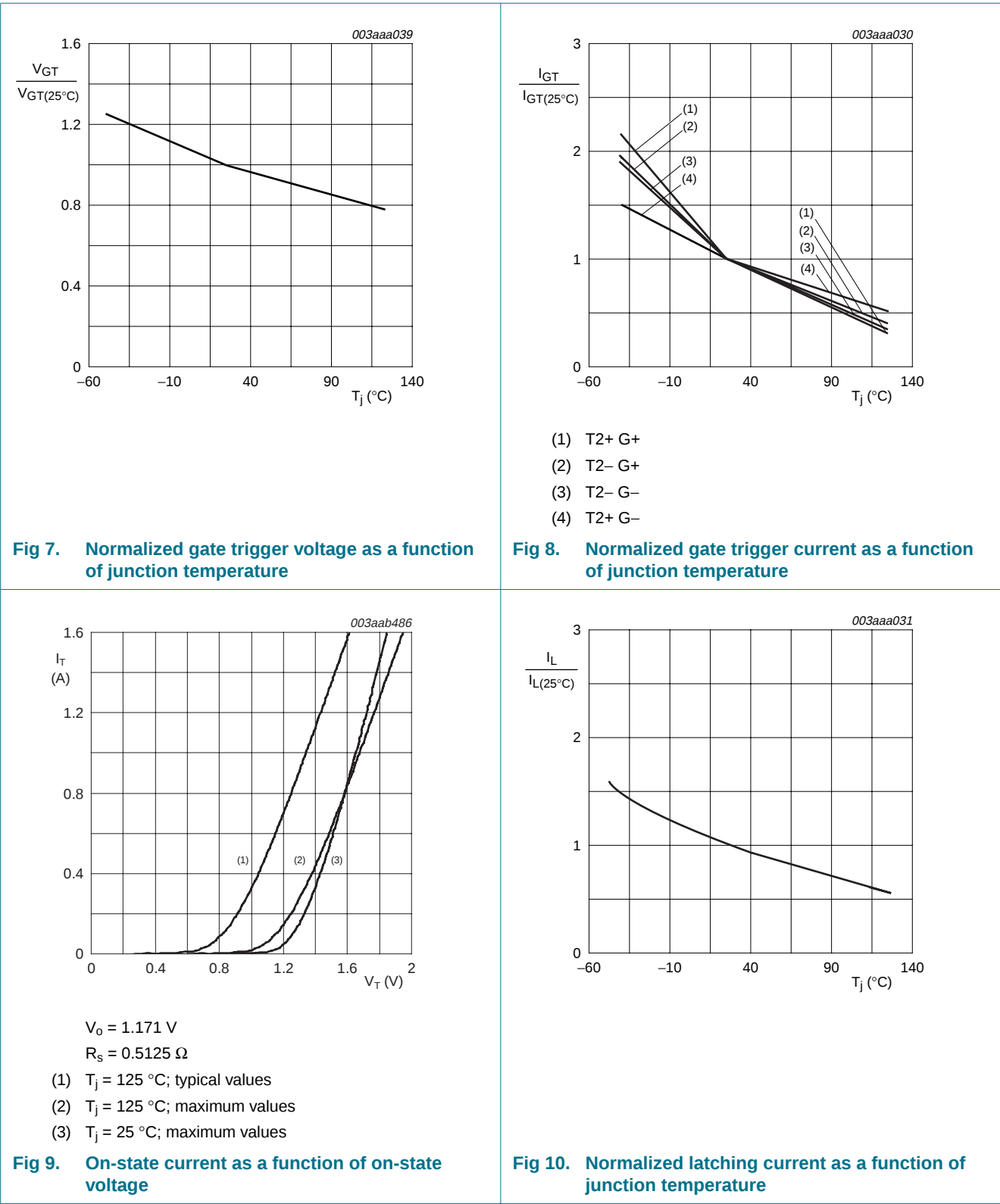


6. Characteristics

Table 5. Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; see Figure 8				
		T2+ G+	-	1	5	mA
		T2+ G-	-	2	5	mA
		T2- G-	-	2	5	mA
		T2- G+	-	4	7	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; see Figure 10				
		T2+ G+	-	1	10	mA
		T2+ G-	-	5	10	mA
		T2- G-	-	1	10	mA
		T2- G+	-	2	10	mA
I_H	holding current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; see Figure 11	-	1	10	mA
V_T	on-state voltage	$I_T = 0.85\text{ A}$; see Figure 9	-	1.35	1.6	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; see Figure 7	-	0.9	2	V
		$V_D = V_{DRM}$; $I_T = 0.1\text{ A}$; $T_j = 110\text{ °C}$	0.1	0.7	-	V
I_D	off-state current	$V_D = V_{DRM(max)}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 0.67 \times V_{DRM(max)}$; $T_j = 110\text{ °C}$; exponential waveform; gate open circuit	30	45	-	V/ μ s
dV_{com}/dt	rate of change of commutating voltage	$V_{DM} = V_{DRM(max)}$; $T_j = 50\text{ °C}$; $I_{TM} = 0.84\text{ A}$; $dI_{com}/dt = 0.3\text{ A/ms}$	-	5	-	V/ μ s
t_{gt}	gate-controlled turn-on time	$I_{TM} = 1\text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 25\text{ mA}$; $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μ s



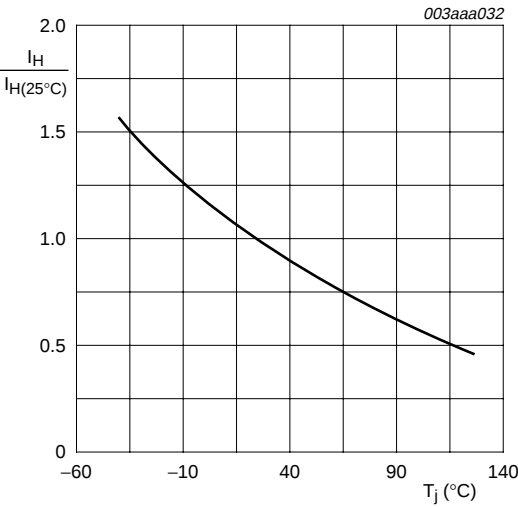


Fig 11. Normalized holding current as a function of junction temperature

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

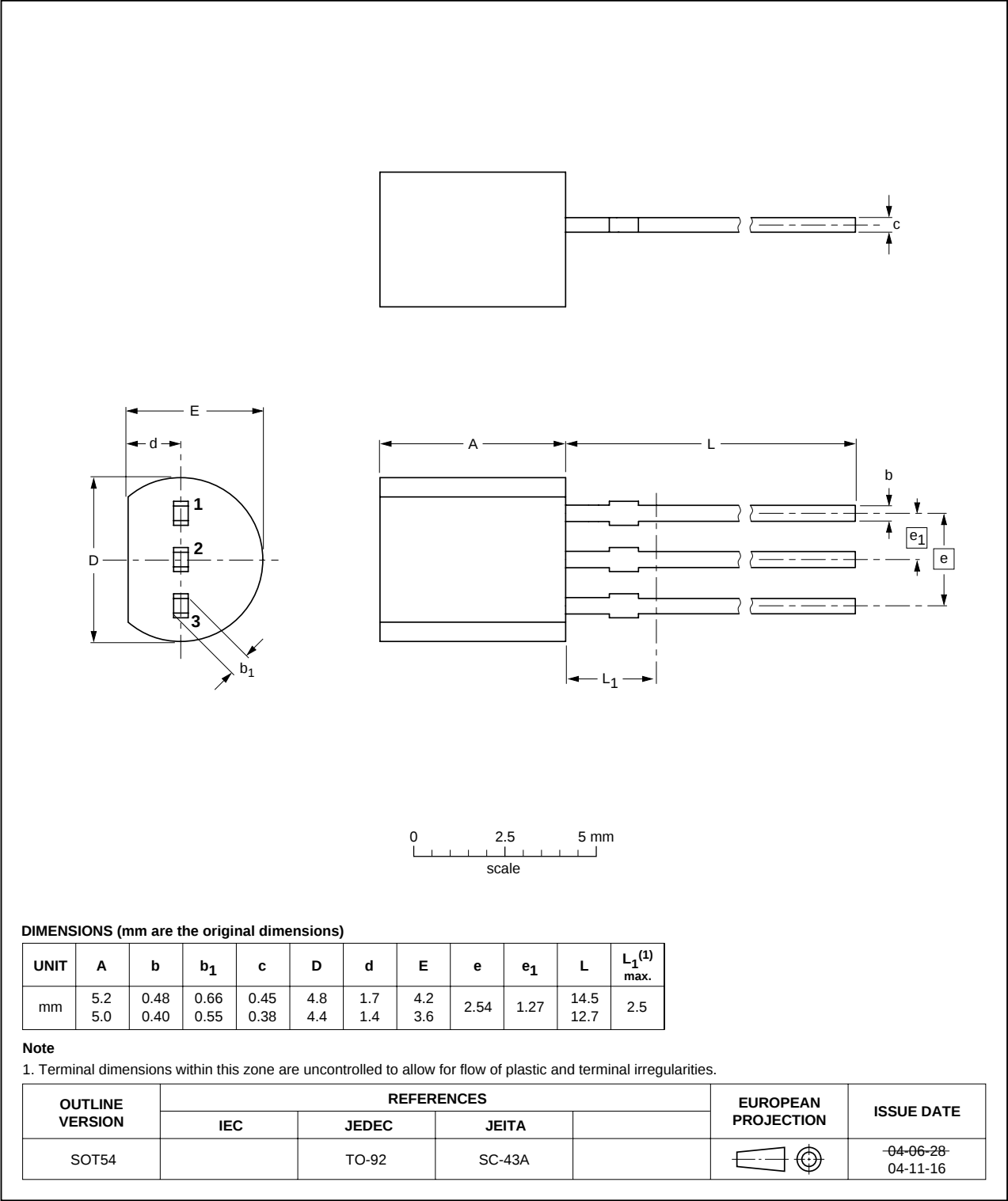


Fig 12. Package outline SOT54 (TO-92)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT1308_SER_D_1	20080226	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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