LCD Segment Driver series

# Standard function Segment Drivers

## BU9795AKV, BU9795AFV, BU9795AGUW

No.09044EBT01

### ●Description

This is LCD segment driver for 140 segment type display. There is a lineup which is suitable for multi function display and is integrated display RAM and power supply circuit for LCD driving with 4 common output type: BU9795AKV/FV/GUW.

### ●Features

1) 3wire serial interface (CSB, SD, SCL)
2) Integrated RAM for display data (DDRAM) : 35 × 4bit (Max 140 Segment)
3) LCD driving port: 4 Common output,
   Segment: 35output (BU9795AKV), 31output (BU9795AGUW), 27output (BU9795AFV)
4) Display duty: 1/4 duty
5) Integrated Buffer AMP for LCD driving power supply
6) 1/2bias, 1/3bias selectable
7) No external components
8) Low power/ Ultra low power consumption design: +2.5～5.5V

### ●Applications

Telephone, FAX, Portable equipment (POS, ECR, PDA etc.),
DSC, DVC, Car audio, Home electrical appliance, Meter equipment etc.

### ●Line up matrix

| Parameter | BU9795AKV | BU9795AFV | BU9795AGUW |
|---|---|---|---|
| Segment output | 35 | 27 | 31 |
| Common output | 4 | 4 | 4 |
| Package | VQFP48C | SSOP-B40 | VBGA048W040 |

●**Absolute maximum ratings** (Ta=25degree, VSS=0V)

| Parameter | Symbol | Limits | Unit | Remark |
|---|---|---|---|---|
| Power supply voltage1 | VDD | -0.5 ～ +7.0 | V | Power supply |
| Power supply voltage2 | VLCD | -0.5 ～ VDD | V | LCD drive voltage |
| Allowable loss | Pd | 0.6 | W | When use more than Ta=25°C, subtract 6mW per degree.(BU9795AKV) |
| | | 0.7 | W | When use more than Ta=25°C, subtract 7mW per degree (BU9795AFV) |
| | | 0.27 | W | When use more than Ta=25°C, subtract 2.7mW per degree (BU9795AGUW) |
| Input voltage range | VIN | -0.5 ～ VDD+0.5 | V | |
| Operational temperature range | Topr | -40 ～ +85 | degree | |
| Storage temperature range | Tstg | -55 ～ +125 | degree | |

*This product is not designed against radioactive ray.

●**Operating conditions** (Ta=25degree,VSS=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Power Supply voltage1 | VDD | 2.5 | - | 5.5 | V | Power supply |
| Power Supply voltage2 | VLCD | 0 | - | VDD-2.4 | V | LCD drive voltage |

* Please use VDD-VLCD≧2.4V condition.

**●Electrical characteristics**

DC Characteristics (VDD=2.5～5.5V, VSS=0V, Ta=-40～85degree, unless otherwise specified)

| Parameter | | Symbol | Limit | | | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | |
| “H” level input voltage | | VIH | 0.7VDD | - | VDD | V | |
| “L” level input voltage | | VIL | VSS | - | 0.3VDD | V | |
| “H” level input current | | IIH | - | - | 1 | uA | |
| “L” level input current | | IIL | -1 | - | - | uA | |
| LCD Driver on resistance | SEG | RON | - | 3.5 | - | kΩ | Iload=±10uA |
| | COM | RON | - | 3.5 | - | kΩ | |
| VLCD supply voltage | | VLCD | 0 | - | VDD -2.4 | V | VDD-VLCD≧2.5V |
| Standby current | | Ist | - | - | 5 | uA | Display off, Oscillator off |
| Power consumption 1 | | IDD1 | - | 12.5 | 30 | uA | VDD=3.3[V], Ta=25,<br>Power save mode1, FR=70Hz<br>1/3 bias, Frame inverse |
| Power consumption 2 | | IDD2 | - | 20 | 40 | uA | VDD=3.3[V], Ta=25,<br>Normal mode, FR=80Hz<br>1/3 bias, Line inverse |

● Oscillation Characteristics

(VDD=2.5～5.5V,VSS=0V, Ta=-40～85degree)

| Parameter | Symbol | Limit | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Frame frequency | $f_{CLK}$ | 56 | 80 | 104 | Hz | FR = 80Hz setting |
| Frame frequency1 | $f_{CLK1}$ | 70 | 80 | 90 | Hz | VDD=3.5V, 25degree |

● MPU interface Characteristics

(VDD=2.5V～5.5V,VSS=0V, Ta=-40～85degree)

| Parameter | Symbol | Limit | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Input rise time | tr | - | - | 80 | ns | |
| Input fall time | tf | - | - | 80 | ns | |
| SCL cycle time | tSCYC | 400 | - | - | ns | |
| “H” SCL pulse width | tSHW | 100 | - | - | ns | |
| “L” SCL pulse width | tSLW | 100 | - | - | ns | |
| SD setup time | tSDS | 20 | - | - | ns | |
| SD hold time | tSDH | 50 | - | - | ns | |
| CSB setup time | tCSS | 50 | - | - | ns | |
| CSB hold time | tCSH | 50 | - | - | ns | |
| “H” CSB pulse width | tCHW | 50 | - | - | ns | |

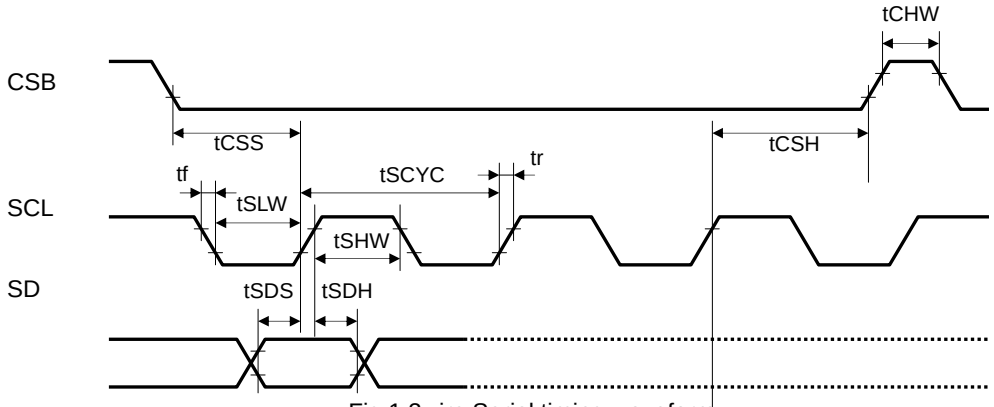



Fig.1 3wire Serial timing waveform

* BU9795AKV

● Block Diagram

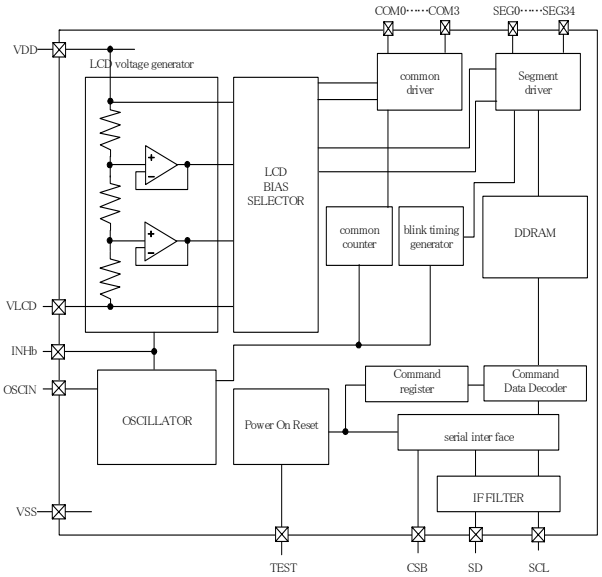



Fig. 2A
BU9795AKV Block diagram

● Pin Arrangement

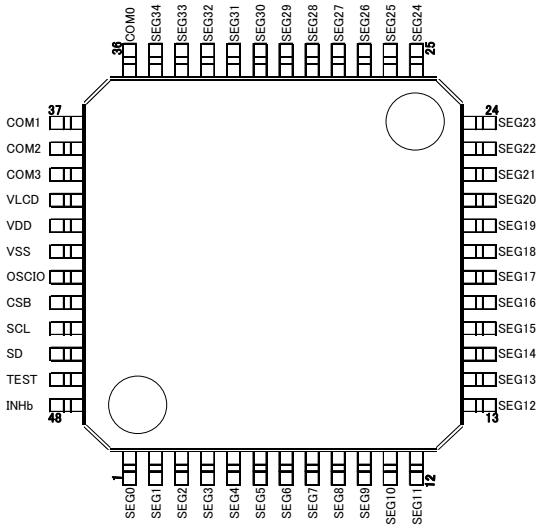



Fig. 3A
BU9795AKV Pin arrangement

● Terminal description

| Terminal | Terminal No. | I/O | Function |
|---|---|---|---|
| INHb | 48 | I | Input terminal for turn off display<br>H: turn on display L: turn off display |
| TEST | 47 | I | Test input (ROHM use only)<br>Must be connect to VSS |
| OSCIO | 43 | I | External clock input<br>Ex clock and Int clock can be changed by command.<br>Must be connect to VSS when use internal oscillation circuit. |
| SD | 46 | I | serial data input |
| SCL | 45 | I | serial data transfer clock |
| CSB | 44 | I | Chip select : “L” active |
| VSS | 42 | | GND |
| VDD | 41 | | Power supply |
| VLCD | 40 | | Power supply for LCD driving |
| SEG0-34 | 1-35 | O | SEGMENT output for LCD driving |
| COM0-3 | 36-39 | O | COMMON output for LCD driving |

* BU9795AFV

● Block Diagram

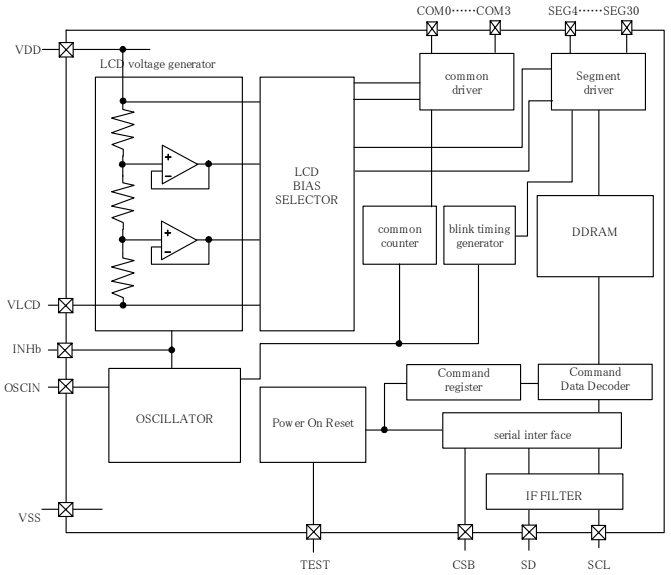



Fig. 2B
BU9795AFV Block diagram

● Pin Arrangement

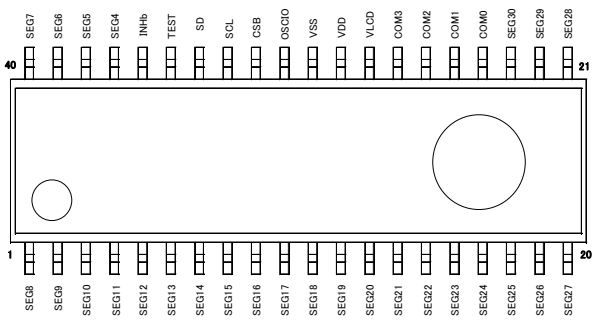



Fig. 3B
BU9795AFV Pin arrangement

● Terminal description

| Terminal | Terminal No. | I/O | Function |
|---|---|---|---|
| INHb | 36 | I | Input terminal for turn off display<br>H: turn on display L: turn off display |
| TEST | 35 | I | Test input (ROHM use only)<br>Must be connect to VSS |
| OSCIO | 31 | I | External clock input<br>Ex clock and Int clock can be changed by command.<br>Must be connect to VSS when use internal oscillation circuit. |
| SD | 34 | I | serial data input |
| SCL | 33 | I | serial data transfer clock |
| CSB | 32 | I | Chip select : “L” active |
| VSS | 30 | | GND |
| VDD | 29 | | Power supply |
| VLCD | 28 | I | Power supply for LCD driving |
| SEG4-30 | 1-23, 37-40 | O | SEGMENT output for LCD driving |
| COM0-3 | 24-27 | O | COMMON output for LCD driving |

* BU9795AGUW

● Block Diagram

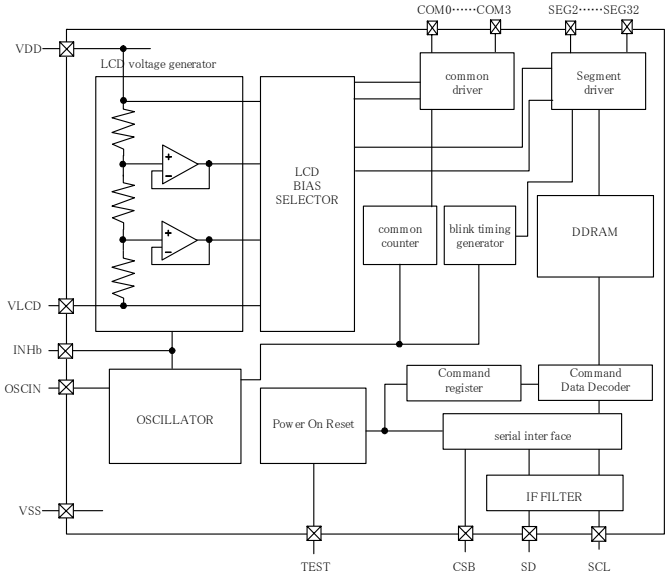



Fig. 2C
BU9795AGUW Block diagram

● Pin Arrangement

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| G | (NC) | SEG13 | SEG15 | SEG18 | SEG20 | SEG22 | (NC) |
| F | SEG11 | SEG12 | SEG16 | SEG17 | SEG21 | SEG23 | SEG24 |
| E | SEG9 | SEG10 | SEG14 | SEG19 | SEG25 | SEG27 | SEG26 |
| D | SEG7 | SEG6 | SEG8 | SEG5 | SEG30 | SEG28 | SEG29 |
| C | SEG4 | SEG3 | SEG2 | CSB | COM3 | SEG32 | SEG31 |
| B | | INHb | SD | VSS | VDD | COM1 | COM0 |
| A | (NC) | TEST2 | SCL | OSCIO | VLCD | COM2 | (NC) |

Fig. 3C
BU9795AGUW Pin arrangement

● Terminal description

| Terminal | I/O | Function |
|---|---|---|
| INHb | I | Input terminal for turn off display<br>H: turn on display L: turn off display |
| TEST | I | Test input (ROHM use only)<br>Must be connect to VSS |
| OSCIO | I | External clock input<br>Ex clock and Int clock can be changed by command.<br>Must be connect to VSS when use internal oscillation circuit. |
| SD | I | serial data input |
| SCL | I | serial data transfer clock |
| CSB | I | Chip select : “L” active |
| VSS | | GND |
| VDD | | Power supply |
| VLCD | I | Power supply for LCD driving |
| SEG2-32 | O | SEGMENT output for LCD driving |
| COM0-3 | O | COMMON output for LCD driving |

(Caution) About terminal number, please refer to above pin arrangement

●Command Description

D7 (MSB) is bit for command or data judgment.
Refer to Command and data transfer method.

C: 0: Next byte is RAM write data.
1: Next byte is command.

○ **Mode Set (MODE SET)**

| MSB D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 |
|---|---|---|---|---|---|---|---|
| C | 1 | 0 | * | P3 | P2 | * | * |

(*:Don't care)

Set display ON and OFF

| Setting | P3 | Reset initialize condition |
|---|---|---|
| Display OFF (DISPOFF) | 0 | ○ |
| Display ON (DISPON) | 1 | |

Set bias level

| Setting | P2 | Reset initialize condition |
|---|---|---|
| 1/3 Bias | 0 | ○ |
| 1/2 Bias | 1 | |

○ **Address set (ADSET)**

| MSB D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 |
|---|---|---|---|---|---|---|---|
| C | 0 | 0 | P4 | P3 | P2 | P1 | P0 |

Address data is specified in P[4:0] and P2 (ICSET command) as follows.

| | MSB | | | LSB |
|---|---|---|---|---|
| Internal register | Address [5] | Address [4] | ・・・ | Address [0] |
| Bit of each command | ICSET [P2] | ADSET [P4] | ・・・ | ADSET [P0] |

○ **Display control (DISCTL)**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 0 | 1 | P4 | P3 | P2 | P1 | P0 |

Set Frame frequency

| Setting | P4 | P3 | Reset initialize condition |
|---|---|---|---|
| 80Hz | 0 | 0 | ○ |
| 71Hz | 0 | 1 | |
| 64Hz | 1 | 0 | |
| 53Hz | 1 | 1 | |

Set LCD drive waveform

| Setting | P2 | Reset initialize condition |
|---|---|---|
| Line inversion | 0 | ○ |
| Frame inversion | 1 | |

Set Power save mode

| Setting | P1 | P0 | Reset initialize condition |
|---|---|---|---|
| Power save mode 1 | 0 | 0 | |
| Power save mode 2 | 0 | 1 | |
| Normal mode | 1 | 0 | ○ |
| High power mode | 1 | 1 | |

∗ VDD-VLCD>=3.0V is required for High power mode.

○ **Set IC Operation (ICSET)**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 1 | 1 | 0 | 1 | P2 | P1 | P0 |

P2: MSB data of DDRAM address. Please refer to “ADSET” command.

| Setting | P2 | Reset initialize condition |
|---|---|---|
| Address MSB‘0’ | 0 | ○ |
| Address MSB‘1’ | 1 | |

Set Software Reset condition

| Setting | P1 |
|---|---|
| No operation | 0 |
| Software Reset | 1 |

Switch between internal clock and external clock.

| Setting | P0 | Reset initialize condition |
|---|---|---|
| Internal clock | 0 | ○ |
| External clock input | 1 | |

○ **Blink control (BLKCTL)**

MSB LSB

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C | 1 | 1 | 1 | 0 | * | P1 | P0 |

Set blink condition

| Setting | P1 | P0 | Reset initialize condition |
|---|---|---|---|
| OFF | 0 | 0 | ○ |
| 0.5 Hz | 0 | 1 | |
| 1 Hz | 1 | 0 | |
| 2 Hz | 1 | 1 | |

○ **All pixel control (APCTL)**

MSB LSB

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C | 1 | 1 | 1 | 1 | 1 | P1 | P0 |

All display set ON. OFF

| Setting | P1 | Reset initialize condition |
|---|---|---|
| Normal | 0 | ○ |
| All pixel ON | 1 | |

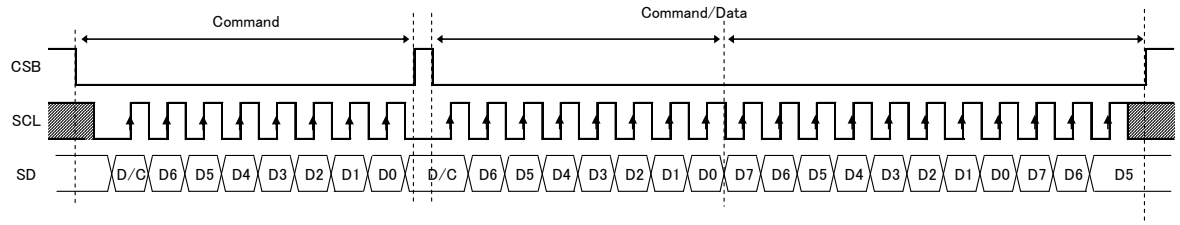
| Setting | P0 | Reset initialize condition |
|---|---|---|
| Normal | 0 | ○ |
| All pixel OFF | 1 | |

●Function description

○ Command and data transfer method

○ 3-SPI (3wire Serial interface)

This device is controlled by 3-wire signal (CSB, SCL, and SD).
First, Interface counter is initialized with CSB="H",
and CSB="L" makes SD and SCL input enable.
The protocol of 3-SPI transfer is as follows.
Each command starts with Command or Data judgment bit (D/C) as MSB data,
and continuously in order of D6 to D0 are followed after CSB ="L".
(Internal data is latched at the rising edge of SCL, it converted to 8bits parallel data
at the falling edge of 8th CLK.)



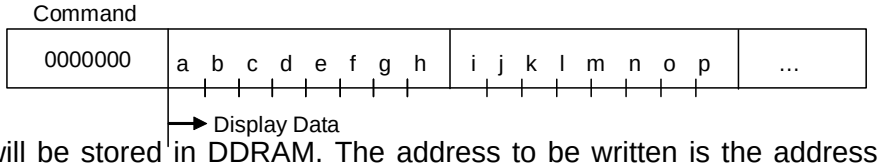

D/C = "H" : Command D/C = "L" : Data

Fig. 4 3-SPI Command/Data transfer format

○Write display data and transfer method

* BU9795AKV

This LSI have Display Data RAM (DDRAM) of 35×4=140bit.
The relationship between data input and display data, DDRAM data and address are as follows.




8 bit data will be stored in DDRAM. The address to be written is the address specified by Address set command, and the address is automatically incremented in every 4bit data.
Data can be continuously written in DDRAM by transmitting Data continuously.
(When RAM data is written successively after writing RAM data to 22h (SEG34), the address is returned to 00h (SEG0) by the auto-increment function.

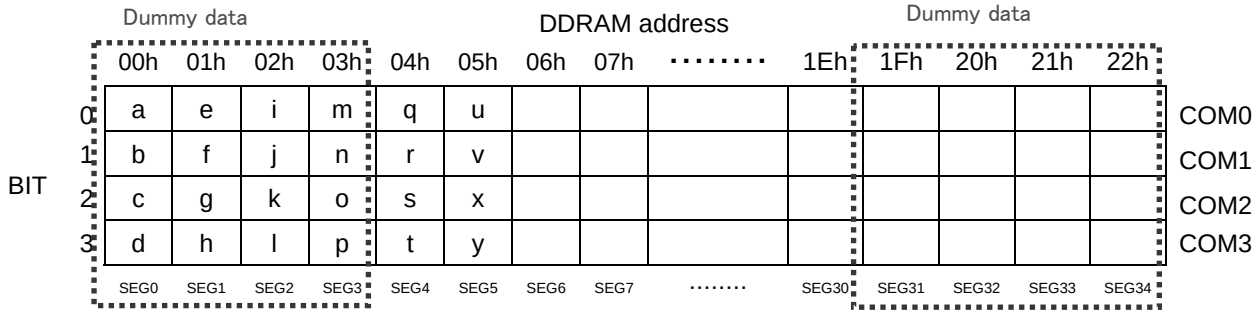
DDRAM address

| BIT | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | ····· | 1Eh | 1Fh | 20h | 21h | 22h | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | a | e | i | m | q | u | | | | | | | | | COM0 |
| 1 | b | f | j | n | r | v | | | | | | | | | COM1 |
| 2 | c | g | k | o | s | x | | | | | | | | | COM2 |
| 3 | d | h | l | p | t | y | | | | | | | | | COM3 |
| | SEG0 | SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | SEG6 | SEG7 | ····· | SEG30 | SEG31 | SEG32 | SEG33 | SEG34 | |

As data transfer to DDRAM happens every 4bit data, it will be cancelled if it changes CSB="L"→"H" before 4bits data transfer.

* BU9795AFV

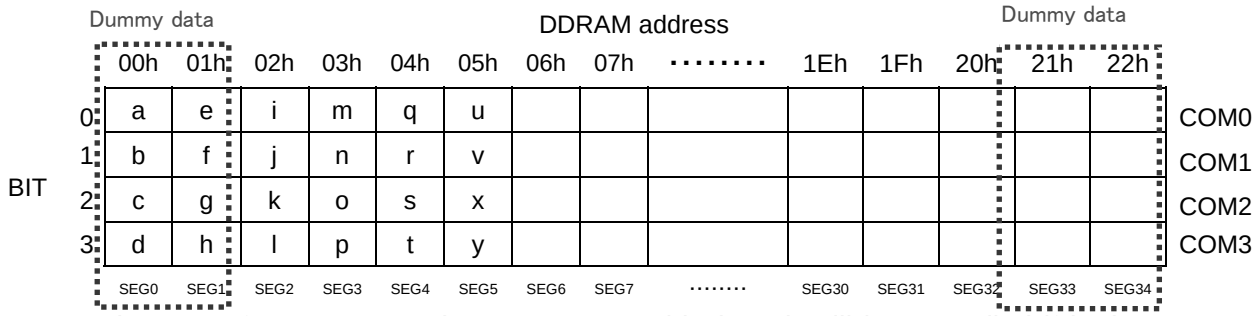
As SEG0, SEG1, SEG2, SEG3, SEG31, SEG32, SEG33, SEG34 are not output, these address will be dummy address.




As data transfer to DDRAM happens every 4bit data, it will be cancelled if it changes CSB="L"→"H" before 4bits data transfer.

* BU9795AGUW

As SEG0, SEG1, SEG33, SEG34 are not output, these address will be dummy address.




As data transfer to DDRAM happens every 4bit data, it will be cancelled if it changes CSB="L"→"H" before 4bits data transfer.

○ Reset (initial) condition

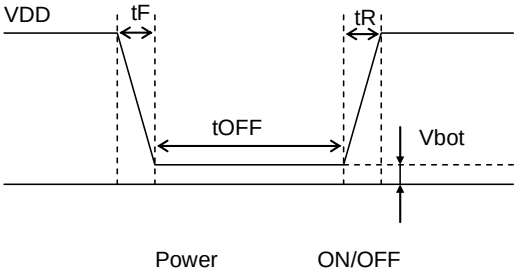
Initial condition after execute Software Reset is as follows.

- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).
- Refer to Command Description about initialize value of register.

## ● Cautions of Power-On condition

This LSI has “P.O.R” (Power-On Reset) circuit and Software Reset function.
Please keep the following recommended Power-On conditions in order to power up properly.

1. Please set power up conditions to meet the recommended tR, tF, tOFF, and Vbot spec below in order to ensure P.O.R operation.




Recommendation condition of tR,tF,tOFF,Vbot

| tR | tF | tOFF | Vbot |
|---|---|---|---|
| Less than 1ms | Less than 1ms | More than 150ms | Less than 0.1V |

Fig. 5 Power on-off waveform

2. If it is difficult to meet above conditions, execute the following sequence after Power-On. Because it doesn’t accept the command in power off, it is necessary to care that correspondence by software reset doesn’t become alternative to POR function completely.

(1) CSB=”L”→”H” condition

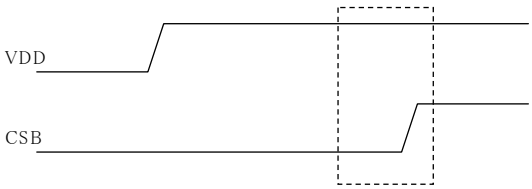



Fig. 6 CSB Timing

(2) After CSB”H”→“L”, execute Software Reset (ICSET command).

● IO Circuit (BU9795AKV /AFV /AGUW)

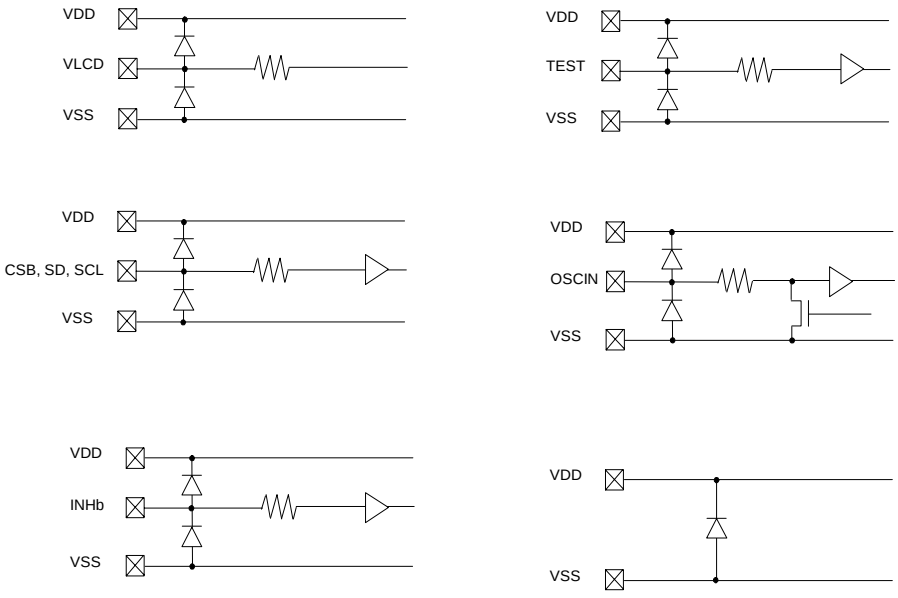
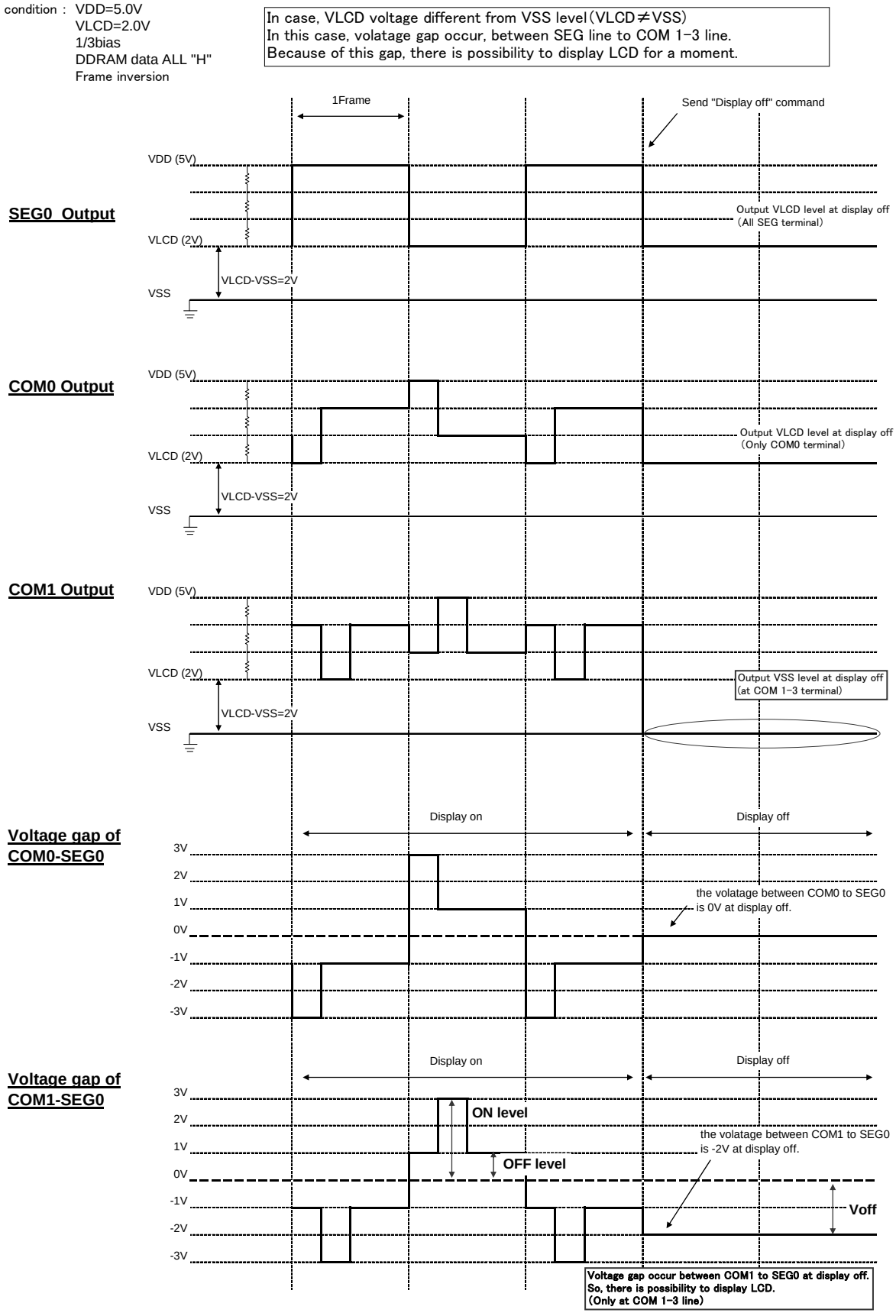



Fig. 7 IO circuit

● Notes for Application (BU9795AKV /BU9795AFV / BU9795AGUW)

In case, BU9795AKV/ BU9795AFV/ BU9795AGUW used at VLCD≠VSS, voltage gap occur between SEG line to COM1 – 3 line at Display off state. Because of this voltage gap, there is possibility to display LCD for a moment.

To avoid this phenomenon, please decide VDD and VLCD level to satisfy Voff voltage lower than OFF level (OFF level = 1V at the example explained below).



## ●Notes for use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, or the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

(13) Rush current
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special condition to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

●**Ordering part number**

| B | D | 9 | 7 | 9 | 5 | A | K | V | - | E | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|

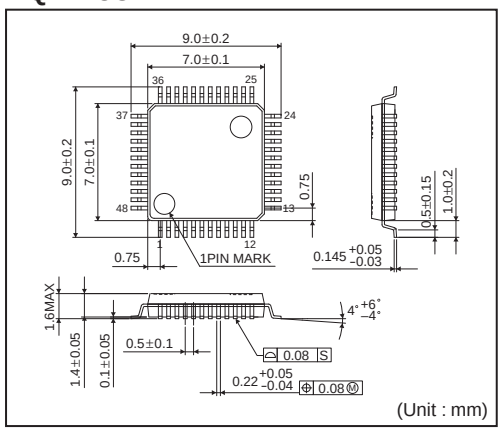
Part No. (BD)

Part No. (9795A)

Package
KV: VQFP48C
FV: SSOP-B40
GUW:
VBGA048W040

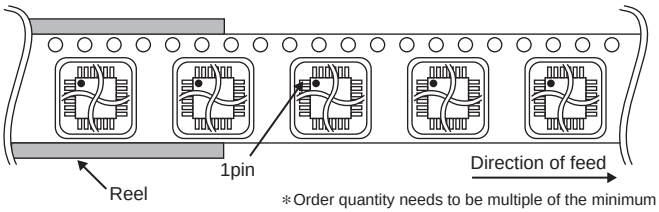
Packaging and forming specification
E2: Embossed tape and reel

**VQFP48C**



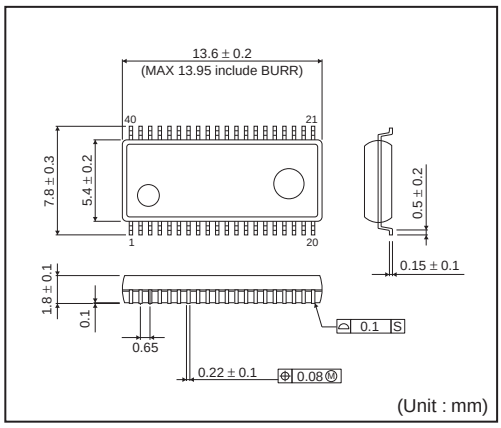

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 1500pcs |
| Direction of feed | E2 ( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



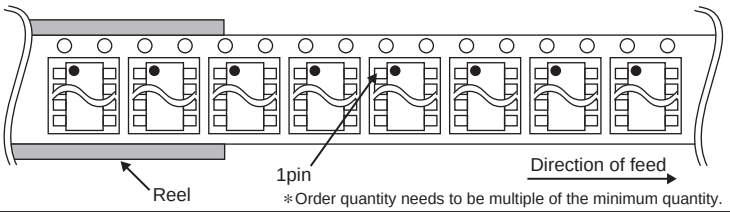

∗Order quantity needs to be multiple of the minimum quantity.

**SSOP-B40**



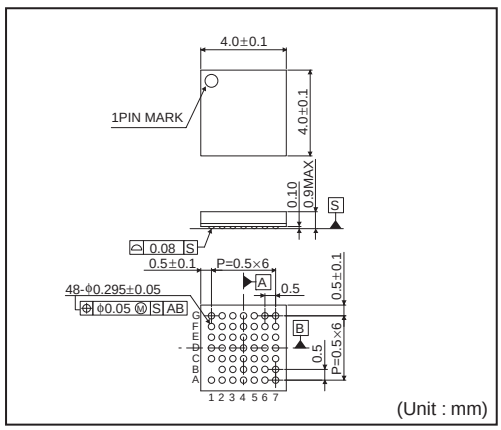

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2000pcs |
| Direction of feed | E2 ( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



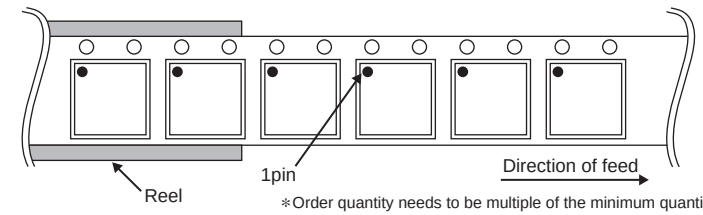

∗Order quantity needs to be multiple of the minimum quantity.

**VBGA048W040**




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape (with dry pack) |
| Quantity | 2500pcs |
| Direction of feed | E2 ( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.

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