Pb Free ROHM Electronic Components

RoHS Directive Compliance

Memory for Plug & Play

I²C BUS 3Ports for HDMI Port Serial EEPROM

BU9883FV-W

● Description

BU9883FV-W is for DDC 3 ports, 2K × 8 bit array 3 BANK EEPROM.

●Features

- There are 3 BANKs, 1 BANK compose of 256 word address × 8 bit EEPROM
- There are 3 DDC interface channels, and each channel can access each BANK independently from other ports.
- 2K bit X 3 BANK memory bits can be accessed from write port (Port0).
- Operate voltage (3.0V～5.5V)
- Built in diode for power supply from HDMI ports and system.
- Automatic erase
- 8 byte page write mode
- Low power consumption
  - Active (5.0V) : 1.2mA (Typ.)
  - Standby (5.0V) : 100μA(Max.)
- DATA security
- Write Protect pin can switch write port
- Inhibit to WRITE at low VCC
- Pin package ------ SSOP16pin
- Endurance : 1,000,000 erase/write cycles
- Data retention : 40 years
- Filtered inputs in all SCL・SDA for noise suppression
- Shipment data all address FFh

●Absolute maximum rating (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.3～6.5	V
Power Dissipation	Pd	400 *1	mW
Storage Temperature	Tstg	-65 ～ 125	℃
Operating Temperature	Topr	-40 ～ 85	℃
Terminal Voltage	—	-0.3～Vcc＋0.3 *1	V

*1 Degradation is done at 3.0mW/℃ for operation above 25℃

*2 The Max value of terminal voltage is not over 6.5V

●EEPROM recommended operating condition

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	3.0～5.5	V
Input Voltage	VIN	0 ～ Vcc0～3	

●Memory cell characteristics(Ta=25℃, Vcc0～3 = 3.0～5.5V)

Parameter	Specification			Unit
	Min.	Typ.	Max.	
Write/Erase Cycle *1	1,000,000	—	—	Cycles
Data Retention *1	40	—	—	Years

*1:Not 100% TESTED

●Input/output capacity (Ta=25℃, Frequency=5MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SDA pins (SDA0,1,2,3) *1	Cin	—	7	—	pF
SCL pins (SCL0,1,2,3) *1	Cin2	—	7	—	pF

*1:Not 100% TESTED

●EEPROM DC operating characteristics (Unless otherwise specified, Ta=-40～85℃, Vcc0～3 = 3.0～5.5V)

Parameter	Symbol	Specification			Unit	Test condition
		Min.	Typ.	Max.		
"H" Input Voltage0	VIH0	0.7×Vcc0	—	Vcc0+0.5	V	3.0≦Vcc0≦5.5V (SCL0, SDA0)
"L" Input Voltage0	VIL0	-0.3	—	0.3×Vcc0	V	3.0≦Vcc0≦5.5V (SCL0, SDA0)
"H" Input Voltage1	VIH1	0.7×Vcc1	—	Vcc1+0.5	V	3.0≦Vcc1≦5.5V (SCL1, SDA1)
"L" Input Voltage1	VIL1	-0.3	—	0.3×Vcc1	V	3.0≦Vcc1≦5.5V (SCL1, SDA1)
"H" Input Voltage2	VIH2	0.7×Vcc2	—	Vcc2+0.5	V	3.0≦Vcc2≦5.5V (SCL2, SDA2)
"L" Input Voltage2	VIL2	-0.3	—	0.3×Vcc2	V	3.0≦Vcc2≦5.5V (SCL2, SDA2)
"H" Input Voltage3	VIH3	0.7×Vcc3	—	Vcc3+0.5	V	3.0≦Vcc3≦5.5V (SCL3, SDA3)
"H" Input Voltage3	VIL3	-0.3	—	0.3×Vcc3	V	3.0≦Vcc3≦5.5V (SCL3, SDA3)
"L" Output Voltage0	VOL0	—	—	0.4	V	IOL=3.0mA , 3.0V≦Vcc0≦5.5V (SDA0)
"L" Output Voltage1	VOL1	—	—	0.4	V	IOL=3.0mA , 3.0V≦Vcc1≦5.5V (SDA1)
"L" Output Voltage2	VOL2	—	—	0.4	V	IOL=3.0mA , 3.0V≦Vcc2≦5.5V (SDA2)
"L" Output Voltage3	VOL3	—	—	0.4	V	IOL=3.0mA , 3.0V≦Vcc3≦5.5V (SDA3)
WP "H" Input Voltage	VIH4	0.7×Vcc0	—	Vcc0+0.3	V	3.0≦Vcc0≦5.5V (WPB)
WP "L" Input Voltage	VIL4	-0.3	—	0.3×Vcc	V	3.0≦Vcc0≦5.5V (WPB)
Input Leakage Current0	ILI0	-1	—	1	μA	VIN=0～5.5V (SCL0～3)
Input Leakage Current1	ILI1	55	110	230	μA	WPB=5.5V , Vcc=5.5V
Output Leakage Current0	ILO0	-1	—	1	μA	VOUT=0～5.5 (SDA0～3)
Operating Current	ICC1	—	—	2.0	mA	Vcc0=5.5V, fSCL=400kHz, tWR=5ms Byte Write, Page Write
	ICC2	—	—	1.0	mA	Vcc0～3=5.5V, fSCL=400kHz Random Read, Current Read, Sequential Read, (each port operation)
Standby Current	ISB0	—	—	100	μA	Vcc～0=5.5V, SDA0～3=SCL0～3=5.5V, WPB=GND
Standby Current	ISB1	—	—	100	μA	Vcc1=5.5V, SDA0～3=SCL0～3=5.5V, WPB=GND
Standby Current	ISB2	—	—	100	μA	Vcc2=5.5V, SDA0～3=SCL0～3=5.5V, WPB=GND
Standby Current	ISB3	—	—	100	μA	Vcc3=5.5V, SDA0～3=SCL0～3=5.5V, WPB=GND

○This product is not designed for protection against radioactive rays.

●EEPROM AC operating characteristics (Ta=-40～85℃, Vcc0～3 = 3.0～5.5V)

Parameter	Symbol	3.0≦Vcc0～3≦5.5V			Unit
		Min.	Typ.	Max.	Min.
Clock Frequency	fSCL	—	—	400	kHz
Data Clock High Period	tHIGH	0.6	—	—	μs
Data Clock Low Period	tLOW	1.2	—	—	μs
SDA0~3 and SCL0~3 Rise Time *1	tR	—	—	0.3	μs
SDA0~3 and SCL0~3 Fall Time *1	tF	—	—	0.3	μs
Start Condition Hold Time	tHD:STA	0.6	—	—	μs
Start Condition Setup Time	tSU:STA	0.6	—	—	μs
Input Data Hold Time	tHD:DAT	0	—	—	ns
Input Data Setup Time	tSU:DAT	100	—	—	ns
Output Data Delay Time	tPD	0.1	—	0.9	μs
Output Data Hold Time	tDH	0.1	—	—	μs
Stop Condition Setup Time	tSU:STO	0.6	—	—	μs
Bus Free Time	tBUF	1.2	—	—	μs
Write Cycle Time	tWR	—	—	5	ms
Noise Spike Width (SDA0~3 and SCL0~3)	tI	—	—	0.1	μs
WP Hold Time	tHD:WP	0	—	—	ns
WP Setup Time	tSU:WP	0.1	—	—	μs
WP valid time	tHIGH:WP	1.0	—	—	μs

*1 : Not 100% TESETED

●Synchronous data input/output timing

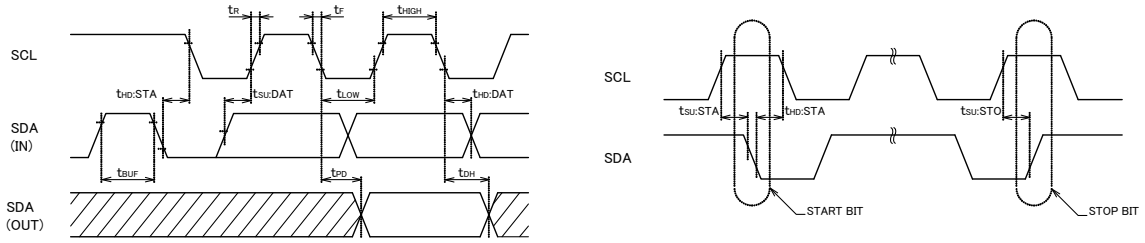


Fig.-1 SYNCHRONOUS DATA TIMING

○SDA data is latched into the chip at the rising edge of the SCL clock. (This is commoness in all port.)
○Output date toggles at the falling edge of the SCL clock. (This is commoness in all port.)

●Characteristic data (The following values are Typ. ones).

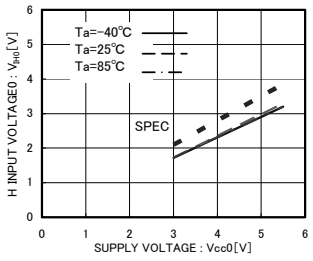


Fig.2 'H' Input Voltage0 V_{IH0}
(SCL0,SDA0)

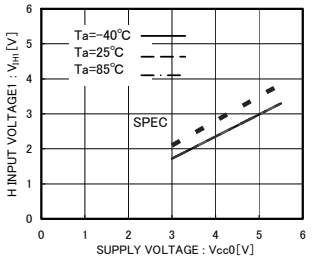


Fig.3 'H' Input Voltage1 V_{IH1}
(SCL1,SDA1)

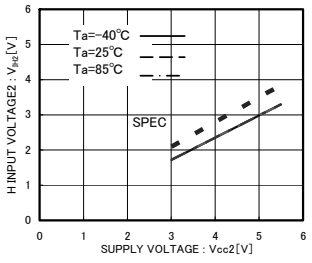


Fig.4 'H' Input Voltage2 V_{IH2}
(SCL2,SDA2)

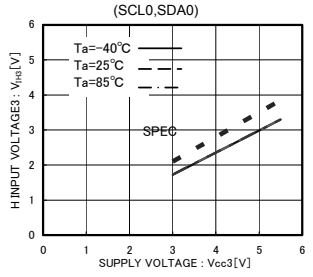


Fig.5 'H' Input Voltage3 V_{IH3}
(SCL3,SDA3)

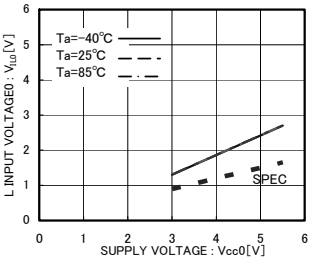


Fig.6 'L' Input Voltage0 V_{IL0}
(SCL0,SDA0)

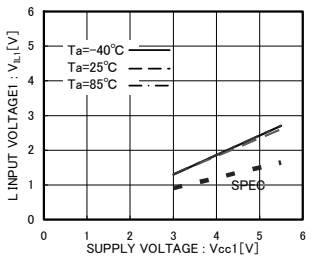


Fig.7 'L' Input Voltage1 V_{IL1}
(SCL1,SDA1)

●Characteristic data (The following values are Typ. ones).

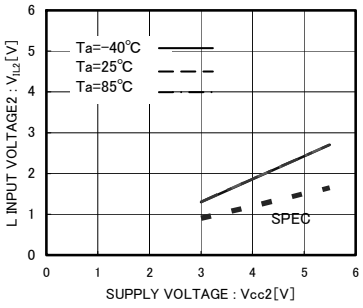


Fig.8 'L' Input Voltage2 V_{IL2} (SCL2,SDA2)

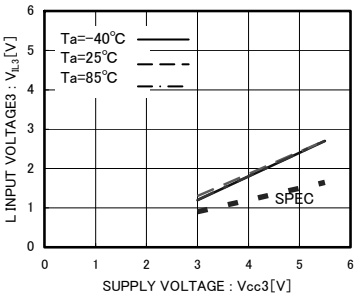


Fig.9 'L' Input Voltage3 V_{IL3} (SCL3,SDA3)

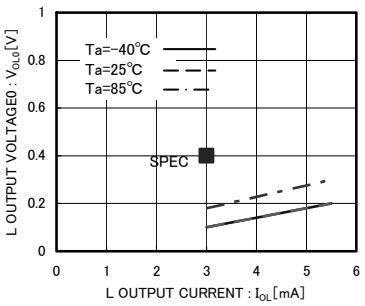


Fig.10 'L' Output Voltage0 V_{OL0}-I_{OL}(Vcc0=3.0V)

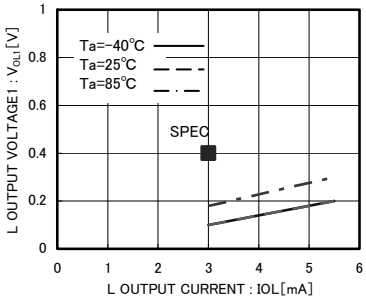


Fig.11 'L' Output Voltage1 V_{OL1}-I_{OL}(Vcc1=3.0V)(SDA1)

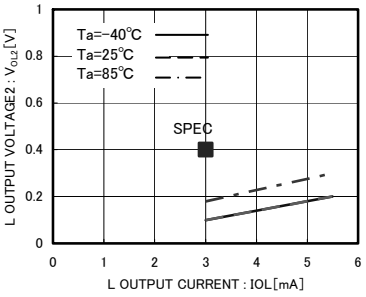


Fig.12 'L' Output Voltage2 V_{OL2}-I_{OL}(Vcc2=3.0V)(SDA2)

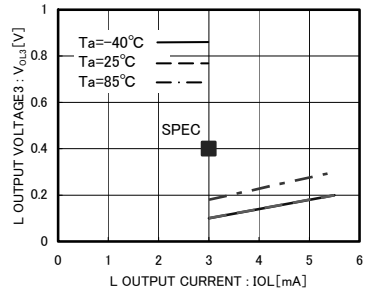


Fig.13 'L' Outnput Voltage3 V_{OL3}-I_{OL}(Vcc3=3.0V)(SDA3)

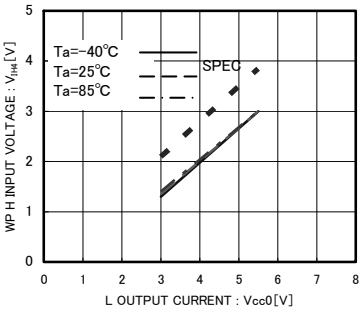


Fig.14 WP 'H' Input Voltage V_{IH4}

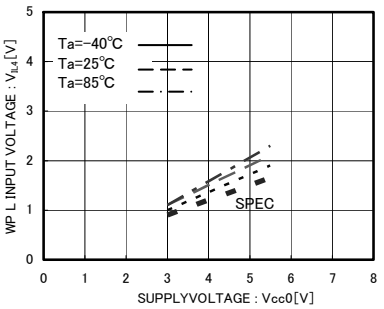


Fig.15 WP 'L'Input Voltage V_{IL4}

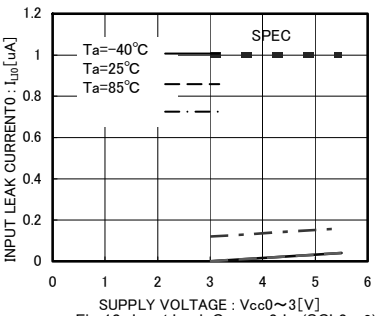


Fig.16 Input Leak Current0 I_{LI0}(SCL0～3)

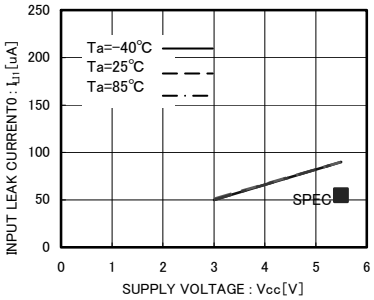


Fig.17 Input Leak Current1 I_{LI1}(WPB)

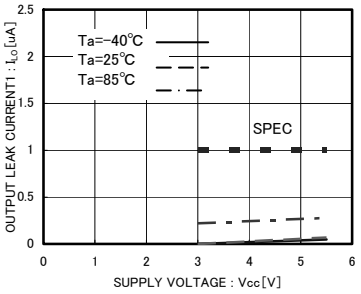


Fig.18 OUTPUT LEAK CURRENT I_{LO} (SDA0～3)

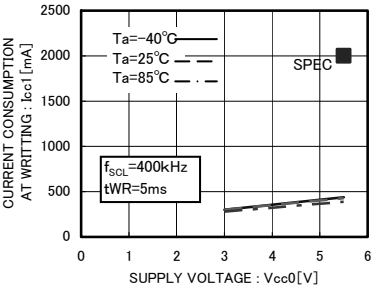


Fig.19 Current Consumption at Reading Icc1

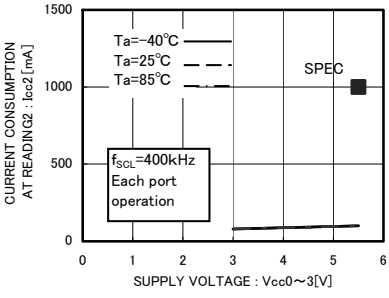


Fig.20 Current Consumption at Reading Icc2

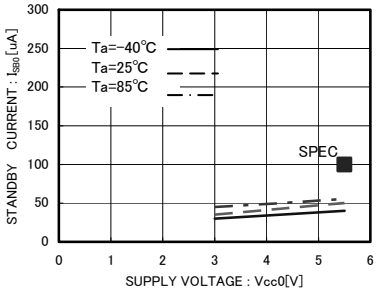


Fig.21 Standby Current I_{SB0}

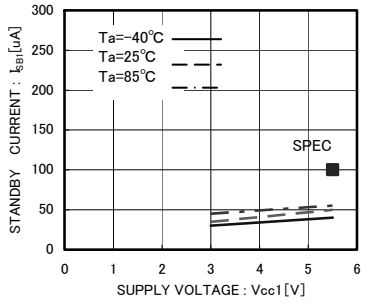


Fig.22 Standby Current I_{SB1}

●Characteristic data (The following values are Typ. ones).

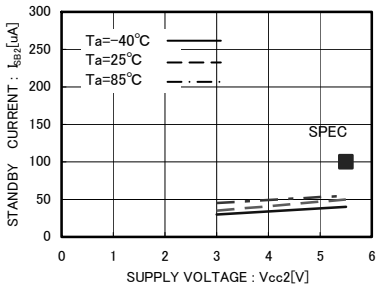


Fig.23 Standby Current2 I_{SB2}

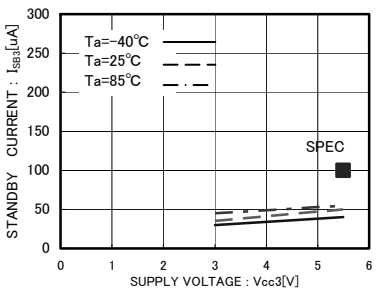


Fig.24 Standby Current I_{SB3}

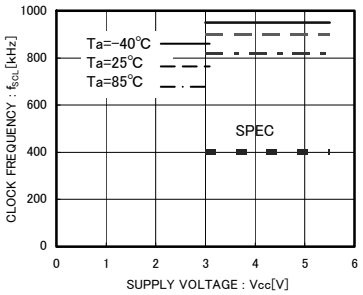


Fig.25 Clock Frequency f_{SCL}

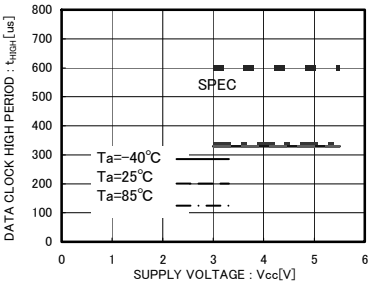


Fig.26 Data Clock High Period t_{HIGH}

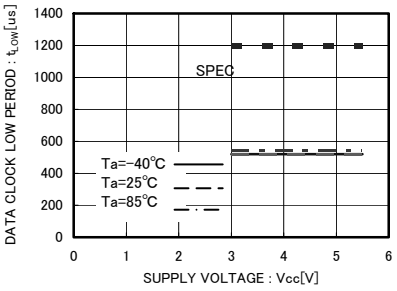


Fig.27 Data Clock Low Period t_{LOW}

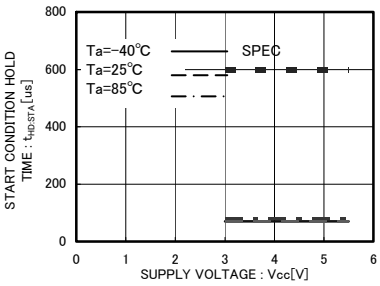


Fig.28 Start Condition Hold Time $t_{HD:STA}$

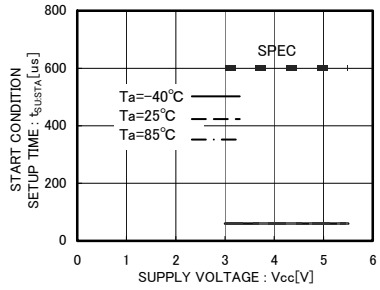


Fig.29 Start Condition Setup Time $t_{SU:STA}$

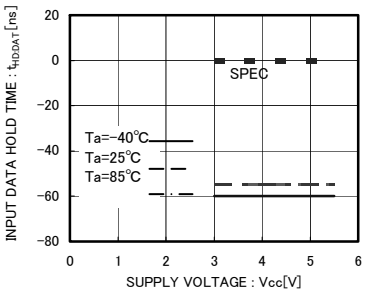


Fig.30 Input Data Hold Time $t_{HD:DAT}$

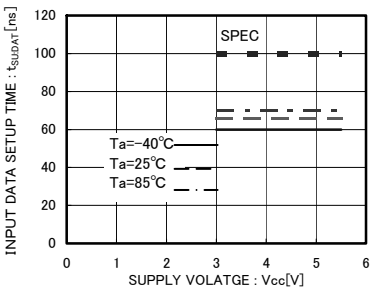


Fig.31 Input Data Setup Time $t_{SU:DAT}$

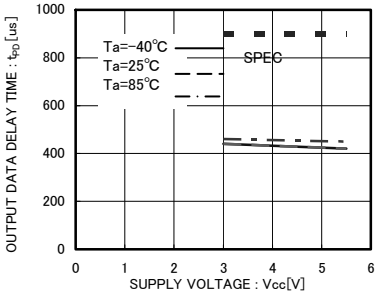


Fig.32 Output Data Delay Time t_{PD}

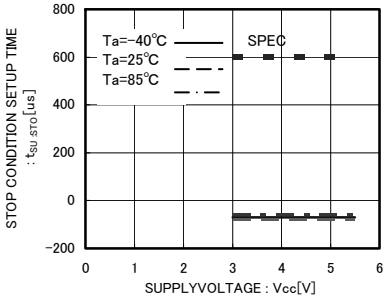


Fig.33 Stop Condition Setup Time $t_{SU:STO}$

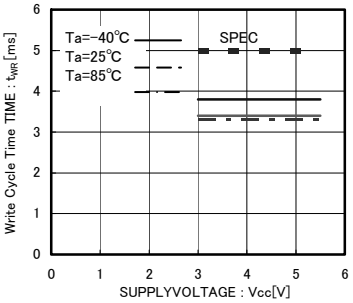


Fig.34 Write Cycle Time t_{WR}

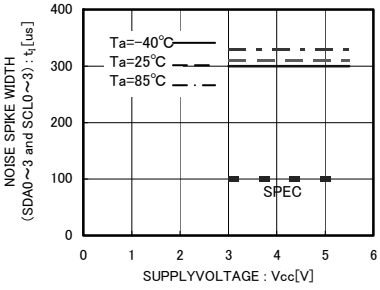


Fig.35 Noise Spike Width t_f
(SDA0～3 and SCL0～3)

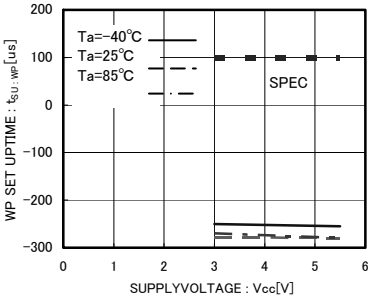


Fig.36 WP Setup Time $t_{SU:WP}$

●Pin configuration

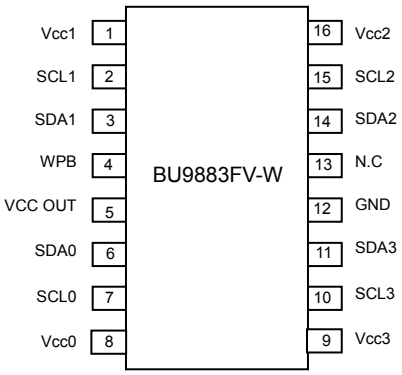


Fig.37 Pin configuration

●PIN NAME

PIN No.	PIN NAME	I/O	FUNCTIONS
1	Vcc1	-	Power Supply
2	SCL1	Input	Serial clock input
3	SDA1	Input / output	Slave and word address, Serial data input serial data output
4	WPB	Input	Write protect terminal（1 : Write enable, 0 : Write disable）
5	VCC OUT	-	Terminal of diode. Connect Bypass capacitor.
6	SDA0	Input / output	Slave and word address, Serial data input serial data output
7	SCL0	Input	Serial clock input
8	Vcc0	-	Power Supply
9	Vcc3	-	Power Supply
10	SCL3	Input	Serial clock input
11	SDA3	Input / output	Slave and word address, Serial data input serial data output
12	GND	-	Reference voltage of all input / output
13	N.C	-	Non connect terminal. Don’t connect each other.
14	SDA2	Input / output	Slave and word address, Serial data input serial data output
15	SCL2	Input	Serial clock input
16	Vcc2	-	Power Supply

●BLOCK DIAGRAM

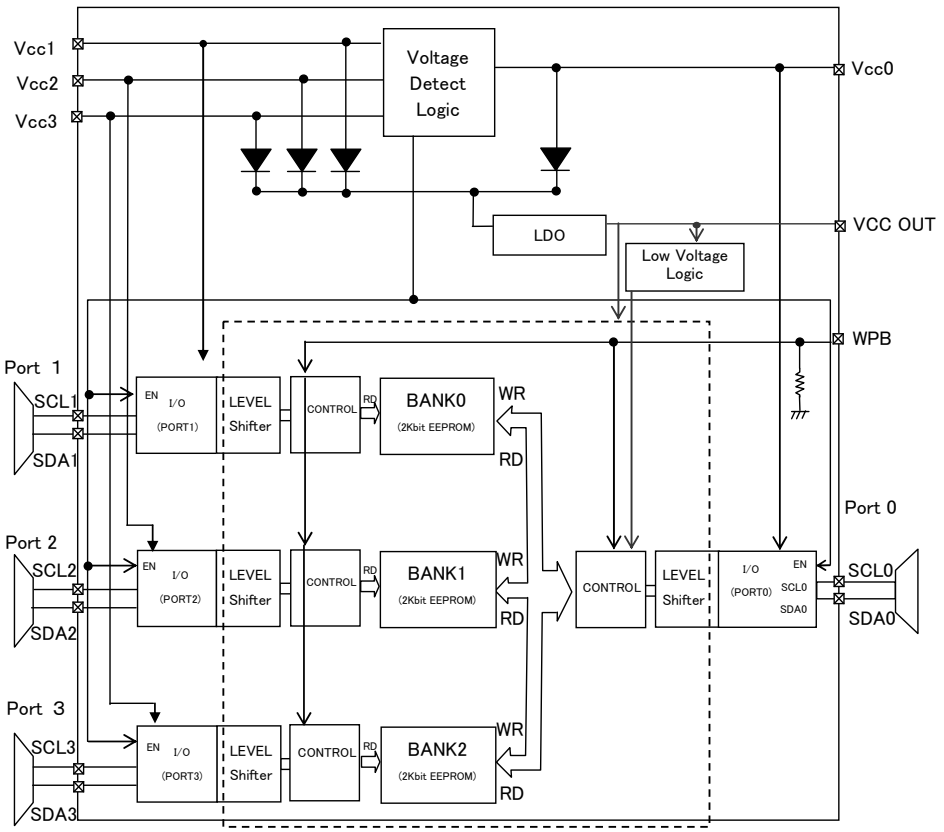


Fig.38　BLOCK DIAGRAM

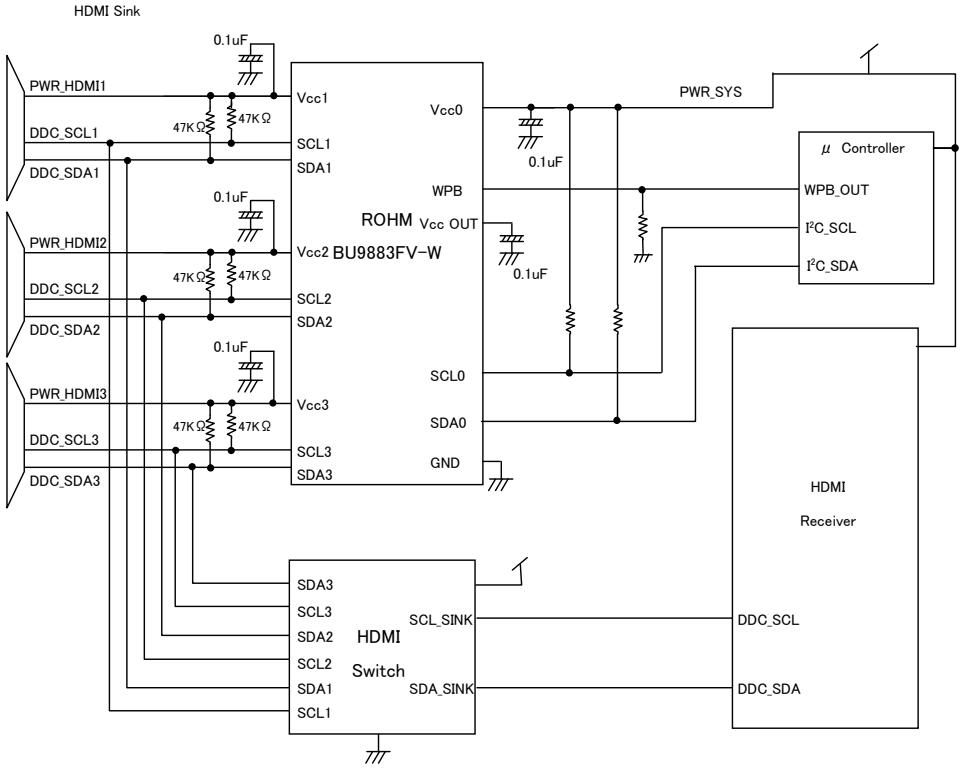


Fig.39　Application circuit

●WRITE CYCLE TIMING

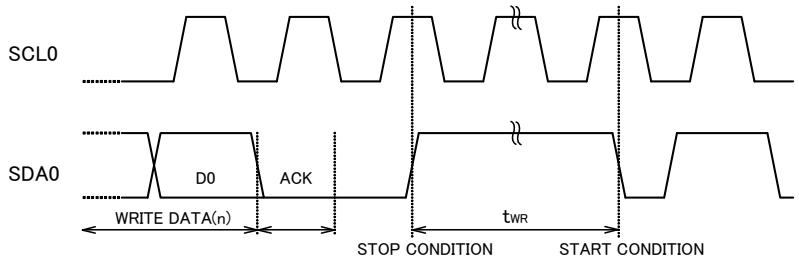


Fig.40 WRITE CYCLE TIMING

●WRITE OPERATION

BU9883FV-W has 2K bit EEPROM in each port, there are three BANKs, 6K bit EEPROM in this device.
Each BANK EEPROM can be written through PORT0.
There is no write operation through PORT1,2,3.
When this device is accessed throgh PORT0, WPB terminal must be set to “HIGH”.

Table1 Access port and write enable BANK

Port0	BANK1 ~ 3
Port1	No write operation
Port2	No write operation
Port3	No write operation

●READ OPERATION

Each BANK EEPROM can be read through each port.
The relation ship of access port and access BANK is describe Table2.

Table 1

Port0	BANK1 ~ 3
Port1	No write operation
Port2	No write operation
Port3	No write operation

Table 2

Port0	BANK1 ~ 3
Port1	BANK1
Port2	BANK2
Port3	BANK3

○When EEPROM access through PORT0, P1, P0 bits in slave address appoint access BANK.

Table 3

P1	P0	P1,P0 bit and access BANK
0	0	No bank selected
0	1	BANK1
1	0	BANK2
1	1	BANK3

Note) When P1=0, P0=0 : this device doesn’t return Acknowlege.

○During PORT0 access, WPB terminal must be set to “HIGH”, then PORT1 ~ 3 accesses will be cancelled.
○In accessing from PORT1 ~ 3, set WPB termianl to “LOW”

●DEVICE OPERATION

○START CONDITION

・ All commands are proceeded by the start condition, which is a HIGH to LOW transition of SDA0～3 when SCL0～3 is HIGH.
・ This device continuously monitors the SDA0～3 and SCL0～3 lines for the start condition and will not respond to any command until this condition has been met.

○STOP CONDITION

・ All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA0 ～3when SCL0～3 is HIGH.
・ The stop condition initiates internal write cycle to write the data into memory array after write sequence.
・ The stop condition is also used to place the device into the standby power mode after read sequence.
・ A stop condition can only be issued after the transmitting device has released the bus.

○NOTICE ON WRITE COMMAND

・ In Write command, after transmit write data, if there are no stop condition, EEPROM data don’t change.

○DEVICE ADDRESSING

・ Following a START condition, the master output the device address of the slave to be accessed.

The most significant four bits of the slave address are the “device type indentifier,” for this device, this is fixed as “1010.”

The next three bit specify a particular device. For PORT0 access, that are set “0”, “P1”, “P0”, for PORT 1 ~ 3 access, that must be set “000”.

The last bit of the stream determines the operation to be performed.

When set to “1” a read operation is selected ; when set to “0,” a write operation is selected.

R/$\overline{W}$ set to “0” ・・・・・・・・・ WRITE

R/$\overline{W}$ set to “1” ・・・・・・・・・ READ

○ACKNOWLEDGE

・ Acknowledge is a software convention used to indicate successful data transfers.The master or the slave will release the bus after transmitting eight bits.During the ninth clock cycle, the receiver will pull the SDA line LOW to Acknowledgethat the eight bits of data has been received.

・ This device will respond with an Acknowledge after recognition of a START condition and its slave address.If both the device and a write operation have been selected, this device will respond with an Acknowledge, after the receipt of each subsequent 8-bit word.

・ In the READ mode, this device will transmit eight bit of data, release the SDA line, and monitor the line for an Acknowledge.

・ If an Acknowledge is detected, and no STOP condition is generated by the master, this device will continue to transmit the data.

・ If an Acknowledge is not detected, this device will terminate further data transmissions and await a STOP condition before returning to the standby mode.

・ This device dosen't return Acknouwedge in internal write cycle.

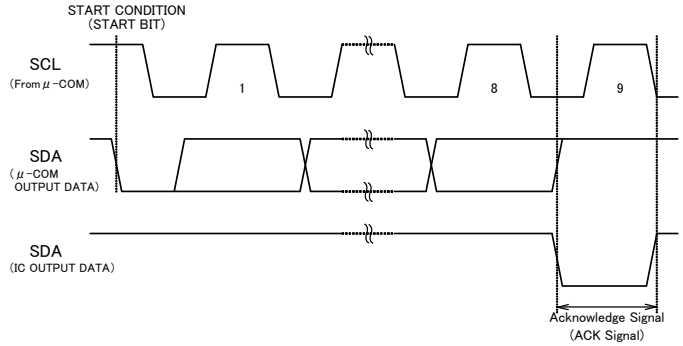


Fig.41 ACKNOWLEDGE RESPONSE FROM RECEIVER

●PORT0 access commands

○For PORT0 access, WPB terminal must be set to “HIGH”.

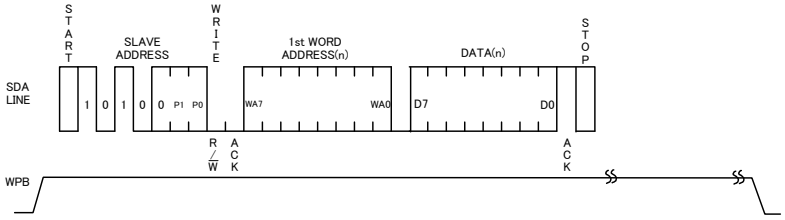


Fig.42 BYTE WRITE CYCLE TIMING (PORT0)

○This write commands operate EEPROM write sequence at address which is appointed by P1, P0. When the master generates a STOP condition, this device begins the internal write cycle to the nonvolatile array.

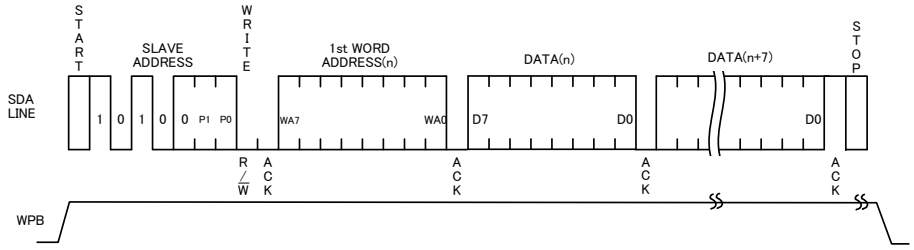


Fig.43 PAGE WRITE CYCLE TIMING (PORT0)

○This device is capable of eight byte page write operation.
○After the receipt of each word, the three low order address bits are internally incremented by one. The most significant address bits (WA7 ~ WA3) remain constant, if the master transmits more than 8 words.
○The relationship of P1, P0 inputs and access BANK is described as follows.

P1	P0	BANK
0	0	No opearation
0	1	BANK1
1	0	BANK2
1	1	BANK3

○Don't set P1, P0=0, 0. If P1, P0 are set to 0, there is no target bank, so this device doesn't return cknowlege.
○WPB terminal must be set to “HIGH” during Byte Write cycle, and Page Write cycle, and internal Write cycles. If WPB is set to “LOW” in above condition, programing doesn't work, and during internal Write cycle, WPB terminal set to “LOW”, this device terminate programing, and the data in programing address is not stored correctly.

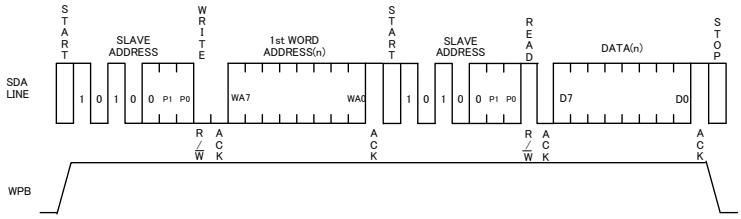


Fig.44 RANDOM READ CYCLE TIMING（PORT0）

○Random read operation allows the master to access any memory location which is appointed by P1, P0 bit.
This operation involves a two-step process.
First, the master issue a write command which includes the start condition and the slave address field (with R/$\overline{W}$ set to “0”) followed by the address of the word be read.
This procedure sets the internal address counter of this device to the desired address. After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by the slave address field with R/$\overline{W}$ the set to “1.” This device will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location.
If the master does not acknowledge the transmission but does generate the stop condition, at this point this device discontinues transmission.

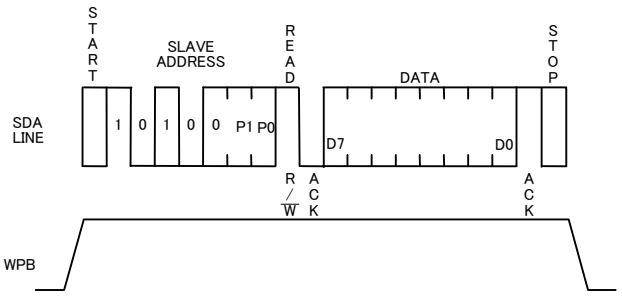


Fig.45 CURRENT READ CYCLE TIMING (PORT0)

○When the command just before Current Read cycle is Random Read cycle or Current Read cycle (each including Sequential Read cycle), data of incremented last read address (n)-th address, i.e.n, data of the (n+1)-th address is output.
When the command just before Current Read cycle is Byte Write or Page write, data of latest write address is output.

○Current Read operation allows the master to access data word stored in internal address counter which is appointed by P1, P0 bit. This operation involves a two-step process. This device will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location.
If the master does not acknowledge the transmission but does generate the stop condition, at this point this device discontinues transmission.

note) If the master send Acknowredge at after D0 output, Sequential Read is selected, and this device output next address data, and master can't send stop condition, so master can't discontinues transmission.
To stop read command, the master must send no Acknowledge at after D0 output, and issue stop condition.

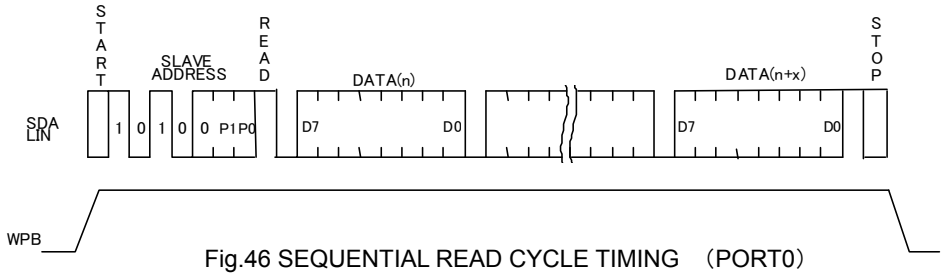


Fig.46 SEQUENTIAL READ CYCLE TIMING （PORT0）

○During the sequential read operation, the internal address counter of this device automatically increments with each acknowledge received ensuring the data from address will be followed with the data from n+1. For read operations, all bits of the address counter are incremented allowing the entire array to be read during a single operation. When the counter reaches the top of the array, it will “roll over” to the bottom of the array of BANK and continue to transmit the data.
○The sequential read operation can be performed with both current read and random read.

●PORT1,2,3 access commands

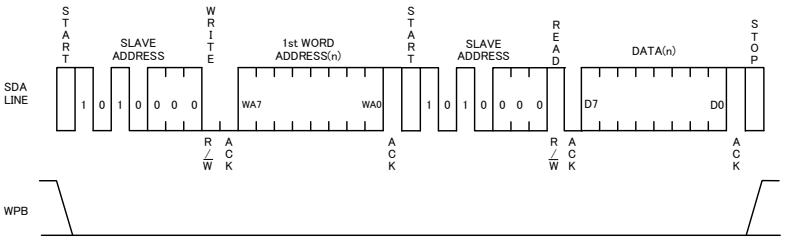


Fig.47 RANDOM READ CYCLE TIMING（PORT1～3）

○Random read operation allows the master to access any memory location of the BANK which is appointed by P1, P0. This operation involves a two-step process.
First, the master issues a write command which includes the start condition and the slave address field (with R/W set to “0”) followed by the address of the word be read.
This procedure sets the internal address counter of this device to the desired address.
After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by the slave address field with R/$\overline{W}$ the set to “1.”
This device will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location.
If the master does not acknowledge the transmission but does generate the stop condition, at this point this device discontinues transmission.

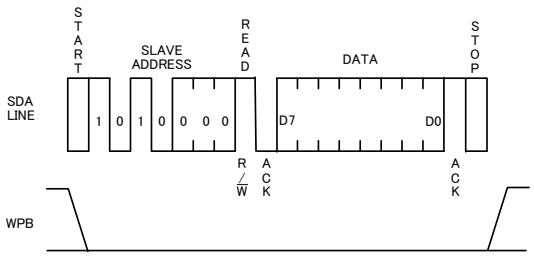


Fig.48 CURRENT READ CYCLE TIMING (PORT1～3)

○When the command just before Current Read cycle is Random Read cycle or Current Read cycle (each including Sequential Read cycle), data of incremented last read address (n)-th address, i.e.n, data of the (n+1)-th address is output. When the command just before Current Read cycle is Byte Write or Page write, data of latest write address is output.

○Random read operation allows the master to access any memory location. The BANK which is appointed by P1, P0. This operation involves a two-step process.

First, the master issues a write command which includes the start condition and the slave address field (with R/$\overline{W}$ set to “0”) followed by the address of the word be read. This procedure sets the internal address counter of this device to the desired address. After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by the slave address field with R/$\overline{W}$ the set to “1.” This device will respond with an acknowledge and then transmit the 8-data bits stored
at the addressed location.

If the master does not acknowledge the transmission but does generate the stop condition, at this point this device discontinues transmission.

note) If the master send Acknowredge at after D0 output, Sequential Read is selected, and this device output next address data, and master can't send stop condition, so master can't discontinues transmission. To stop read command, the master must send no Acknowledge at after D0 output, and issue stop condition.

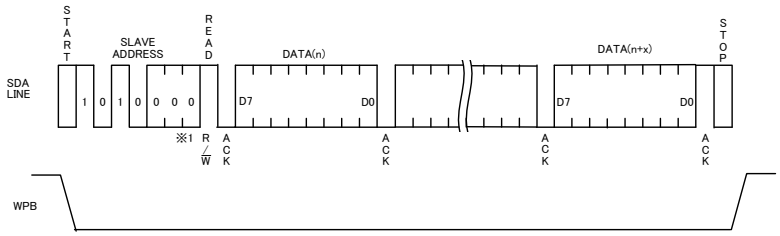


Fig.49 SEQUENTIAL READ CYCLE TIMING （PORT1～3）

○During the sequential read operation, the internal address counter of this device automatically increments with each acknowledge received ensuring the data from address n will be followed with the data from n+1. For read operations, all bits of the address counter are incremented allowing the entire array to be read during a single operation. When the counter reaches the top of the array, it will “roll over to the bottom of the array and continue to transmit the data.

○The sequential read operation can be performed with both current read and random read.

●Access Control of PORT0,1,2,3

WPB terminal controls access enable of each PORT, as follows.

PORT	WPB terminal inputs	
	0	1
PORT0	not accessible	Read/Write
PORT1	Read	not accessible
PORT2	Read	not accessible
PORT3	Read	not accessible

Table4 WPB terminal and port accesibility

○When WPB terminal is “HIGH”, PORT0 only can access this device.
In this case, when commands from PORT1, 2, 3 are inputted, these port don't return acknowledge.

○When WPB terminal is “LOW”, PORT0 access is not valid, but PORT1, 2, 3 can access this device this device.
Commands from PORT1, 2, 3 is performs independently other port.

●Software reset

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Fig.50(a), Fig.50(b), and Fig.50 (c).) In dummy clock input area, release the SDA0～3 bus ('H' by pull up). In dummy clock area, ACK output and read data '0' (both 'L' level) may be output from EEPROM, therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

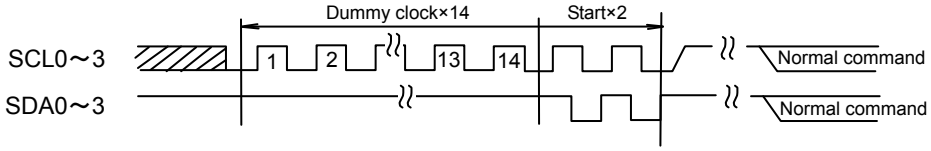


Fig.50-(a) The case of dummy clock +START+START+ command input

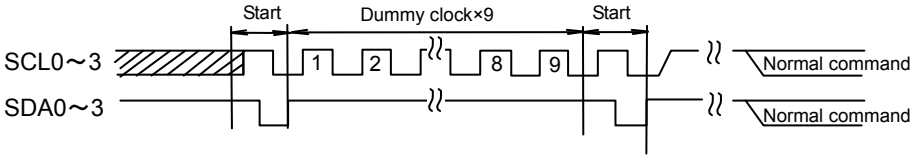


Fig.50-(b) The case of START +9 dummy clocks +START+ command input

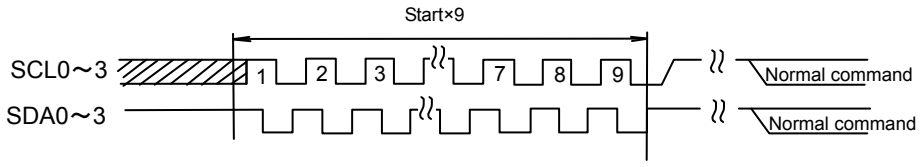


Fig.50-(c) START×9+ command input

※ Start command from START input.

●Acknowledge polling

During internal write execution, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back 'L', then it means end of write action, while if it sends back 'H', it means now in writing. By use of acknowledge polling, next command can be executed without waiting for tWR = 5ms.

When to write continuously, R/$\overline{W}$ = 0, when to carry out current read cycle after write, slave address R/$\overline{W}$ = 1 is sent, and if ACK signal sends back 'L', then execute word address input and data output and so forth.

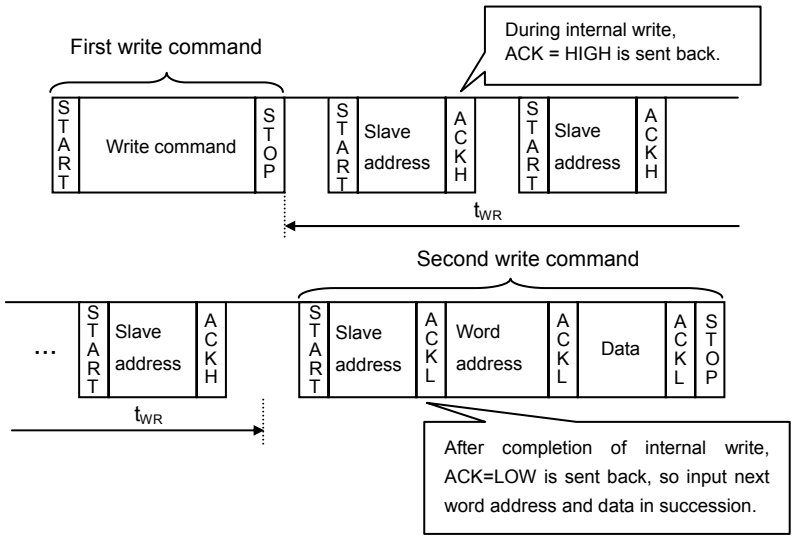


Fig.51 Case to continuously write by acknowledge polling

●Command cancel by start condition and stop condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Refer to Fig. 52.)

However, in ACK output area and during data read, SDA0～3 bus may output 'L', and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. And when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in succession, carry out random read cycle.

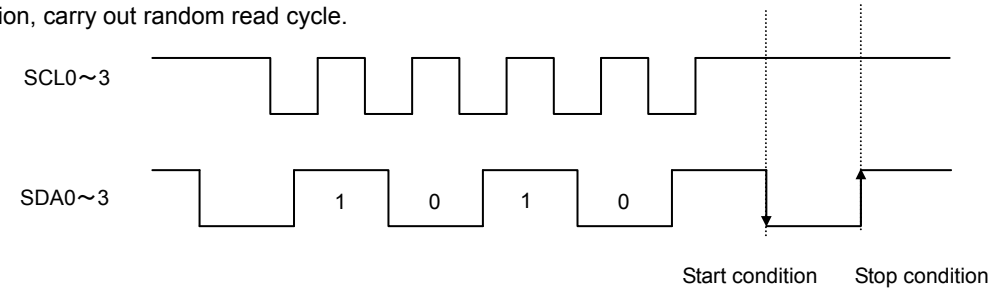


Fig.52 Case of cancel by start, stop condition during slave address input

●I/O peripheral circuit

○Pull up resistance of SDA0～3 terminal

SDA0～3 is NMOS open drain, so requires pull up resistance. As for this resistance value (R_{PU}), select an appropriate value to this resistance value from microcontroller V_{IL}, I_L, and V_{OL}0～3-I_{OL} characteristics of this IC. If R_{PU} is large, action frequency is limited. The smaller the R_{PU}, the larger the consumption current at action.

○Maximum value of R_{PU}

The maximum value of R_{PU} is determined by the following factors. The following Vcc, SDA, R_{PU} and I_L correspond to them of each port.

(1)SDA0～3 rise time to be determined by the capacitance (CBUS) of bus line of R_{PU} and SDA0～3 should be tR or below.
And AC timing should be satisfied even when SDA0～3 rise time is late.

(2)The bus electric potential Ⓐ to be determined by input leak total (I_L) of device connected to bus at output of 'H' to SDA0～3 bus and R_{PU} should sufficiently secure the input 'H' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin 0.2Vcc.

$$Vcc - I_L R_{PU} - 0.2Vcc \geqq V_{IH}$$

$$\therefore \quad R_{PU} = \frac{0.8Vcc - V_{IH}}{I_L}$$

Ex.) When V_{CC} =3V, I_L=10 μ A, V_{IH}=0.7 V_{CC},

from (2)

$$R_{PU} \leqq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}}$$

$$\leqq 300\ [k\Omega]$$

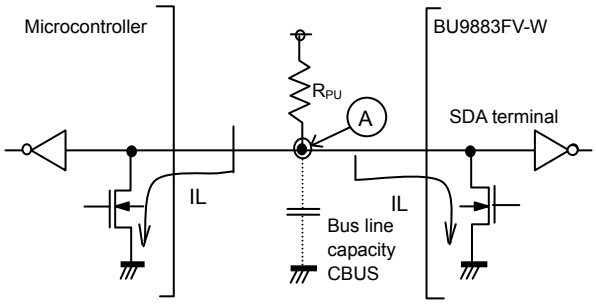


Fig.53 I/O circuit diagram

○Minimum value of R_{PU}

The minimum value of R_{PU} is determined by the following factors. The following Vcc, V_{OL}, I_{OL}, and R_{PU} correspond to them of each port.

(1)When IC outputs LOW, it should be satisfied that V_{OLMAX}=0.4V and I_{OLMAX}=3mA.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leqq I_{OL} \qquad \therefore \quad R_{PU} \leqq \frac{V_C - V_{OL}}{I_{OL}}$$

(2)V_{OLMAX}=0.4V should secure the input 'L' level (V_{IL}) of microcontroller and EEPROM including recommended noise margin 0.1Vcc.

$$V_{OLMAX} \leqq V_{IL} - 0.1\ V_{CC}$$

Ex.) When V_{CC} =3V, V_{OL}=0.4V, I_{OL}=3mA, microcontroller, EEPROM V_{IL}=0.3Vcc

from (1)

$$R_{PU} \geqq \frac{3 - 0.4}{3 \times 10^{-3}}$$

$$\geqq 867\ [\Omega]$$

And

$$V_{OL} = 0.4\ [V]$$

$$V_{IL} = 0.3 \times 3$$

$$= 0.9\ [V]$$

Therefore, the condition (2) is satisfied.

○Pull up resistance of SCL0～3 terminal

When SCL0～3 control is made at CMOS output port, there is no need, but in the case there is timing where SCL0～3 becomes 'Hi-Z', add a pull up resistance. As for the pull up resistance, one of several kΩ ~ several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

●Cautions on microcontroller connection

○Rs

In I^2C BUS, it is recommended that SDA port is of open drain input/output. However, when to use CMOS input / output of tri state to SDA port, insert a series resistance Rs between the pull up resistance Rpu and the SDA terminal of EEPROM. This is controls over current that occurs when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. Rs also plays the role of protection of SDA terminal against surge. Therefore, even when SDA port is open drain input/output, Rs can be used. The following SCL SDA R_{PU} and R_S correspond to them of each port.

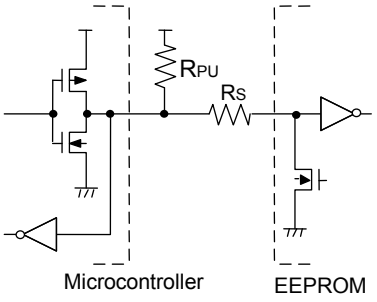


Fig.54 I/O circuit diagram

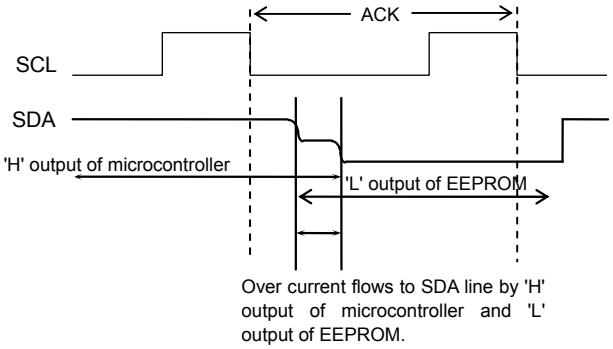


Fig.55 Input / output collision timing

○Maximum value of Rs

The maximum value of Rs is determined by the following relations. The following Vcc, V_{OL}, R_S, R_{PU}, I_{OL}, and SDA correspond to them of each port.

(1)SDA rise time to be determined by the capacity (CBUS) of bus line of Rpu and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential Ⓐ to be determined by Rpu and Rs the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level (V_{IL}) of microcontroller including recommended noise margin 0.1Vcc.

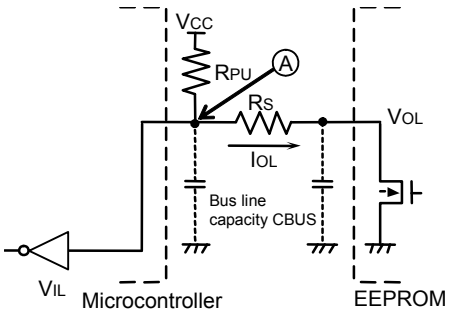


Fig.56 I/O circuit diagram

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

$$\therefore\ R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Example) When V_{CC}=3V, V_{IL}=0.3V_{CC}, V_{OL}=0.4V, R_{PU}=20kΩ,

$$\text{from(2)},\quad R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leqq 1.67[k\Omega]$$

○Minimum value of Rs

The minimum value of Rs is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below. The following Vcc, R_{PU}, R_S, and I correspond to them of each port.

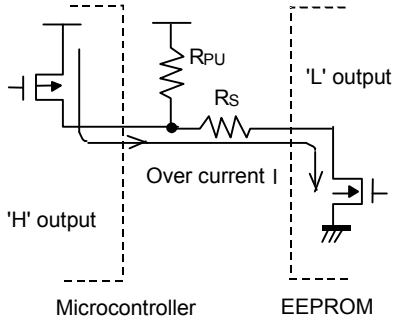


Fig.57 I/O circuit diagram

$$\frac{V_{CC}}{R_S} \leqq I$$

$$\therefore\ R_S \geqq \frac{V_{CC}}{I}$$

Example) When V_{CC}=3V, I=10mA

$$R_S \geqq \frac{3}{10\times10^{-3}}$$

$$\geqq 300[\Omega]$$

●I^2C BUS input / output circuit

○Input (SCL0～3)

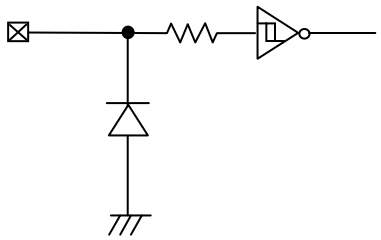


Fig.58 Input pin circuit diagram

○Input / output (SDA0～3)

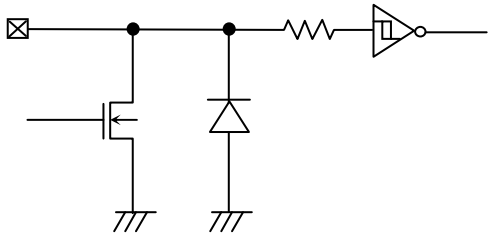


Fig.59 Input / output pin circuit diagram

○Input (WPB)

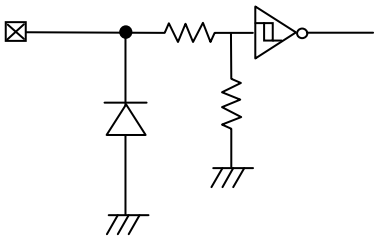


Fig.60 Input pin circuit diagram

●Notes on power ON

At power on, in IC internal circuit and set, Vcc rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, functions of POR circuit and LVCC circuit are equipped. To assure the action, observe the following conditions at power on.

1. Set SDA0～3 = 'H' and SCL0～3 ='L' or 'H'
2. Start power source so as to satisfy the recommended conditions of t_R, t_{OFF}, and Vbot for operating POR circuit.

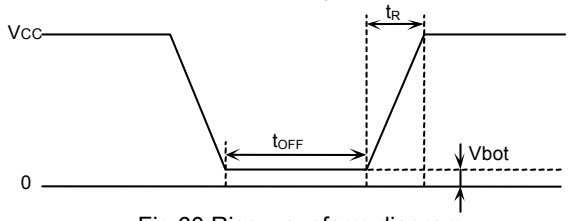


Fig.60 Rise waveform diagram

Recommended conditions of t_R, t_{OFF},Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or longer	0.3V or below
100ms or below	10ms or longer	0.2V or below

3. Set SDA0～3 and SCL0～3 so as not to become 'Hi-Z'.

When the above conditions 1 and 2 cannot be observed, take the following countermeasures.

a) In the case when the above condition 1 cannot be observed. When SDA0～3 becomes 'L' at power on.

→Control SCL0～3 and SDA0～3 as shown below, to make SCL0～3 and SDA0～3, 'H' and 'H'.

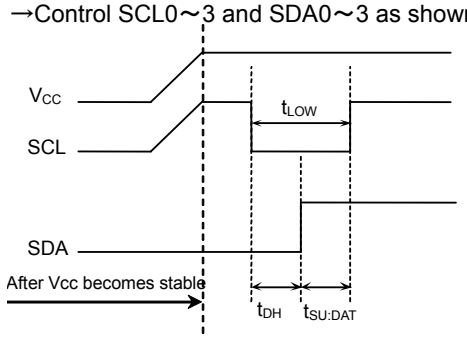


Fig.61 When SCL0～3= 'H' and SDA0～3= 'L'

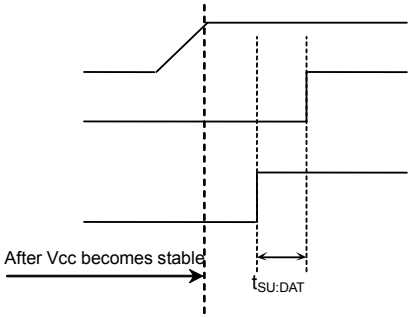


Fig.62 When SCL0～3='L' and SDA0～3='L'

b) In the case when the above condition 2 cannot be observed.

→After power source becomes stable, execute software reset(P11).

c) In the case when the above conditions 1 and 2 cannot be observed.

→Carry out a), and then carry out b).

●Low voltage malfunction prevention function

LVCC circuit prevents data rewrite action at low power, and prevents wrong write. At LVCC voltage (Typ. =1.2V) or below, it prevent data rewrite.

●Vcc noise countermeasures

○Bypass capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC Vcc_{OUT} and GND. At that moment, attach it as close to IC as possible.

And, it is also recommended to attach a bypass capacitor between board Vcc_{OUT} and GND.

●Cautions on use

(1)Described numeric values and data are design representative values, and the values are not guaranteed.

(2)We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3)Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4)GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(5)Terminal design

In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(6)Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7)Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

●Ordering part number

B	U	9	8	8	3	F	V	-	W	E	2

Part No.

Part No.

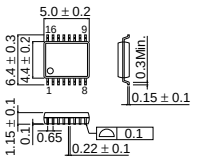
Package
FV: SSOP-B16

W: Double Cell

Packaging and forming specification
E2: Embossed tape and reel

SSOP-B16

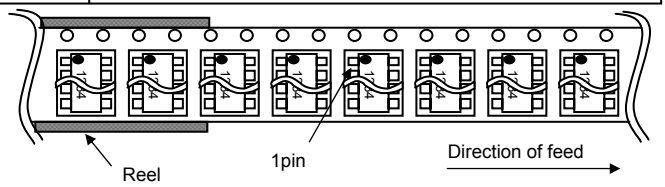
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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R0128A

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