BUJD105AD

NPN power transistor with integrated diode

Rev. 01 — 8 May 2009 Product data sheet

1. Product profile

1.1 General description

High voltage, high speed, planar passivated NPN power switching transistor with integrated anti-parallel E-C diode in a SOT428 (DPAK) surface-mountable plastic package.

1.2 Features and benefits

- Fast switching
- High voltage capability
- Very low switching and conduction losses

1.3 Applications

- DC-to-DC converters
- Electronic lighting ballasts
- Inverters
- Motor control systems

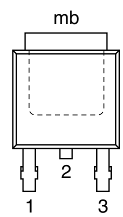
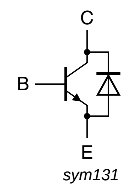
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_C	collector current		-	-	8	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C; see Figure 3	-	-	80	W
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0$ V	-	-	700	V
Static characteristics						
h_{FE}	DC current gain	$V_{CE} = 5$ V; $I_C = 4$ A; $T_{mb} = 25$ °C; see Figure 6; see Figure 7	8	13.5	-	

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 SOT428 (SC-63; DPAK)	
2	C	collector [1]		
3	E	emitter		
mb	C	mounting base; connected to collector		

[1] It is not possible to make a connection to pin 2 of the SOT428 (DPAK) package.

3. Ordering information

Table 3. Ordering information

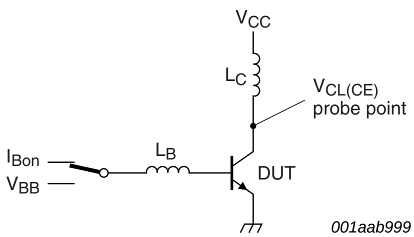
Type number	Package		
	Name	Description	Version
BUJD105AD	SC-63; DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

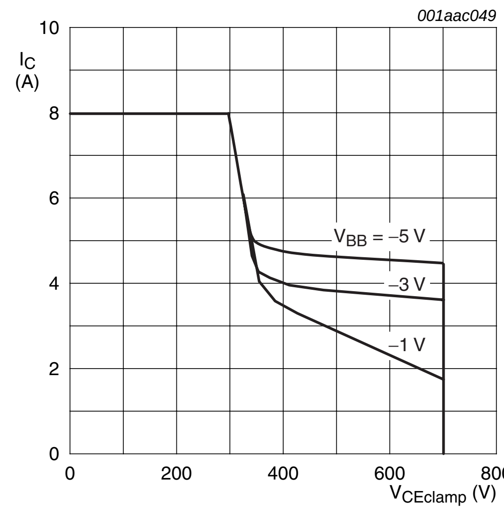
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	V_{BE} = 0 V	-	700	V
V_{CBO}	collector-base voltage	I_E = 0 A	-	700	V
V_{CEO}	collector-emitter voltage	I_B = 0 A	-	400	V
I_C	collector current		-	8	A
I_{CM}	peak collector current	see Figure 1; see Figure 2	-	16	A
I_B	base current		-	4	A
I_{BM}	peak base current		-	8	A
P_{tot}	total power dissipation	T_{mb} ≤ 25 °C; see Figure 3	-	80	W
T_{stg}	storage temperature		-65	150	°C
T_j	junction temperature		-	150	°C



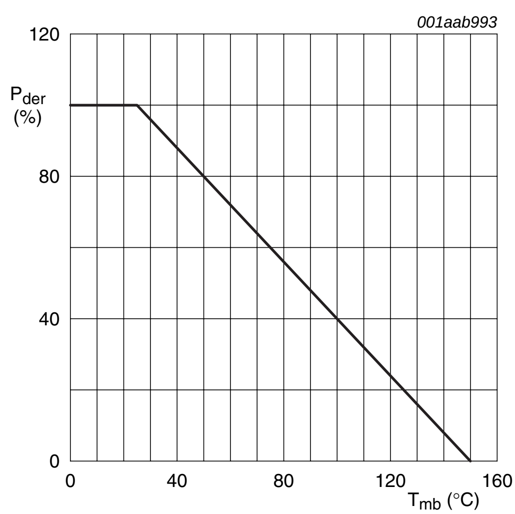
$V_{CEclamp} \leq 1000$ V; $V_{CC} = 150$ V;
$V_{BB} = -5$ V; $L_B = 1$ μH; $L_C = 200$ μH

Fig 1. Test circuit for reverse bias safe operating area



$T_j \leq T_{j(max)}$ °C

Fig 2. Reverse bias safe operating area



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 3. Normalized total power dissipation as a function of mounting base temperature

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.56	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	printed-circuit-board mounted; minimum footprint; see Figure 5	-	75	-	K/W

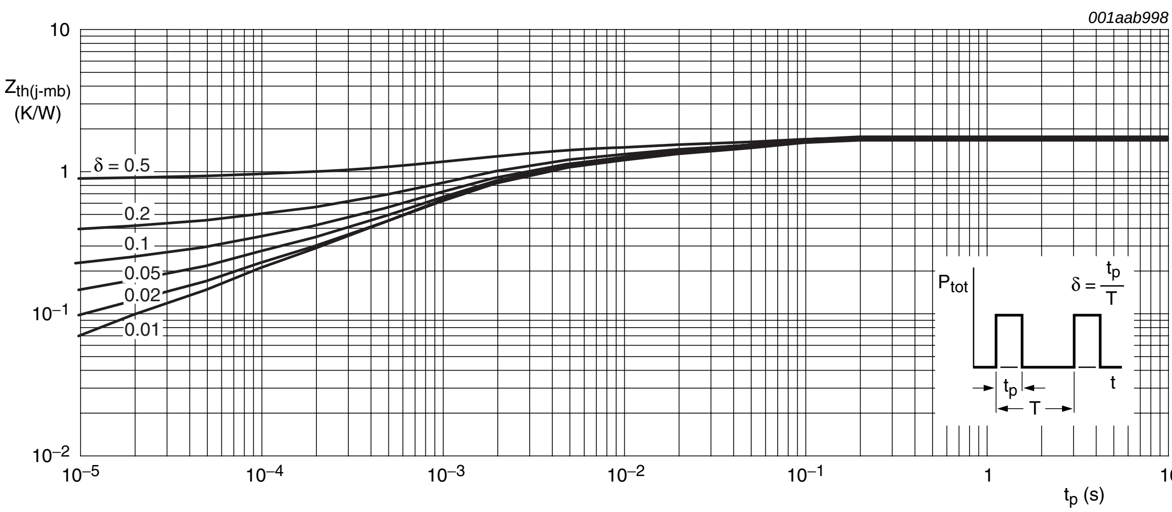
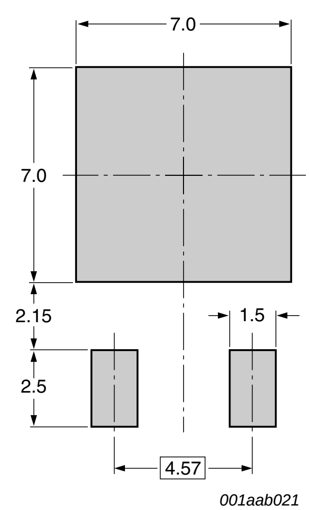


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse width



all dimensions are in mm

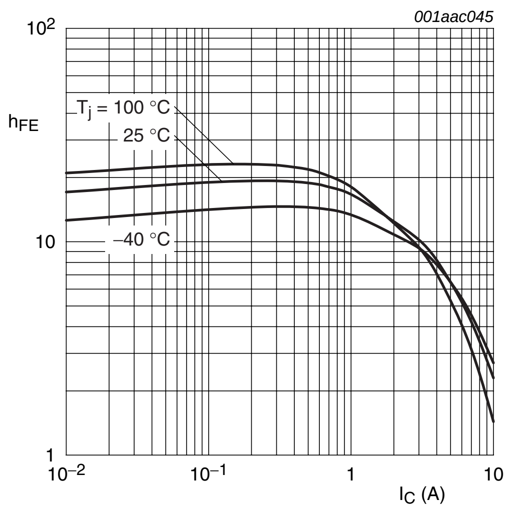
Fig 5. Minimum footprint SOT428

6. Characteristics

Table 6. Characteristics

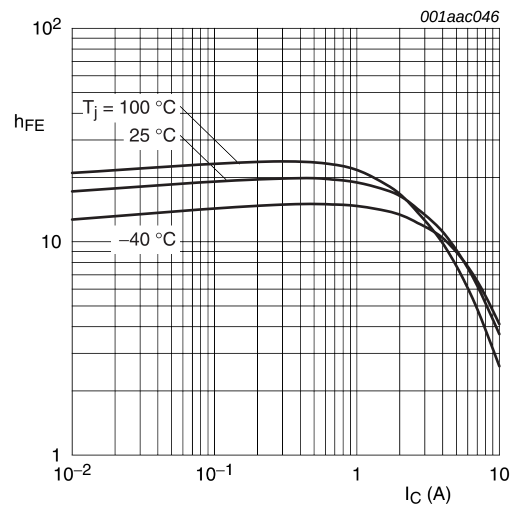
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 4 A; T_{mb} = 25 °C; see Figure 6; see Figure 7		8	13.5	-	
		V_{CE} = 5 V; I_C = 1 mA; T_{mb} = 25 °C		10	17	34	
		V_{CE} = 5 V; I_C = 500 mA; T_{mb} = 25 °C		13	23	36	
I_{CBO}	collector-base cut-off current	I_E = 0 A; V_{CB} = 700 V	[1]	-	-	0.2	mA
I_{CEO}	collector-emitter cut-off current	I_B = 0 A; V_{CE} = 400 V	[1]	-	-	0.1	mA
I_{CES}	collector-emitter cut-off current	V_{CE} = 700 V; V_{BE} = 0 V; T_j = 25 °C	[1]	-	-	0.2	mA
		V_{CE} = 700 V; V_{BE} = 0 V; T_j = 125 °C	[1]	-	-	0.5	mA
I_{EBO}	emitter-base cut-off current	I_C = 0 A; V_{EB} = 9 V		-	-	10	mA
V_{BEsat}	base-emitter saturation voltage	I_C = 4 A; I_B = 0.8 A; see Figure 8		-	1	1.5	V
V_{CEOsus}	collector-emitter sustaining voltage	I_B = 0 A; L_C = 25 mH; I_C = 10 mA; see Figure 9; see Figure 10		400	-	-	V
V_{CEsat}	collector-emitter saturation voltage	I_B = 0.8 A; I_C = 4 A; see Figure 11; see Figure 12		-	0.3	1	V
V_F	forward voltage	I_F = 4 A		-	1.07	1.5	V
Dynamic characteristics							
t_f	fall time	I_C = 5 A; I_{Bon} = 1 A; V_{BB} = -5 V; L_B = 1 µH; inductive load; T_{mb} = 25 °C; see Figure 13; see Figure 14		-	20	50	ns
		I_C = 5 A; I_{Bon} = 1 A; V_{BB} = -5 V; L_B = 1 µH; inductive load; T_{mb} = 100 °C		-	25	100	ns
		I_C = 5 A; I_{Bon} = 1 A; I_{Boff} = -1 A; R_L = 75 Ω; resistive load; T_j = 25 °C; see Figure 15; see Figure 16		-	0.3	0.5	µs
t_{on}	turn-on time	I_C = 5 A; I_{Bon} = 1 A; I_{Boff} = -1 A; R_L = 75 Ω; T_j = 25 °C; resistive load		-	0.65	1	µs
t_s	storage time	I_C = 5 A; I_{Bon} = 1 A; I_{Boff} = -1 A; R_L = 75 Ω; resistive load; T_j = 25 °C		-	1.8	2.5	µs
		I_C = 5 A; I_{Bon} = 1 A; R_L = 75 Ω; inductive load; T_j = 25 °C; L_B = 1 µH; V_{BB} = -5 V		-	1.2	1.7	µs
		I_C = 5 A; I_{Bon} = 1 A; I_{Boff} = -1 A; inductive load; T_j = 100 °C; L_B = 1 µH; V_{BB} = -5 V		-	1.4	1.9	µs

[1] Measured with half sine-wave voltage (curve tracer).



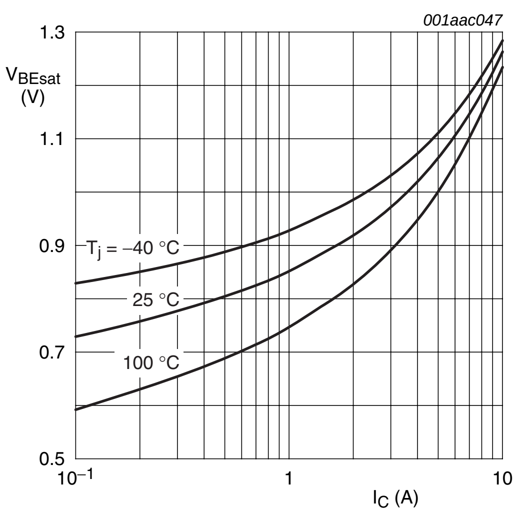
$V_{CE} = 1$ V

Fig 6. DC current gain as a function of collector current; typical values



$V_{CE} = 5$ V

Fig 7. DC current gain as a function of collector current; typical values



$I_C / I_B = 4$

Fig 8. Base-emitter saturation voltage as a function of collector current; typical values

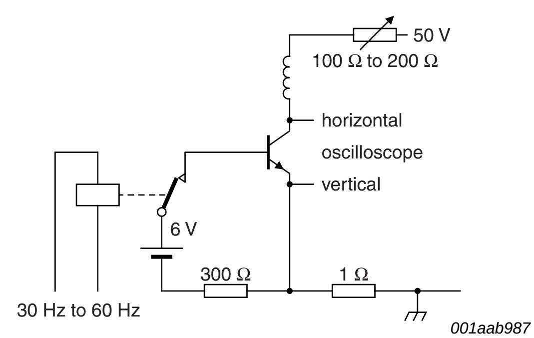


Fig 9. Test circuit for collector-emitter sustaining voltage

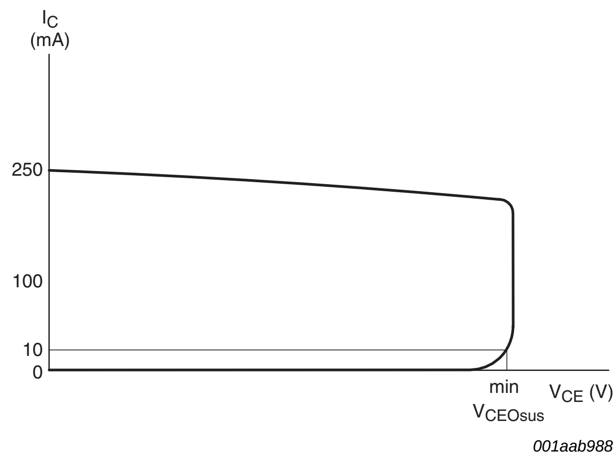
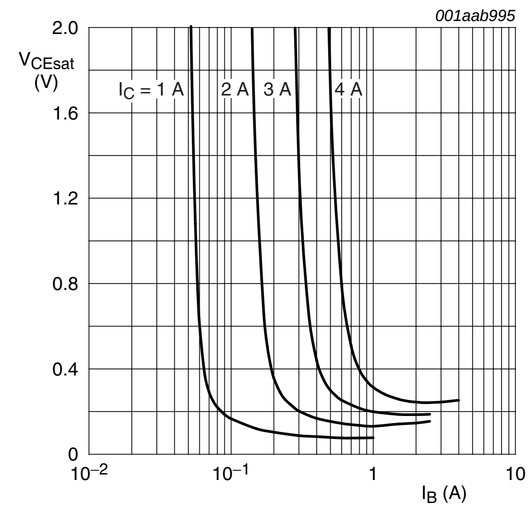
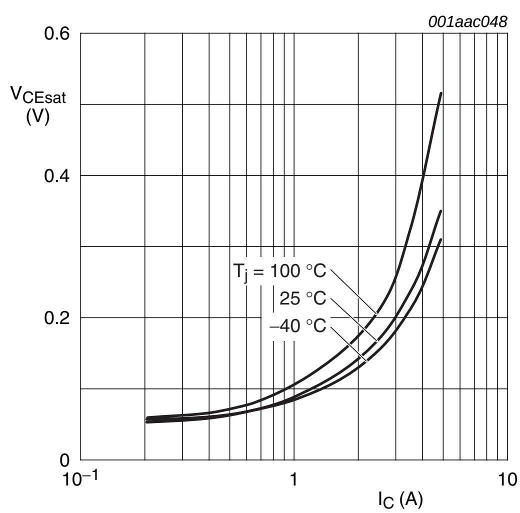


Fig 10. Oscilloscope display for collector-emitter sustaining voltage test waveform



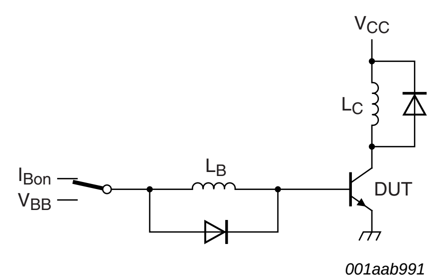
$T_j = 25\ °C$

Fig 11. Collector-emitter saturation voltage as a function of base current; typical values



$I_C / I_B = 4$

Fig 12. Collector-emitter saturation voltage as a function of collector current; typical values



$V_{CC} = 300$ V; $V_{BB} = -5$ V;
$L_C = 200\ \mu$H; $L_B = 1\ \mu$H

Fig 13. Test circuit for inductive load switching

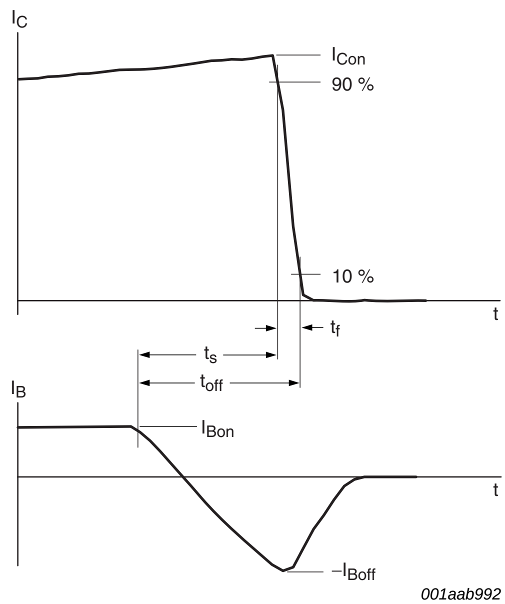
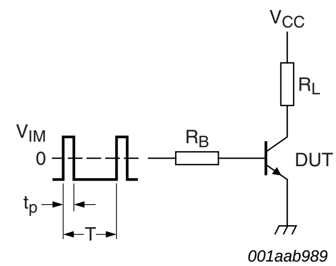


Fig 14. Switching times waveforms for inductive load



V_{IM} = −6 V to +8 V; V_{CC} = 250 V;
t_p = 20 μs; δ = t_p/T = 0.01
R_B and R_L calculated from I_{Con} and I_{Bon} requirements

Fig 15. Test circuit for resistive load switching

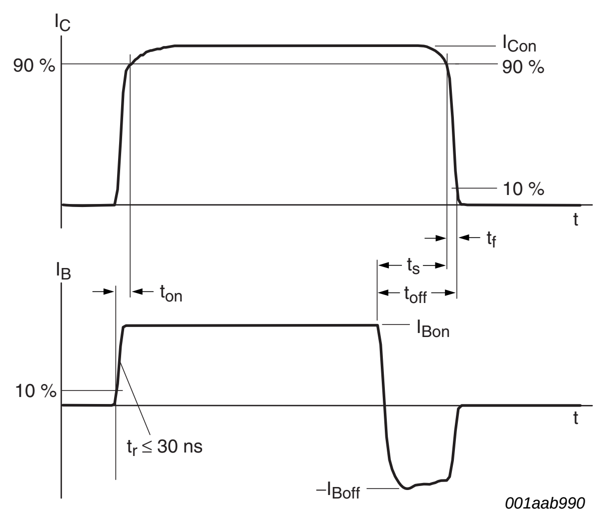
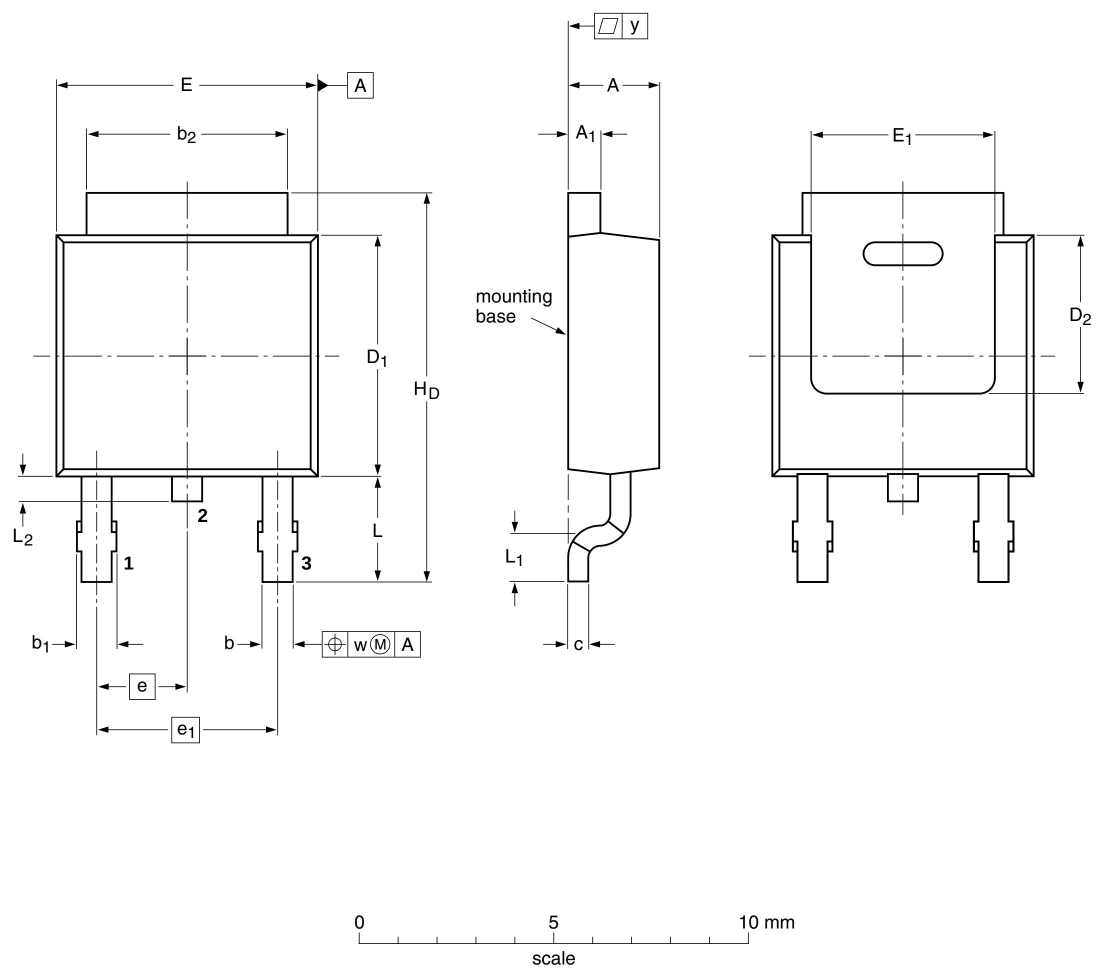


Fig 16. Switching times waveforms for resistive load

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2 min	E	E_1 min	e	e_1	H_D	L	L_1 min	L_2	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-02-14~~ 06-03-16

Fig 17. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUJD105AD_1	20090508	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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11. Contents

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