

BUK9MJJ-55PTT

Dual TrenchPLUS logic level FET

Rev. 01 — 14 May 2009

Product data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode field-effect power transistor in SO20. Device is manufactured using NXP High-Performance (HPA) TrenchPLUS technology, featuring very low on-state resistance, integrated current sensing transistors and over temperature protection diodes.

1.2 Features and benefits

- Integrated current sensors
- Integrated temperature sensors

1.3 Applications

- Lamp switching
- Motor drive systems
- Power distribution
- Solenoid drivers

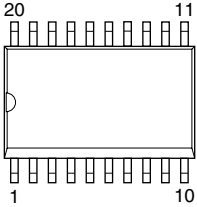
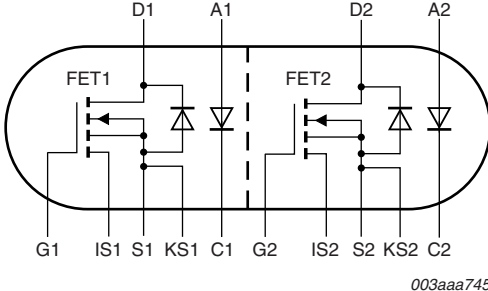
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics, FET1 and FET2						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; see Figure 16 ; see Figure 17	-	13	15	mΩ
I_D/I_{sense}	ratio of drain current to sense current	$T_j = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 18	5850	6500	7150	A/A
$V_{(BR)DSS}$	drain-source breakdown voltage	$T_j = 25\text{ °C}$; $V_{GS} = 0\text{ V}$; $I_D = 250\text{ μA}$	55	-	-	V

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G1	gate 1	 <p>SOT163-1 (SO20)</p>	
2	IS1	current sense 1		
3	D1	drain 1		
4	A1	anode 1		
5	C1	cathode 1		
6	G2	gate 2		
7	IS2	current sense 2		
8	D2	drain 2		
9	A2	anode 2		
10	C2	cathode 2		
11	D2	drain 2		
12	KS2	Kelvin source 2		
13	S2	source 2		
14	S2	source 2		
15	D2	drain 2		
16	D1	drain 1		
17	KS1	Kelvin source 1		
18	S1	source 1		
19	S1	source 1		
20	D1	drain 1		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9MJJ-55PTT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Limiting Values, FET1 and FET2					
V_{DS}	drain-source voltage	$25\text{ °C} < T_j < 150\text{ °C}$	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$; $25\text{ °C} < T_j < 150\text{ °C}$	-	55	V
V_{GS}	gate-source voltage		-15	15	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 3 ; see Figure 2 ; [1][2]	-	12.9	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 2 ; [1][2]	-	8.1	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed; see Figure 3	-	230	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 1	-	4.5	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage		-	100	V
Source-drain diode, FET1 and FET2					
I_S	source current	$T_{sp} = 25\text{ °C}$; [2][1]	-	6.5	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{sp} = 25\text{ °C}$	-	230	A
Avalanche ruggedness, FET1 and FET2					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 12.9\text{ A}$; $V_{sup} \leq 55\text{ V}$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; see Figure 4 ; [3][4] [5]	-	527	mJ
Electrostatic discharge, FET1 and FET2					
V_{ESD}	electrostatic discharge voltage	HBM; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$; pins 3, 16 and 20 to pins 1, 2, 17, 18 and 19 shorted	-	4	kV
		HBM; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$; pins 8, 11 and 15 to pins 6, 7, 12,13 and 14 shorted	-	4	kV
		HBM; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$; all pins	-	0.15	kV

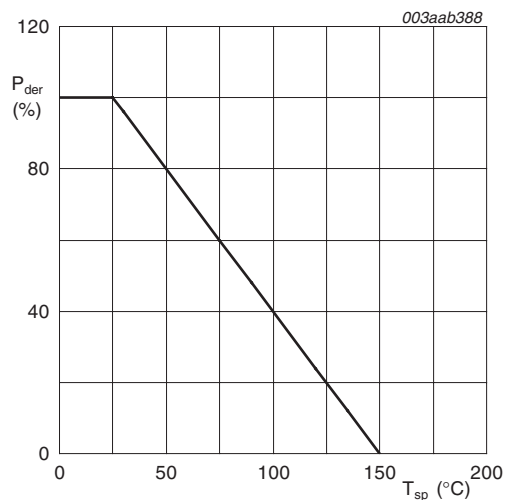
[1] Single device conducting.

[2] Current is limited by chip power dissipation rating.

[3] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C .

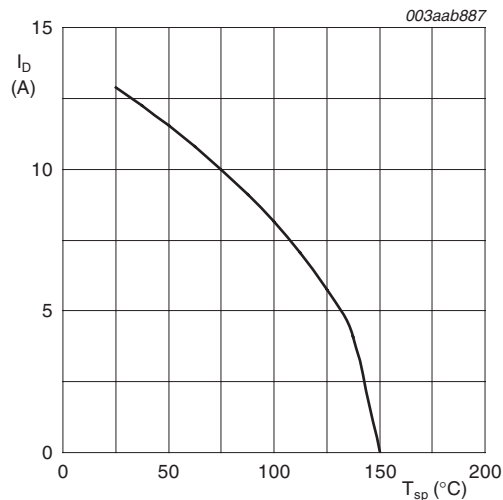
[4] Repetitive rating defined in avalanche rating figure.

[5] Refer to application note AN10273 for further information.



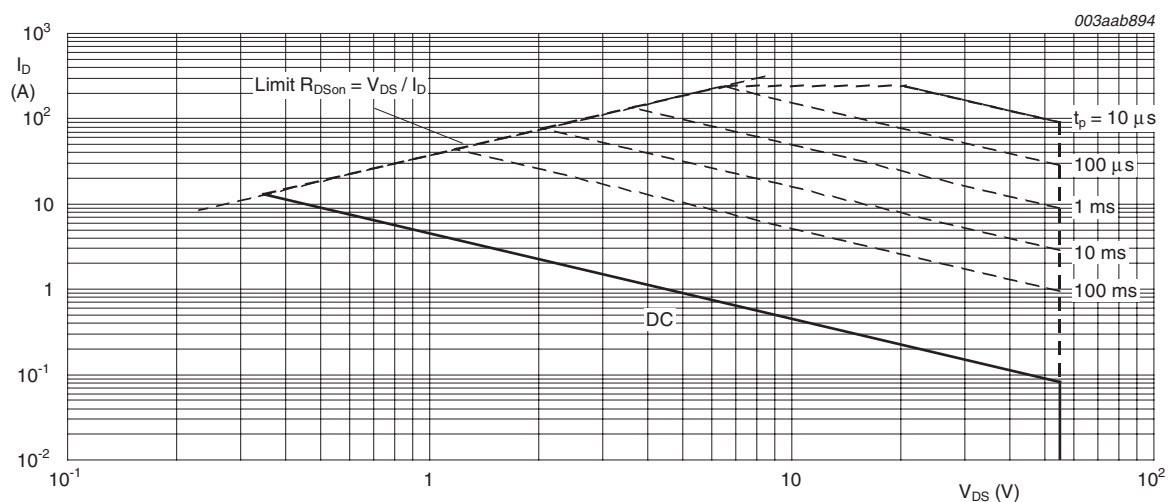
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature, FET1 and FET2



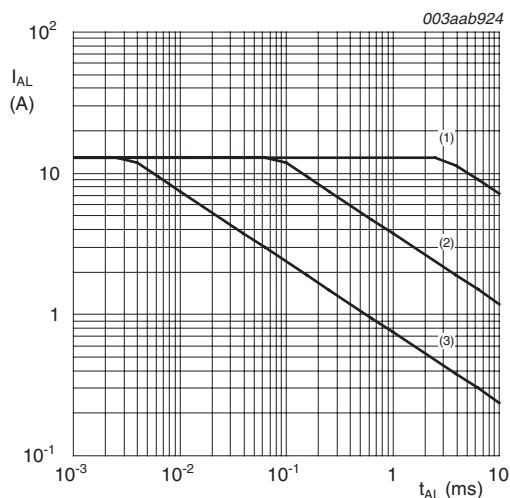
$$V_{GS} \geq 5\text{ V}$$

Fig 2. Continuous drain current as a function of solder point temperature, FET1 and FET2



$$T_{sp} = 25^{\circ}\text{C}; I_{DM} \text{ is single pulse}$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET1 and FET2



(1) Single-pulse; $T_j = 25\text{ }^{\circ}\text{C}$.

(2) Single-pulse; $T_j = 150\text{ }^{\circ}\text{C}$.

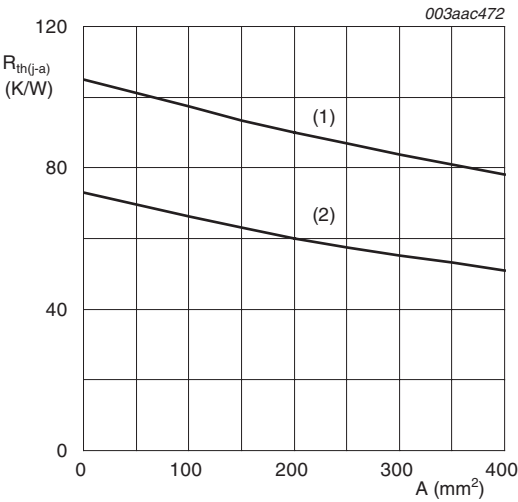
(3) Repetitive.

Fig 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	FET1	-	-	28	K/W
		FET2	-	-	28	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; Both channels conducting; zero heat sink area; see Figure 5 ; see Figure 6	-	73	-	K/W
		mounted on a printed-circuit board; Both channels conducting; 200 mm ² copper heat sink area; see Figure 5 ; see Figure 7	-	60	-	K/W
		mounted on a printed-circuit board; Both channels conducting; 400 mm ² copper heat sink area; see Figure 5 ; see Figure 8	-	51	-	K/W
		mounted on a printed-circuit board; One channel conducting; zero heat sink area; see Figure 5 ; see Figure 6	-	105	-	K/W
		mounted on a printed-circuit board; One channel conducting; 200 mm ² copper heat sink area; see Figure 5 ; see Figure 7	-	90	-	K/W
		mounted on a printed-circuit board; One channel conducting; 400 mm ² copper heat sink area; see Figure 5 ; see Figure 8	-	78	-	K/W



- (1) One channel conducting dissipating 500mW.
 - (2) Both channels conducting each dissipating 500mW.
- Zero air flow

Fig 5. Thermal resistance from junction to ambient as a function of printed-circuit board (PCB) heat sink area

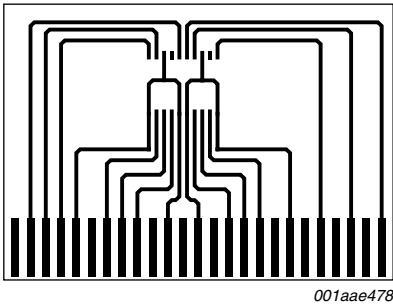


Fig 6. PCB used for thermal tests; zero heat sink area

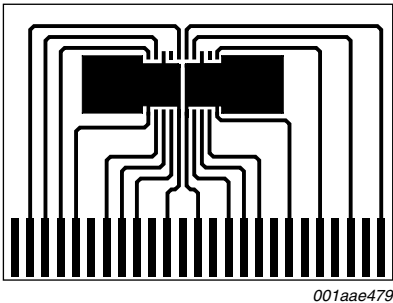


Fig 7. PCB used for thermal tests; heat sink area 200 mm²

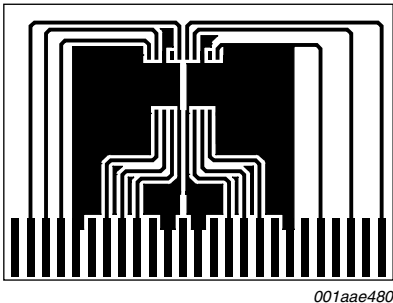


Fig 8. PCB used for thermal tests; heat sink area 400 mm²

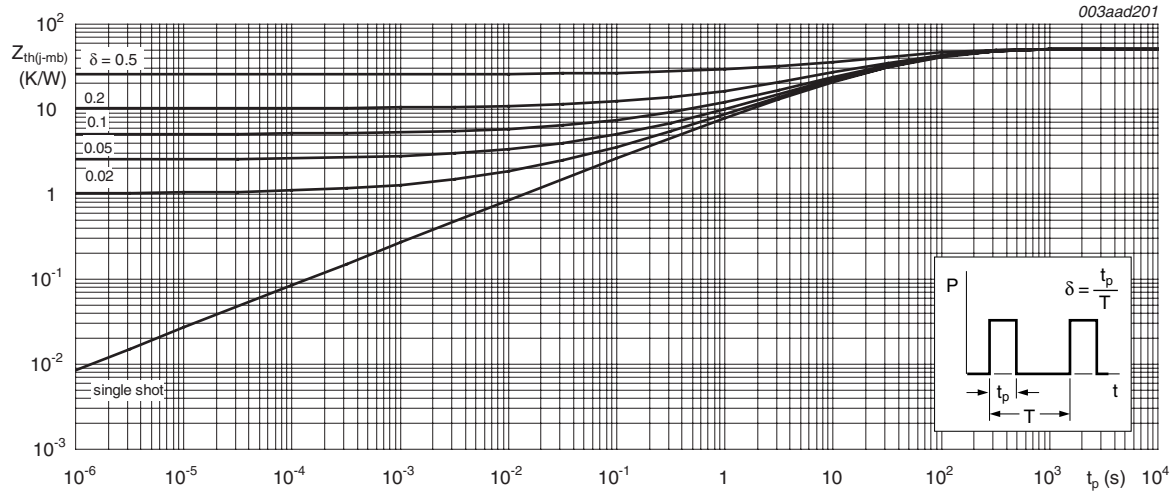


Fig 9. Transient thermal impedance from junction to ambient as a function of pulse duration, FET1 and FET2 (PCB used for thermal tests; heat sink area 400mm²)

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics, FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	55	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = -55 ^\circ C$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = 25 ^\circ C$; see Figure 14 ; see Figure 15	1	1.5	2	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = 150 ^\circ C$; see Figure 14 ; see Figure 15	0.5	-	-	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = -55 ^\circ C$; see Figure 14 ; see Figure 15	-	-	2.3	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	0.02	3	μA
		$V_{DS} = 40 V$; $V_{GS} = 0 V$; $T_j = 150 ^\circ C$	-	-	125	μA
I_{GSS}	gate leakage current	$V_{DS} = 0 V$; $V_{GS} = 15 V$; $T_j = 25 ^\circ C$	-	2	300	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 V$; $I_D = 10 A$; $T_j = 25 ^\circ C$; see Figure 16 ; see Figure 17	-	13	15	m Ω
		$V_{GS} = 5 V$; $I_D = 10 A$; $T_j = 150 ^\circ C$; see Figure 16 ; see Figure 17	-	-	27.6	m Ω
		$V_{GS} = 4.5 V$; $I_D = 10 A$; $T_j = 25 ^\circ C$; see Figure 16 ; see Figure 17	-	14.2	16.7	m Ω
		$V_{GS} = 10 V$; $I_D = 10 A$; $T_j = 25 ^\circ C$; see Figure 16 ; see Figure 17	-	12.1	13.4	m Ω
I_D/I_{sense}	ratio of drain current to sense current	$T_j = 25 ^\circ C$; $V_{GS} = 5 V$; see Figure 18	5850	6500	7150	A/A
$S_{F(TSD)}$	temperature sense diode temperature coefficient	$I_F = 250 \mu A$; $25 ^\circ C < T_j < 150 ^\circ C$; see Figure 19	-5.4	-5.7	-6	mV/K

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{F(TSD)}$	temperature sense diode forward voltage	$I_F = 250 \mu A$; $T_j = 25^\circ C$; see Figure 19	2.855	2.9	2.945	V
Dynamic characteristics, FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 10 A$; $V_{DS} = 44 V$; $V_{GS} = 5 V$; see Figure 20	-	33	-	nC
Q_{GS}	gate-source charge		-	6.7	-	nC
Q_{GD}	gate-drain charge		-	13.3	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 V$; $V_{DS} = 25 V$; $f = 1 MHz$;	-	2450	3267	pF
C_{oss}	output capacitance	$T_j = 25^\circ C$; see Figure 21	-	360	432	pF
C_{rss}	reverse transfer capacitance		-	137	180	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V$; $R_L = 3 \Omega$; $V_{GS} = 5 V$;	-	35	-	ns
t_r	rise time	$R_{G(ext)} = 10 \Omega$	-	70	-	ns
$t_{d(off)}$	turn-off delay time		-	135	-	ns
t_f	fall time		-	61	-	ns
L_D	internal drain inductance	From pin to centre of die	-	0.85	-	nH
L_S	internal source inductance	From source lead to source bonding pad	-	1.9	-	nH
Source-drain diode, FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 10 A$; $V_{GS} = 0 V$; $T_j = 25^\circ C$; see Figure 22	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 5 A$; $dI_S/dt = -100 A/\mu s$; $V_{GS} = -10 V$;	-	44	-	ns
Q_r	recovered charge	$V_{DS} = 30 V$	-	88	-	nC

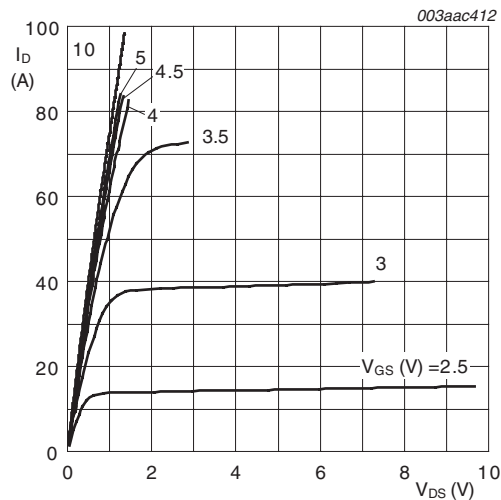

 $T_j = 25^\circ C$; $t_p = 300 \mu s$

Fig 10. Output characteristics: drain current as a function of drain-source voltage; typical values, FET1 and FET2

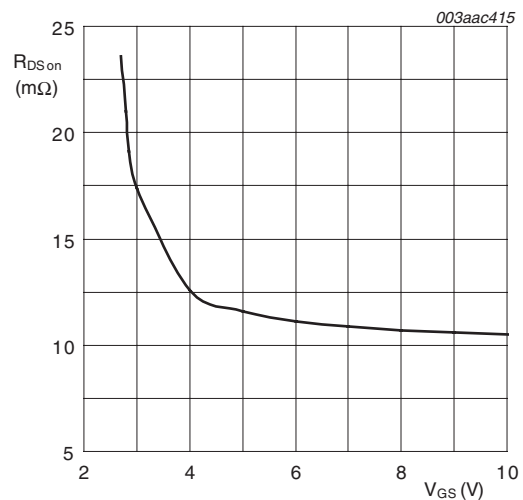

 $T_j = 25^\circ C$; $I_D = 10 A$

Fig 11. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2

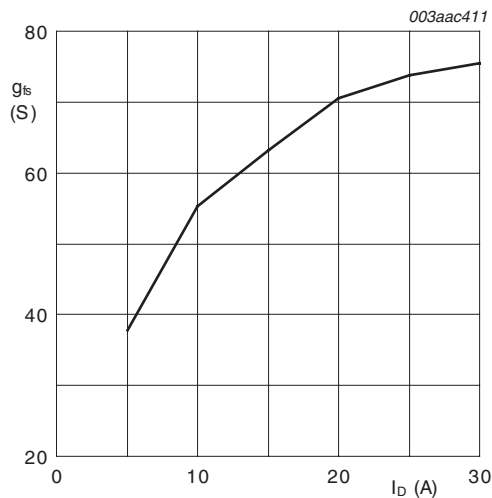


Fig 12. Forward transconductance as a function of drain current; typical values, FET1 and FET2

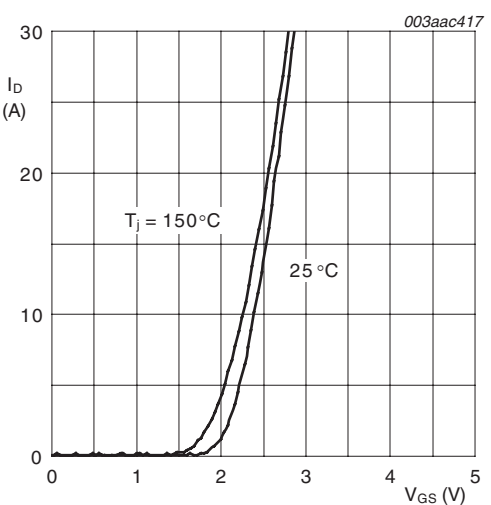


Fig 13. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2

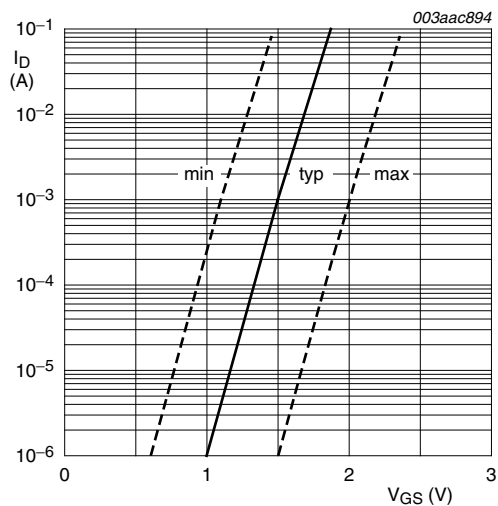


Fig 14. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2

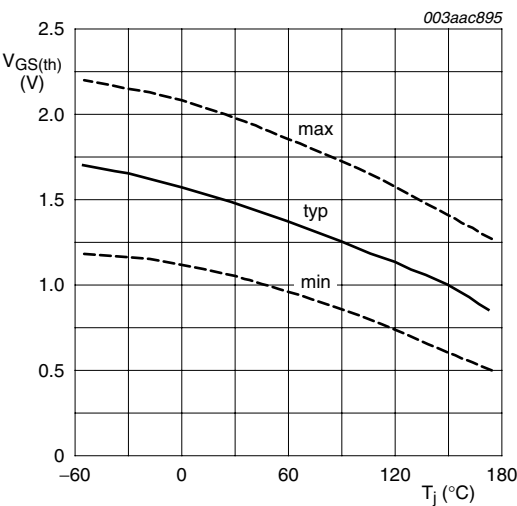


Fig 15. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

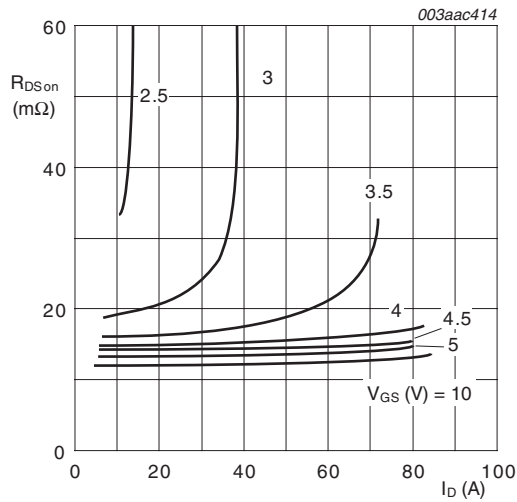


Fig 16. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2

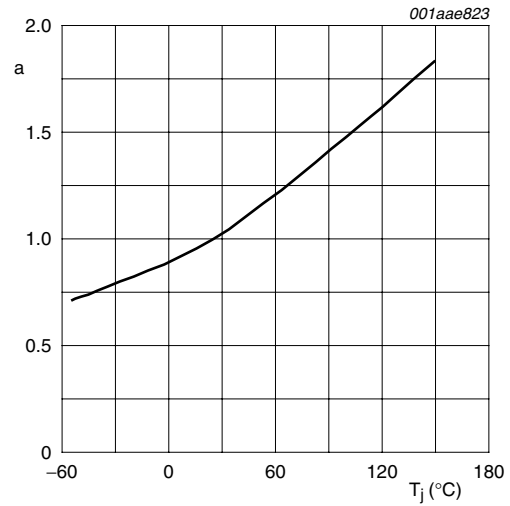


Fig 17. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2

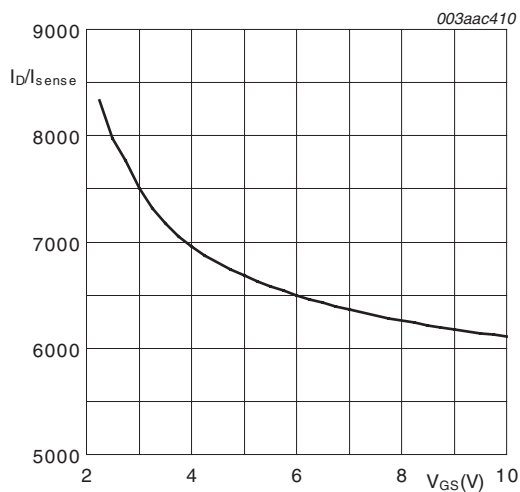


Fig 18. Ratio of drain current to sense current as a function of gate-source voltage; typical values, FET1 and FET2

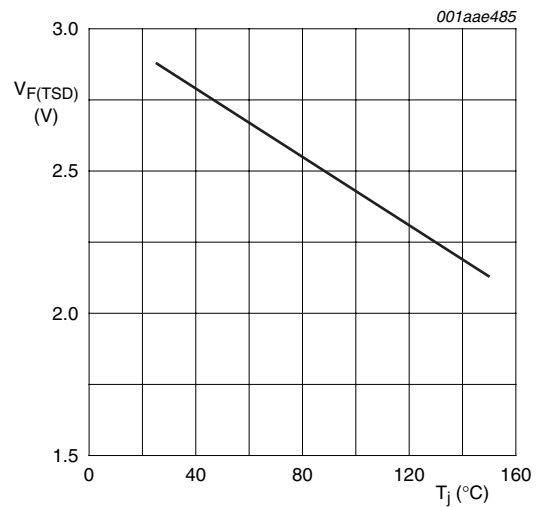
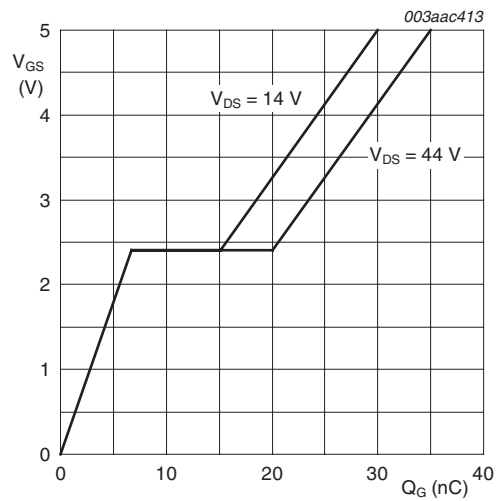
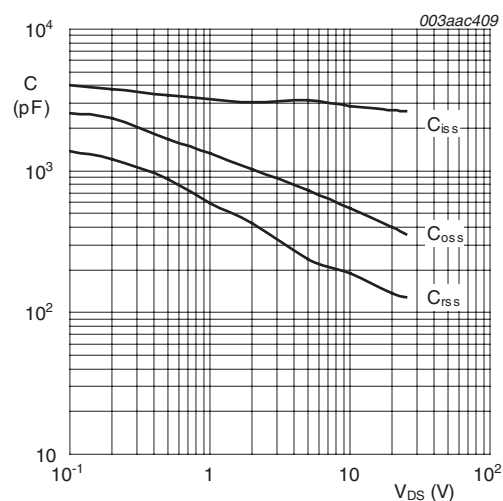


Fig 19. Temperature sense diode forward voltage as a function of junction temperature; typical values, FET1 and FET2



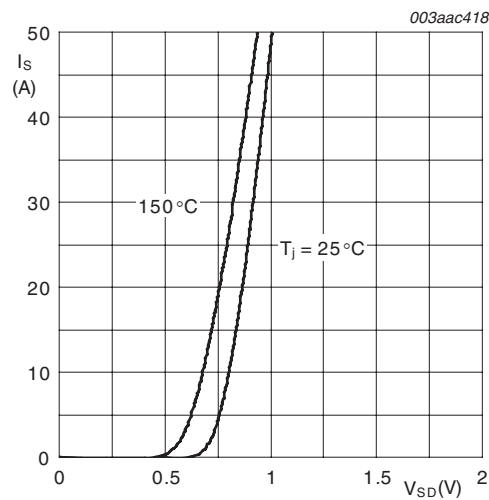
$T_j = 25\text{ }^{\circ}\text{C}; I_D = 10\text{ A}$

Fig 20. Gate-source voltage as a function of turn-on gate charge; typical values, FET1 and FET2



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 21. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2



$V_{GS} = 0\text{ V}$

Fig 22. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

7. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

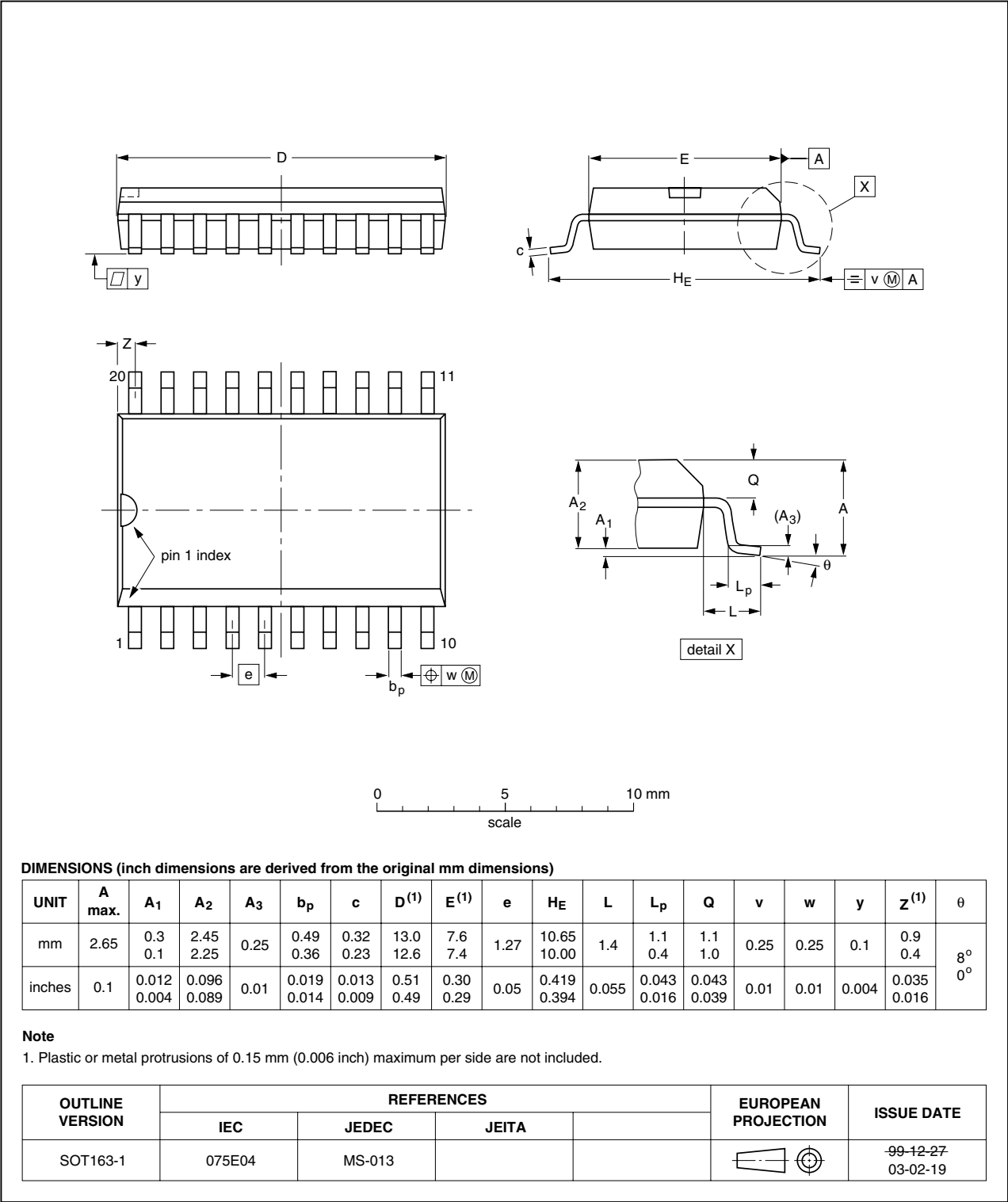


Fig 23. Package outline SOT163-1

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9MJJ-55PTT_1	20090514	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

1 Product profile1

1.1 General description1

1.2 Features and benefits1

1.3 Applications1

1.4 Quick reference data1

2 Pinning information2

3 Ordering information2

4 Limiting values3

5 Thermal characteristics5

6 Characteristics7

7 Package outline12

8 Revision history13

9 Legal information14

9.1 Data sheet status14

9.2 Definitions14

9.3 Disclaimers14

9.4 Trademarks14

10 Contact information14



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