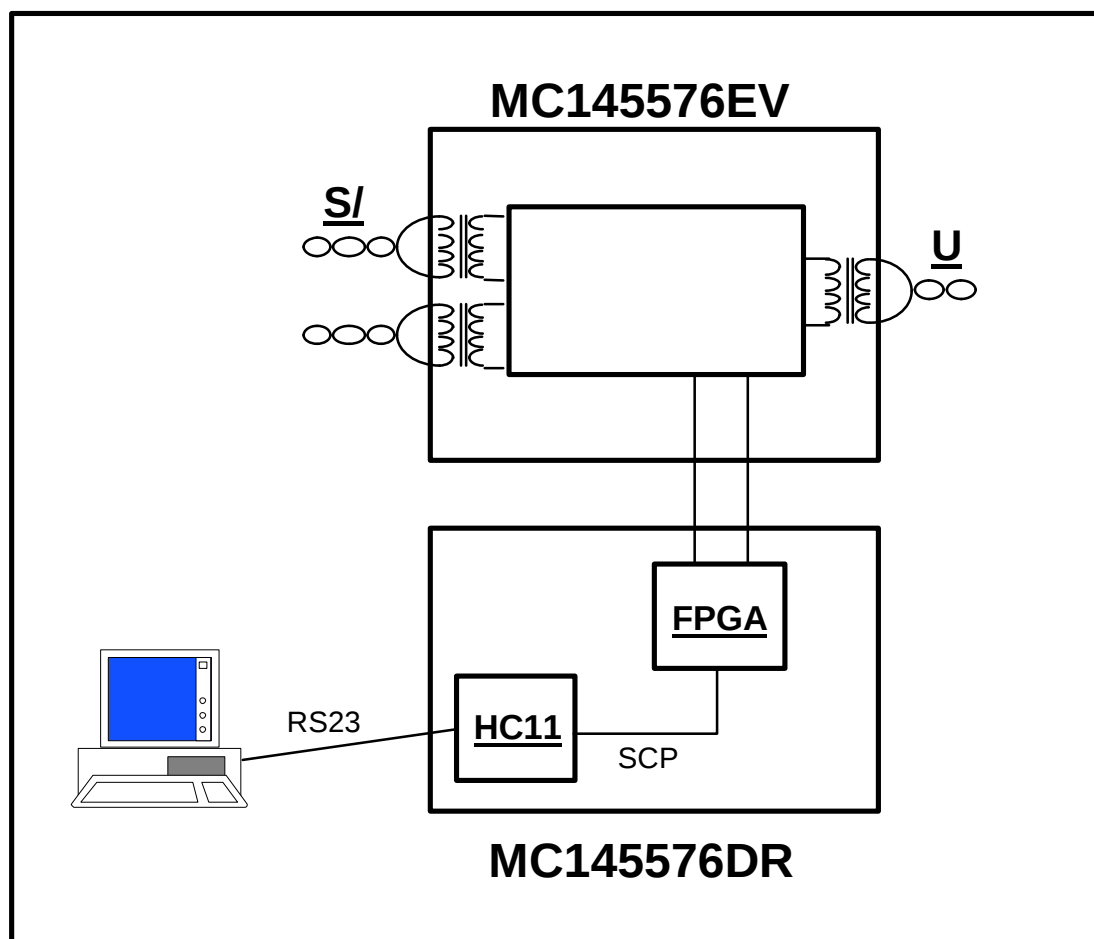


MC145576EVK

Advance Information

ISDN Single chip NT1 Transceiver Evaluation Kit



Rev 1.1

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Go to: www.freescale.com**

MC145576EVK

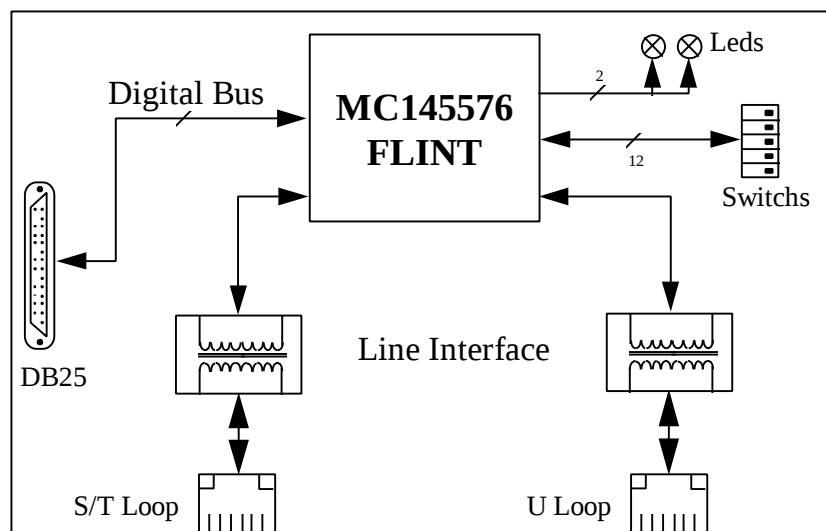
I. Introduction

The MC145576EVK board has been designed to demonstrate and evaluate the Motorola single chip NT1 solution based on the FLINT (MC145576).

The MC145576 is configured by default to work in a standard NT1 mode (see section III), this configuration can be changed to provide a terminal access to the MC145576 which is required for the SMART NT1 applications (see section IV). This terminal access can be IDL/SCP or GCI.

The MC145576EVK board is powered by an external 5V power supply, there is no power feeding circuitry which recovers the power from the U line. Another connector can be used to provide +40V power supply down to the TE through the S/T line (+40V and +5V power supplies have separated grounds).

II. MC145576EVK Block Diagram



III. MC145576 in NT1 mode

In the NT1 mode, as there is no terminal access required and where the minimum possible power consumption is desired, the MC145576 will provide a U and S/T analog interfaces and some configuration and indication pins.

Switchs configuration:

CLK_SEL	no function
ENO_L	OFF (logic high)
LED2	ON
LED1	ON
CLASS/ECHOIN	no function
FIX	OFF, Fix mode, ON, Adaptative mode

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IDL/GCI	Freescale Semiconductor, Inc.
DRQ_AR	OFF see note
PS1	OFF PS1=1, ON PS1=0
PS2	OFF PS2=1, ON PS2=0
Pulse 1	OFF /Pulse1=1, ON /Pulse1=0
Pulse 2	OFF /Pulse2=1, ON /Pulse2=0

Note: If Activation Request DRQ_AR need to be used, ENO_L should be switch ON.

IV. FLINT in Smart NT1 mode

In the Smart NT1 mode, the terminal access is required. This terminal access, plus some control and indication signals, are available on a DB25 connector (P1).

Switchs configuration:

CLK_SEL	OFF 2.048 MHz , ON 512 KHz
ENO_L	ON (logic low)
LED2	depending on the mode selected
LED1	depending on the mode selected
CLASS/ECHOIN	depending on the mode selected
FIX	OFF Fix mode, ON Adaptative mode
IDL/GCI	OFF IDL/SCP mode, ON GCI mode
DRQ_AR	depending on the mode selected
PS1	depending on the mode selected
PS2	depending on the mode selected
Pulse 1	depending on the mode selected
Pulse 2	depending on the mode selected

Note: OFF applies a logic high, ON applies a logic low.

Motorola has designed a board (based on the HC11 and a FPGA) and software (on PC) which can be directly connected to the MC145576EVK board. This board (MC145576DRV) which works only in IDL/SCP mode, provides quick access to the internal registers and gated clocks.

V. Getting Started

Jumpers configuration:

- JP8: jumper to short circuit the C13 capacitor.
- JP9: jumper to terminate the S/T loop transmit path with an 100 Ohms resistor.
- JP10: jumper to terminate the S/T loop receive path with an 100 Ohms resistor.

Getting Started

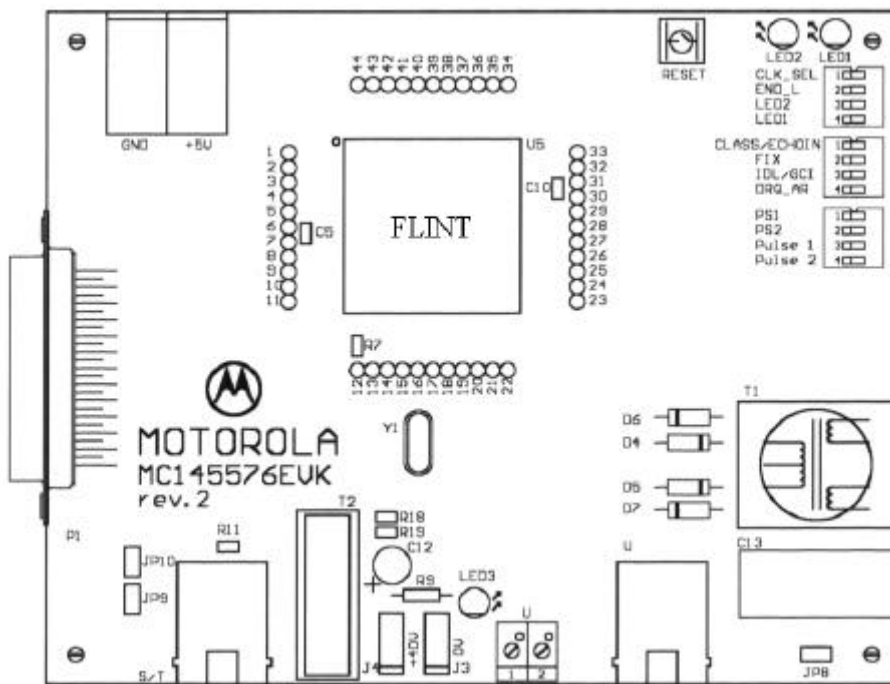
Configure the MC145576 according the mode choosen, then switch on the +5V power supply and reset the MC145576. The board is ready.

VI. Reference Manuals

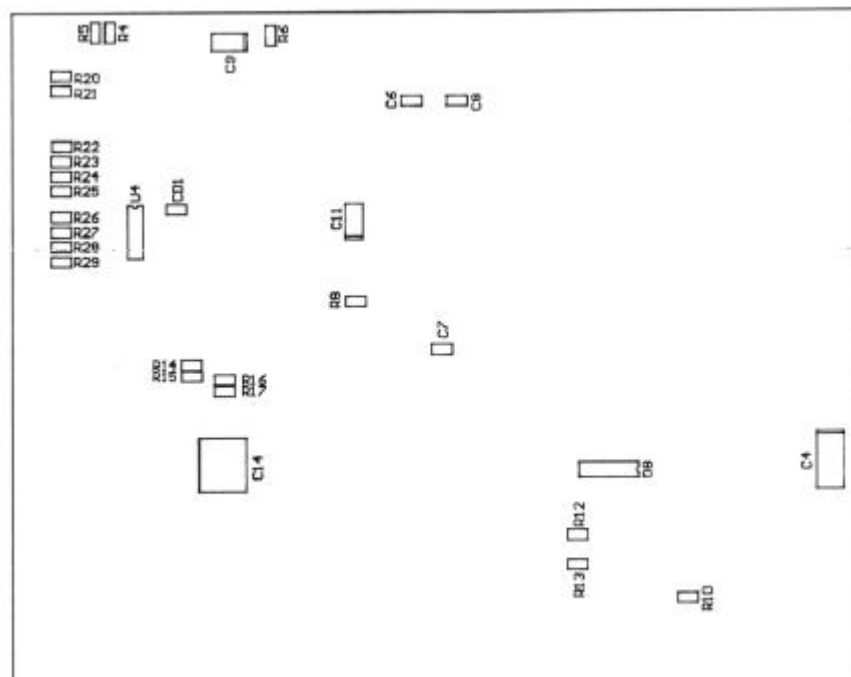
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- * MC145576 FLINT **Freescal Semiconductor, Inc.**
- * MC145574 S/T Interface User's Manual (MC145574/D).
- * MC145572 U Interface User's Manual (MC145572/D).
- * CCITT I.430 Specification.
- * ETSI ETR 300 012 Specification.
- * ETSI ETR 080 Specification.
- * GCI Interface document written by Alcatel, Italtel, GPT and Siemens.

VII. MC145576EVK Layout



Top Layer



Bottom Layer

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