

CAT24C128

128 kb I²C CMOS Serial EEPROM

Description

The CAT24C128 is a 128 kb Serial CMOS EEPROM, internally organized as 16,384 words of 8 bits each.

It features a 64-byte page write buffer and supports both the Standard (100 kHz) as well as Fast (400 kHz) I²C protocol.

Write operations can be inhibited by taking the WP pin High (this protects the entire memory).

Features

- Supports Standard and Fast I²C Protocol
- 1.8 V to 5.5 V Supply Voltage Range
- 64-Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- 8-lead PDIP, SOIC, TSSOP, MSOP and UDFN Packages
- This Device is Pb-Free, Halogen Free/BFR Free and RoHS Compliant*

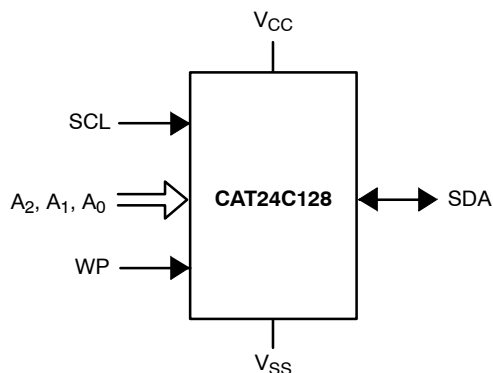


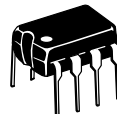
Figure 1. Functional Symbol

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

<http://onsemi.com>



PDIP-8
L SUFFIX
CASE 646AA



TSSOP-8
Y SUFFIX
CASE 948AL



SOIC-8
W SUFFIX
CASE 751BD

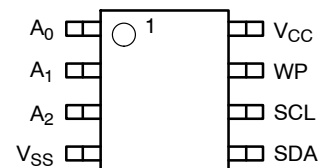


MSOP-8
Z SUFFIX
CASE 846AD



UDFN-8
HU3 SUFFIX
CASE 517AX

PIN CONFIGURATION



PDIP (L), SOIC (W), TSSOP (Y),
MSOP (Z), UDFN (HU3)

For the location of Pin 1, please consult the corresponding package drawing.

PIN FUNCTION

Pin Name	Function
A ₀ , A ₁ , A ₂	Device Address Inputs
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect Input
V _{CC}	Power Supply
V _{SS}	Ground

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

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Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	-0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than -0.5 V or higher than $V_{CC} + 0.5$ V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than $V_{CC} + 1.5$ V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program / Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
3. Page Mode, $V_{CC} = 5$ V, 25°C

Table 3. D.C. OPERATING CHARACTERISTICS ($V_{CC} = 1.8$ V to 5.5 V, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CCR}	Read Current	Read, $f_{SCL} = 400$ kHz		1	mA
I_{CCW}	Write Current	Write, $f_{SCL} = 400$ kHz		3	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC} $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		1	μA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		2	
I_L	I/O Pin Leakage	Pin at GND or V_{CC} $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		1	μA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		2	
V_{IL}	Input Low Voltage		-0.5	$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$	$V_{CC} + 0.5$	V
V_{OL1}	Output Low Voltage	$V_{CC} < 2.5$ V, $I_{OL} = 3.0$ mA		0.4	V
V_{OL2}	Output Low Voltage	$V_{CC} < 2.5$ V, $I_{OL} = 1.0$ mA		0.2	V

Table 4. PIN IMPEDANCE CHARACTERISTICS ($V_{CC} = 1.8$ V to 5.5 V, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note 4)	SDA I/O Pin Capacitance	$V_{IN} = 0$ V	8	pF
C_{IN} (Note 4)	Input Capacitance (other pins)	$V_{IN} = 0$ V	6	pF
I_{WP} (Note 5)	WP Input Current	$V_{IN} < V_{IH}$	200	μA
		$V_{IN} > V_{IH}$	1	μA

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
5. When not driven, the WP pin is pulled down to GND internally. For improved noise immunity, the internal pull-down is relatively strong; therefore the external driver must be able to supply the pull-down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer ($\sim 0.5 \times V_{CC}$), the strong pull-down reverts to a weak current source.

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Table 5. A.C. CHARACTERISTICS ($V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$) (Note 6)

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		μs
$t_{HD:DAT}$	Data Hold Time	0		0		μs
$t_{SU:DAT}$	Data Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1000		300	ns
t_F (Note 7)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		μs
t_{AA}	SCL Low to SDA Data Out		3.5		0.9	μs
t_{DH}	Data Out Hold Time	100		100		ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		μs
t_{WR}	Write Cycle Time		5		5	ms
t_{PU} (Notes 7 and 8)	Power-up to Ready Mode		1		1	ms

6. Test conditions according to "A.C. Test Conditions" table.

7. Tested initially and after a design or process change that affects this parameter.

8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. A.C. TEST CONDITIONS

Input Levels	$0.2 \times V_{CC}$ to $0.8 \times V_{CC}$
Input Rise and Fall Times	$\leq 50 \text{ ns}$
Input Reference Levels	$0.3 \times V_{CC}$, $0.7 \times V_{CC}$
Output Reference Levels	$0.5 \times V_{CC}$
Output Load	Current Source: $I_{OL} = 3 \text{ mA}$ ($V_{CC} \geq 2.5 \text{ V}$); $I_{OL} = 1 \text{ mA}$ ($V_{CC} < 2.5 \text{ V}$); $C_L = 100 \text{ pF}$

Power-On Reset (POR)

The CAT24C128 incorporates Power-On Reset (POR) circuitry which protects the device against powering up in the wrong state.

The CAT24C128 will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi-directional POR feature protects the device against 'brown-out' failure following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A₀, A₁ and A₂: The Address pins accept the device address. When not driven, these pins are pulled LOW internally.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. When not driven, this pin is pulled LOW internally.

Functional Description

The CAT24C128 supports the Inter-Integrated Circuit (I²C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24C128 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 8 devices may be connected to the bus as determined by the device address inputs A₀, A₁, and A₂.

I²C Bus Protocol

The I²C bus consists of two 'wires', SCL and SDA. The two wires are connected to the V_{CC} supply via pull-up

resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 2). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 3). The next 3 bits, A₂, A₁ and A₀, select one of 8 possible Slave devices and must match the state of the external address pins. The last bit, R/ $\overline{W}$, specifies whether a Read (1) or Write (0) operation is to be performed.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge all address bytes and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 5.

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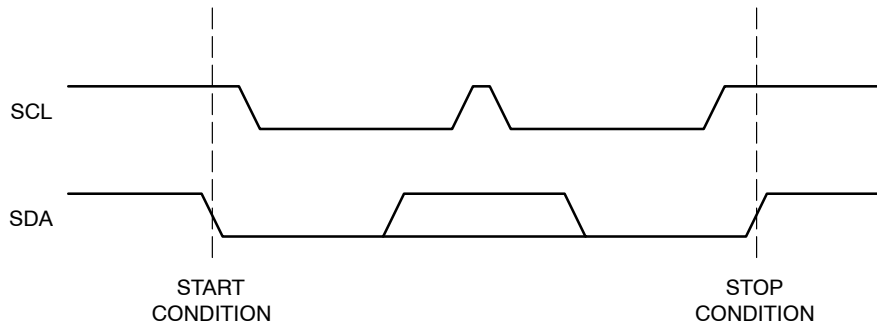


Figure 2. START/STOP Conditions

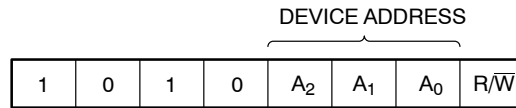


Figure 3. Slave Address Bits

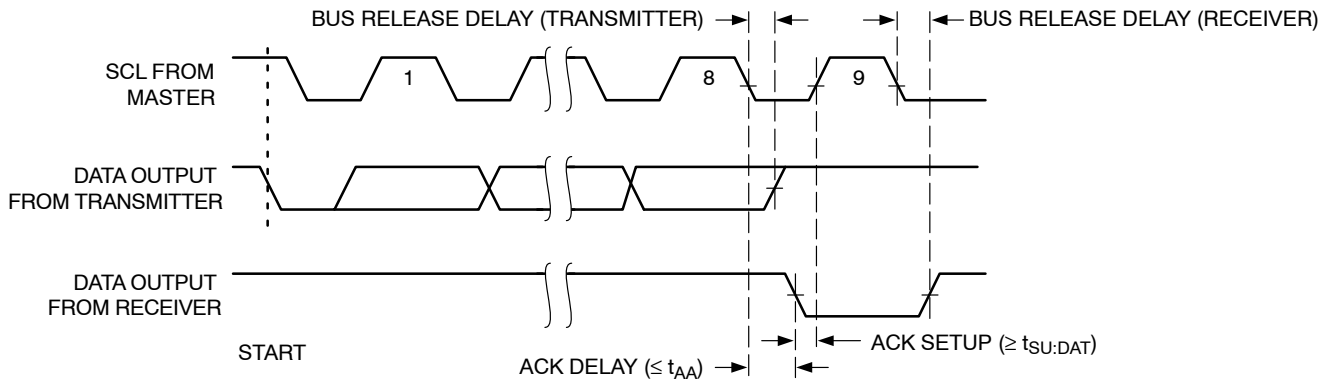


Figure 4. Acknowledge Timing

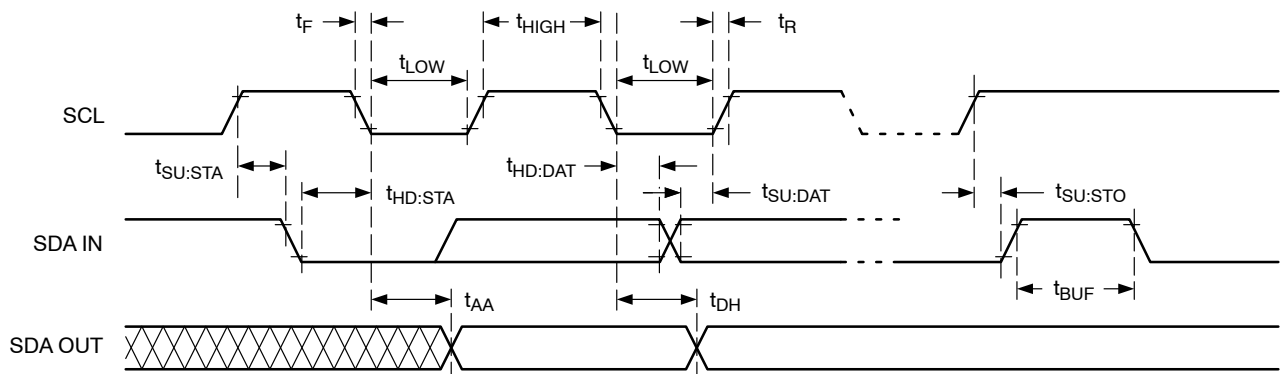


Figure 5. Bus Timing

Write Operations

Byte Write

Upon receiving a Slave address with the $R/\overline{W}$ bit set to '0', the CAT24C128 will interpret the next two bytes as address bytes. These bytes are used to initialize the internal address counter; the 2 most significant bits are 'don't care', the next 8 point to one of 256 available pages and the last 6 point to a location within a 64 byte page. A byte following the address bytes will be interpreted as data. The data will be loaded into the Page Write Buffer and will eventually be written to memory at the address specified by the 14 active address bits provided earlier. The CAT24C128 will acknowledge the Slave address, address bytes and data byte. The Master then starts the internal Write cycle by issuing a STOP condition (Figure 6). During the internal Write cycle (t_{WR}), the SDA output will be tri-stated and additional Read or Write requests will be ignored (Figure 7).

Page Write

By continuing to load data into the Page Write Buffer after the 1st data byte and before issuing the STOP condition, up to 64 bytes can be written simultaneously during one internal Write cycle (Figure 8). If more data bytes are loaded than locations available to the end of page, then loading will continue from the beginning of page, i.e. the page address is

latched and the address count automatically increments to and then wraps-around at the page boundary. Previously loaded data can thus be overwritten by new data. What is eventually written to memory reflects the latest Page Write Buffer contents. Only data loaded within the most recent Page Write sequence will be written to memory.

Acknowledge Polling

The ready/busy status of the CAT24C128 can be ascertained by sending Read or Write requests immediately following the STOP condition that initiated the internal Write cycle. As long as internal Write is in progress, the CAT24C128 will not acknowledge the Slave address.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24C128. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the CAT24C128 will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAT24C128 is shipped erased, i.e., all bytes are FFh.

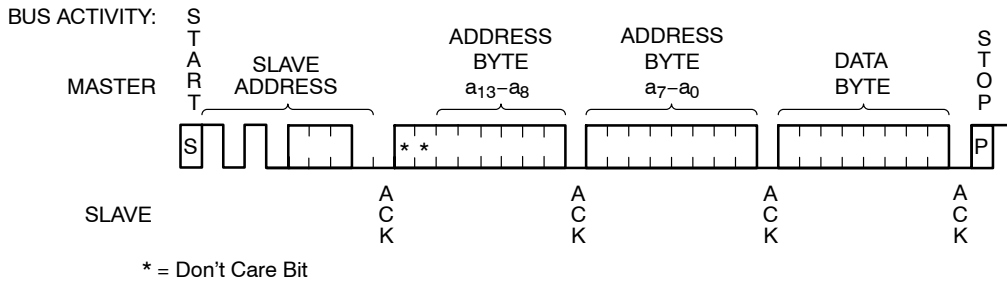


Figure 6. Byte Write Sequence

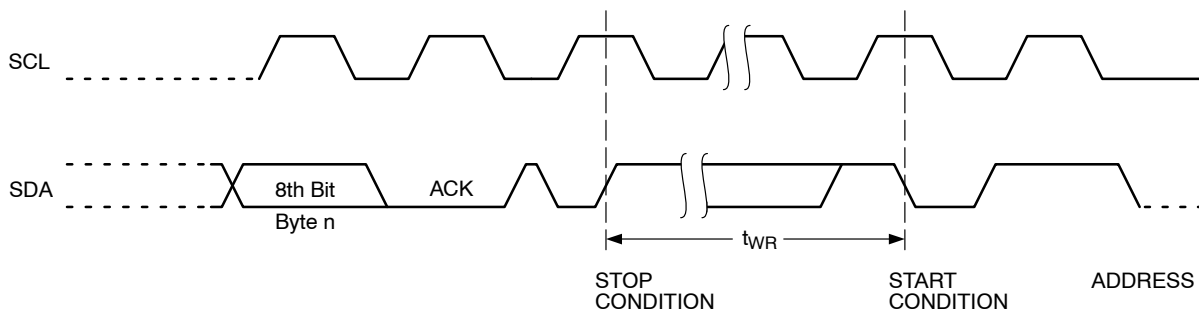


Figure 7. Write Cycle Timing

CAT24C128

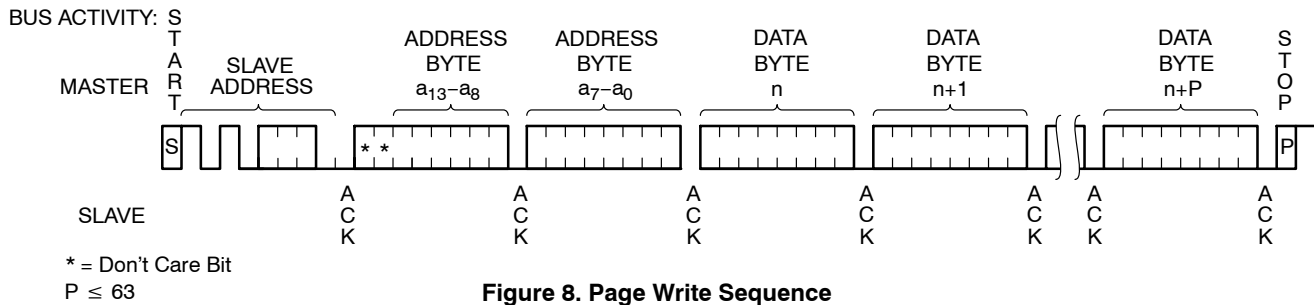


Figure 8. Page Write Sequence

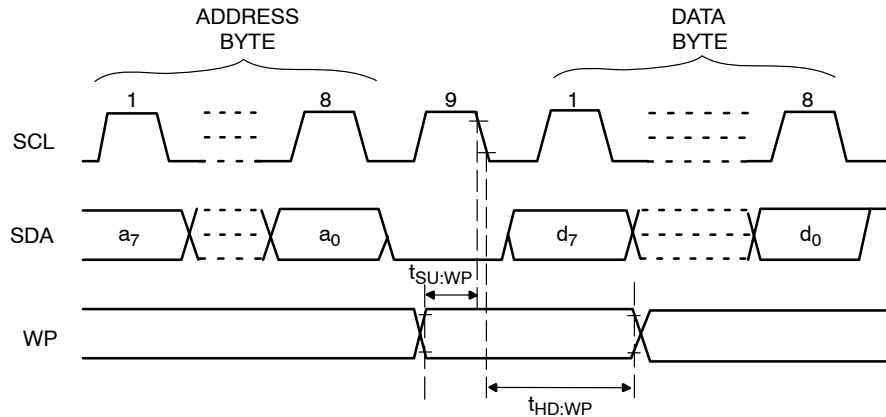


Figure 9. WP Timing

Read Operations

Immediate Read

Upon receiving a Slave address with the $R/\overline{W}$ bit set to '1', the CAT24C128 will interpret this as a request for data residing at the current byte address in memory. The CAT24C128 will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the CAT24C128 returns to Standby mode.

Selective Read

To read data residing at a specific location, the internal address counter must first be initialized as described under Byte Write. If rather than following up the two address bytes

with data, the Master instead follows up with an Immediate Read sequence, then the CAT24C128 will use the 14 active address bits to initialize the internal address counter and will shift out data residing at the corresponding location. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 11), the CAT24C128 returns to Standby mode.

Sequential Read

If during a Read session the Master acknowledges the 1st data byte, then the CAT24C128 will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap-around at end of memory (rather than end of page).

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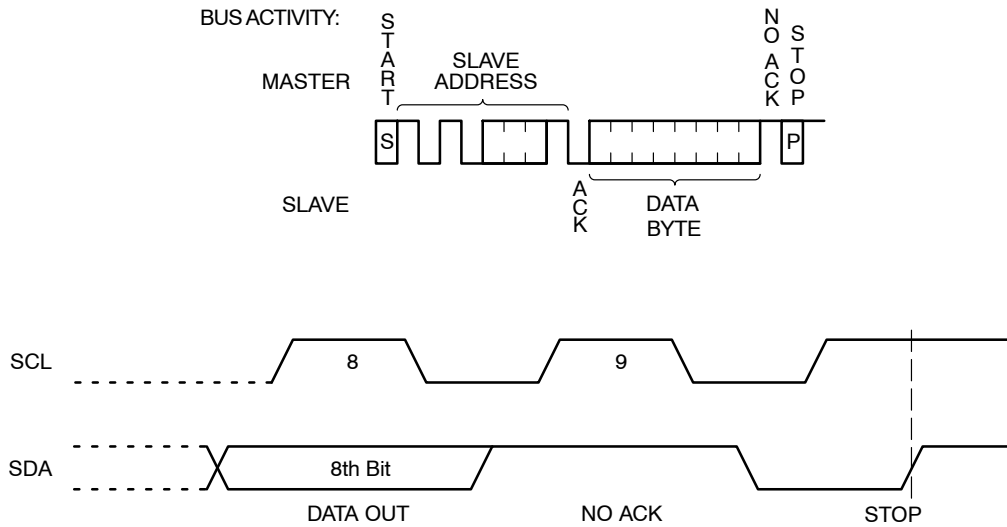


Figure 10. Immediate Read Sequence and Timing

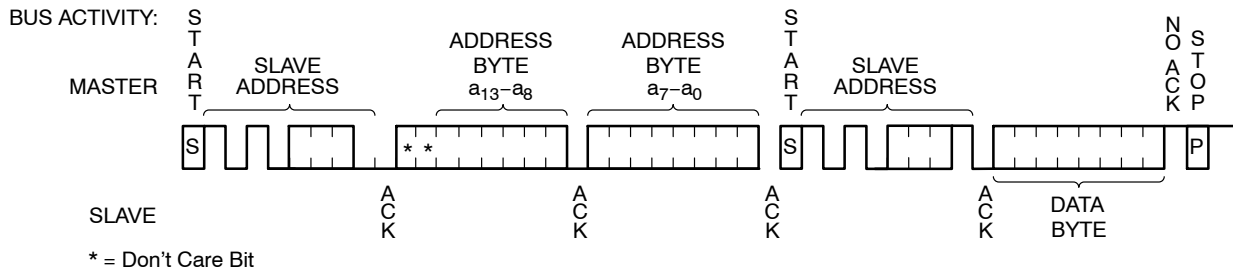


Figure 11. Selective Read Sequence

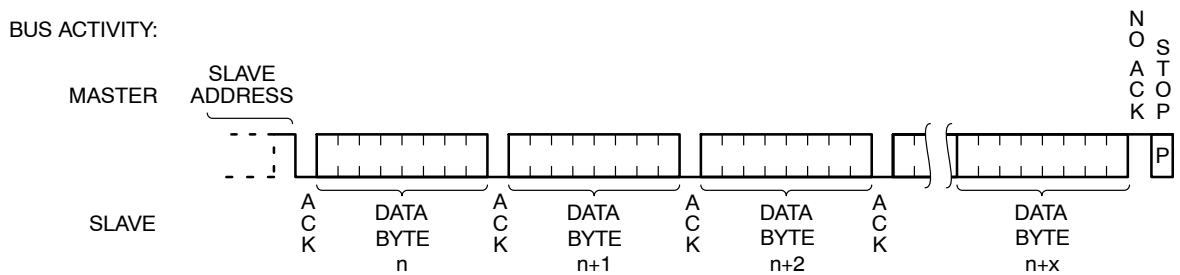
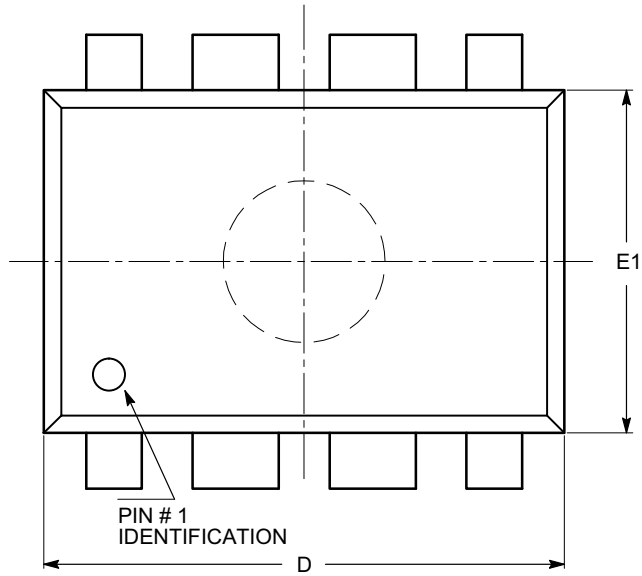


Figure 12. Sequential Read Sequence

CAT24C128

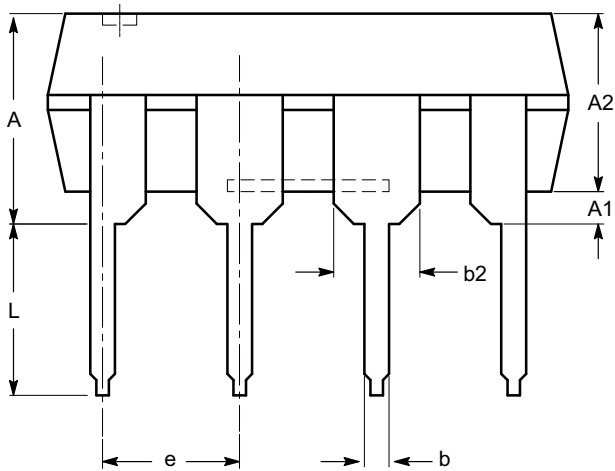
PACKAGE DIMENSIONS

PDIP-8, 300 mils
CASE 646AA-01
ISSUE A

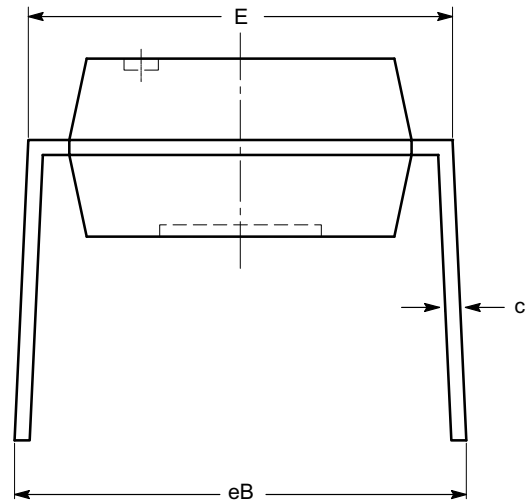


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e	2.54 BSC		
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW



END VIEW

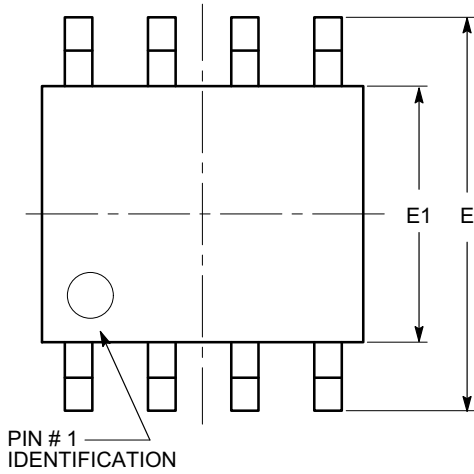
Notes:

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-001.

CAT24C128

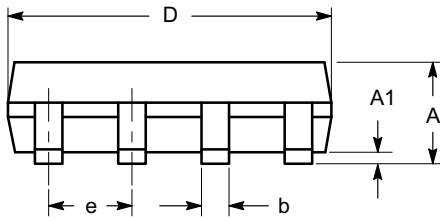
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD-01
ISSUE O

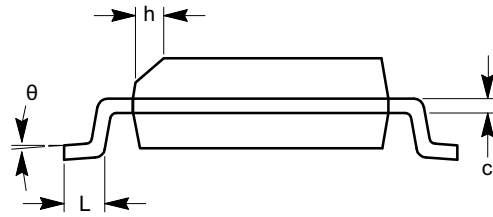


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



END VIEW

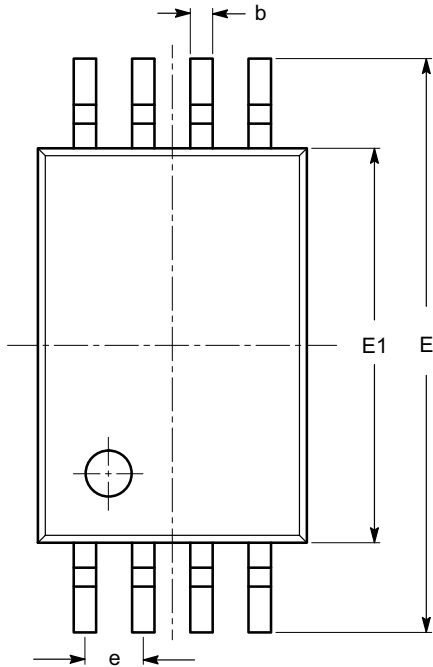
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

CAT24C128

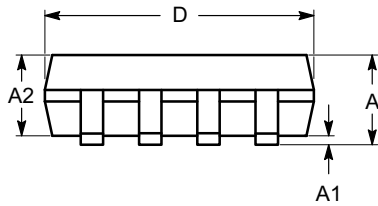
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL-01
ISSUE O

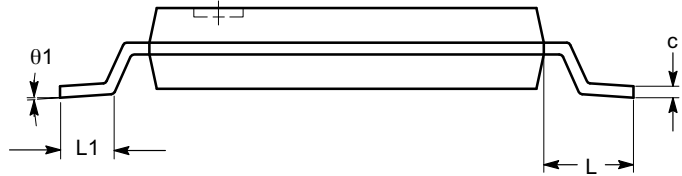


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

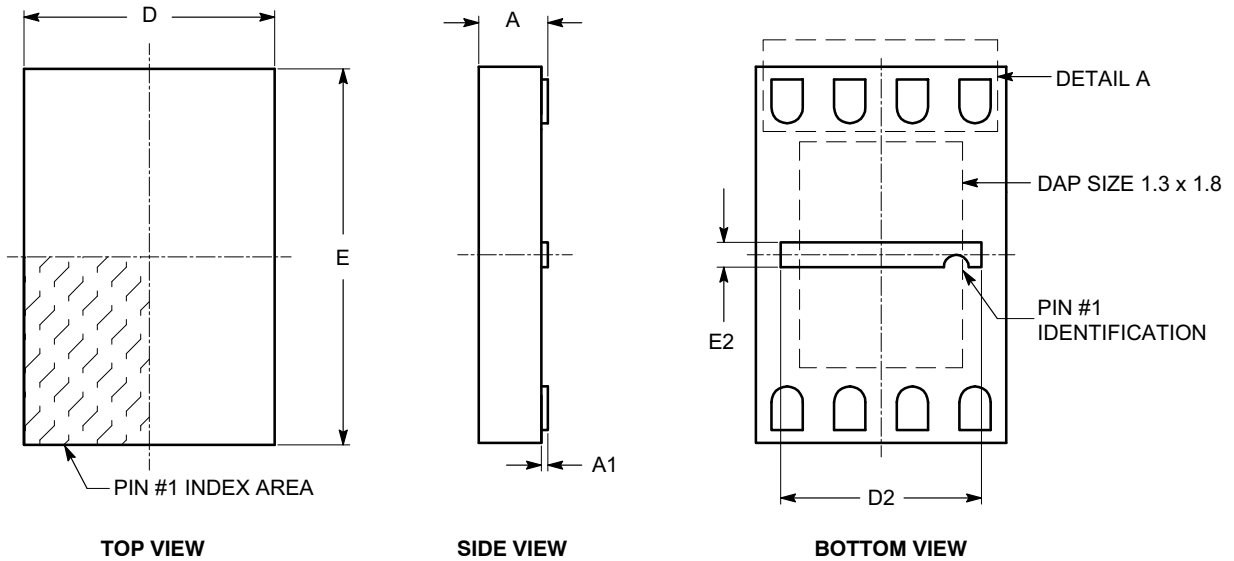
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

CAT24C128

PACKAGE DIMENSIONS

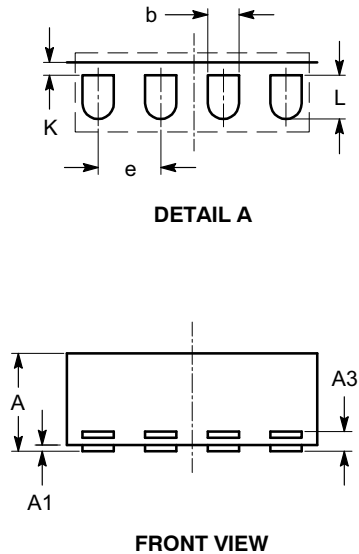
UDFN8, 2x3
CASE 517AX-01
ISSUE O



SYMBOL	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
A3	0.127 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	2.90	3.00	3.10
E2	0.10	0.20	0.30
e	0.50 TYP		
K	0.10 REF		
L	0.30	0.35	0.40

Notes:

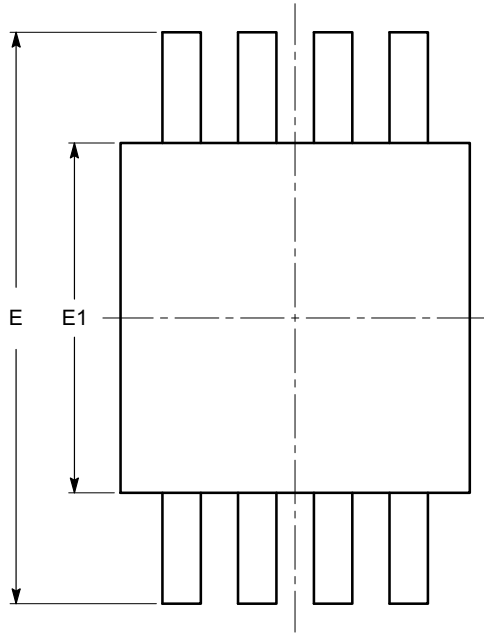
- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MO-229.



CAT24C128

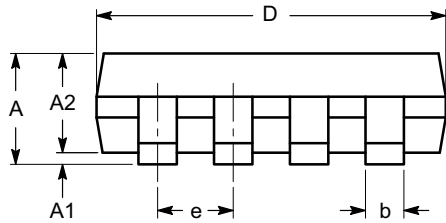
PACKAGE DIMENSIONS

MSOP 8, 3x3
CASE 846AD-01
ISSUE O

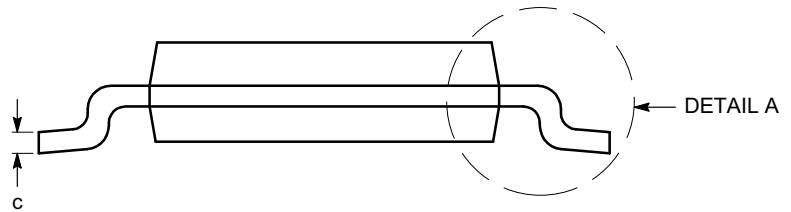


TOP VIEW

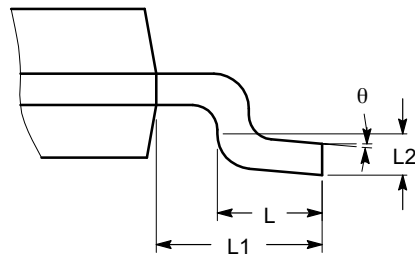
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0°		6°



SIDE VIEW



END VIEW



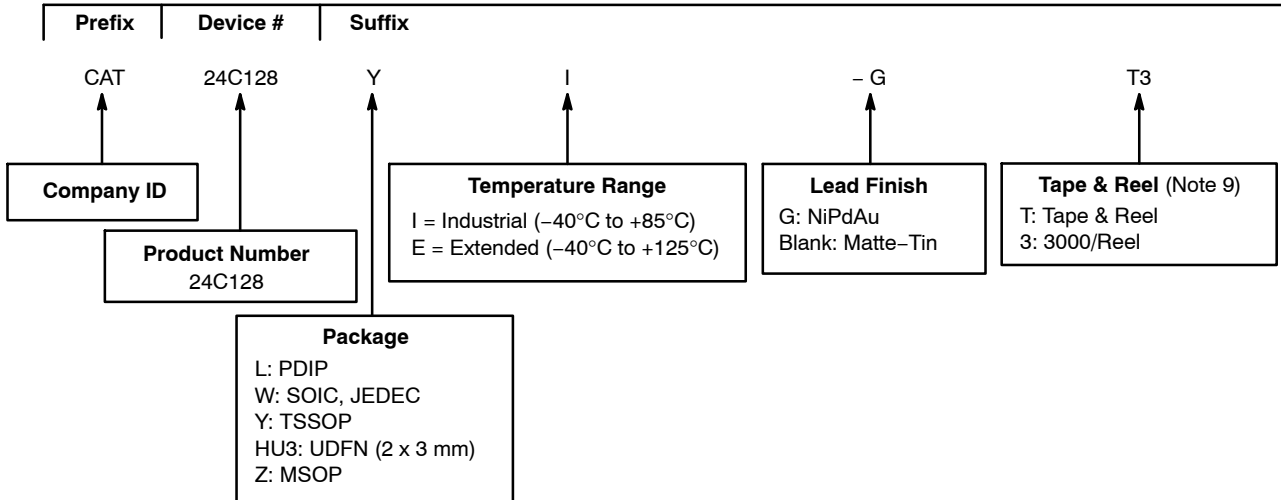
DETAIL A

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-187.

CAT24C128

Example of Ordering Information



9. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ORDERABLE PART NUMBERS

Order Number	Order Number
CAT24C128LI-G	CAT24C128LE-G
CAT24C128WI-GT3	CAT24C128WE-GT3
CAT24C128YI-GT3	CAT24C128YE-GT3
CAT24C128HU3IGT3*	CAT24C128HU3EGT3*
CAT24C128ZI-GT3	CAT24C128ZE-GT3

*Part number is not exactly the same as the "Example of Ordering Information" shown above.
For part numbers marked with "*" there are NO hyphens in the orderable part numbers.

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