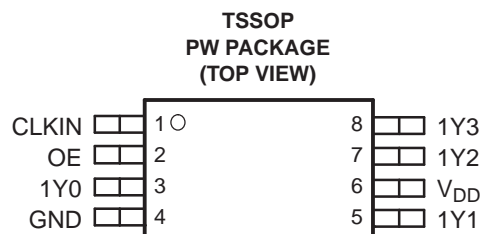


200-MHz GENERAL-PURPOSE CLOCK BUFFER, PCI-X COMPLIANT

FEATURES

- General-Purpose and PCI-X 1:4 Clock Buffer
- Operating Frequency
 - 0 MHz to 200 MHz General-Purpose
- Low Output Skew: <100 ps
- Distributes One Clock Input to One Bank of Four Outputs
- Output Enable Control that Drives Outputs Low when OE is Low
- Operates from Single 3.3-V Supply or 2.5-V Supply
- PCI-X Compliant
- 8-Pin TSSOP Package

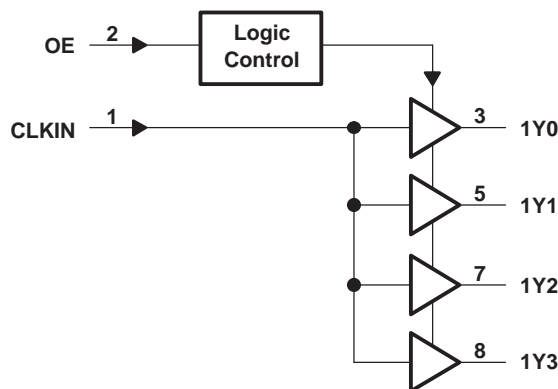


DESCRIPTION

The CDCV304 is a high-performance, low-skew, general-purpose PCI-X compliant clock buffer. It distributes one input clock signal (CLKIN) to the output clocks (1Y[0:3]). It is specifically designed for use with PCI-X applications. The CDCV304 operates at 3.3 V and 2.5 V and is therefore compliant to the 3.3-V PCI-X specifications.

The CDCV304 is characterized for operation from –40°C to 85°C for automotive and industrial applications.

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
CLKIN	OE	1Y[0:3]
L	L	L
H	L	L
L	H	L
H	H	H



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
1Y[0:3]	3, 5, 7, 8	O	Buffered output clocks
CLKIN	1	I	Input reference frequency
GND	4	Power	Ground
OE	2	I	Output enable control
V _{DD}	6	Power	Supply

THERMAL INFORMATION

CDCV304PW 8-PIN TSSOP				THERMAL AIR FLOW (CFM)				UNIT
				0	150	250	500	
R _{θJA}	High K			149	142	138	132	°C/W
R _{θJA}	Low K			230	185	170	150	°C/W
R _{θJC}	High K	65						°C/W
R _{θJC}	High K	69						°C/W

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

	UNIT
Supply voltage range, V _{DD}	−0.5 V to 4.3 V
Input voltage range, V _I ⁽²⁾⁽³⁾	−0.5 V to V _{DD} + 0.5 V
Output voltage range, V _O ⁽²⁾⁽³⁾	−0.5 V to V _{DD} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD})	±50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD})	±50 mA
Continuous total output current, I _O (V _O = 0 to V _{DD})	±50 mA
Package thermal impedance, θ _{JA} : PW package	230.5°C/W
Storage temperature range T _{stg}	−65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This value is limited to 4.6 V maximum.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V _{DD}	2.3		3.6	V
Low-level input voltage, V _{IL}			0.3 x V _{DD}	V
High-level input voltage, V _{IH}	0.7 x V _{DD}			V
Input voltage, V _I	0		V _{DD}	V
High-level output current, I _{OH}	V _{DD} = 2.5 V		−12	mA
	V _{DD} = 3.3 V		−24	
Low-level output current, I _{OL}	V _{DD} = 2.5 V		12	mA
	V _{DD} = 3.3 V		24	
Operating free-air temperature, T _A	−40		85	°C

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Clock frequency		0		200	MHz

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input voltage	$V_{\text{DD}} = 3 \text{ V}$, $I_{\text{I}} = -18 \text{ mA}$			-1.2	V
V_{OH}	High-level output voltage	$V_{\text{DD}} = 2.3 \text{ V}$, $I_{\text{OH}} = -8 \text{ mA}$		1.8		V
		$V_{\text{DD}} = 2.3 \text{ V}$, $I_{\text{OH}} = -16 \text{ mA}$		1.5		
		$V_{\text{DD}} = \text{min to max}$, $I_{\text{OH}} = -1 \text{ mA}$		$V_{\text{DD}} - 0.2$		
		$V_{\text{DD}} = 3 \text{ V}$, $I_{\text{OH}} = -24 \text{ mA}$		2		
		$V_{\text{DD}} = 3 \text{ V}$, $I_{\text{OH}} = -12 \text{ mA}$		2.4		
V_{OL}	Low-level output voltage	$V_{\text{DD}} = 2.3 \text{ V}$, $I_{\text{OL}} = 8 \text{ mA}$			0.5	V
		$V_{\text{DD}} = 2.3 \text{ V}$, $I_{\text{OL}} = 16 \text{ mA}$			0.7	
		$V_{\text{DD}} = \text{min to max}$, $I_{\text{OL}} = 1 \text{ mA}$			0.2	
		$V_{\text{DD}} = 3 \text{ V}$, $I_{\text{OL}} = 24 \text{ mA}$			0.8	
		$V_{\text{DD}} = 3 \text{ V}$, $I_{\text{OL}} = 12 \text{ mA}$			0.55	
I_{OH}	High-level output current	$V_{\text{DD}} = 3 \text{ V}$, $V_{\text{O}} = 1 \text{ V}$	-50			mA
		$V_{\text{DD}} = 3.3 \text{ V}$, $V_{\text{O}} = 1.65 \text{ V}$		-55		
I_{OL}	Low-level output current	$V_{\text{DD}} = 3 \text{ V}$, $V_{\text{O}} = 2 \text{ V}$	60			mA
		$V_{\text{DD}} = 3.3 \text{ V}$, $V_{\text{O}} = 1.65 \text{ V}$		70		
I_{I}	Input current	$V_{\text{I}} = V_{\text{O}}$ or V_{DD}			± 5	μA
I_{DD}	Dynamic current, see Figure 5	$f = 67 \text{ MHz}$, $V_{\text{DD}} = 2.7 \text{ V}$			28	mA
		$f = 67 \text{ MHz}$, $V_{\text{DD}} = 3.6 \text{ V}$			37	
C_{I}	Input capacitance	$V_{\text{DD}} = 3.3 \text{ V}$, $V_{\text{I}} = 0 \text{ V}$ or V_{DD}		3		pF
C_{O}	Output capacitance	$V_{\text{DD}} = 3.3 \text{ V}$, $V_{\text{I}} = 0 \text{ V}$ or V_{DD}		3.2		pF

(1) All typical values are with respect to nominal V_{DD} and $T_{\text{A}} = 25^{\circ}\text{C}$.

SWITCHING CHARACTERISTICS

$V_{\text{DD}} = 2.5 \text{ V} \pm 10\%$, $C_{\text{L}} = 10 \text{ pF}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Low-to-high propagation delay	See Figure 1 and Figure 2	2	2.9	4.5	ns
t_{PHL}	High-to-low propagation delay		2	3	4.5	
$t_{\text{sk(o)}}$	Output skew ⁽²⁾	See Figure 3		50	150	ps
t_{r}	Output rise slew rate		1.5	2.2	4	V/ns
t_{f}	Output fall slew rate		1.5	2.2	4	V/ns

(1) All typical values are with respect to nominal V_{DD} .

(2) The $t_{\text{sk(o)}}$ specification is only valid for equal loading of all outputs.

SWITCHING CHARACTERISTICS

$V_{DD} = 3.3\text{ V} \pm 10\%$, $C_L = 10\text{ pF}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Low-to-high propagation delay	See Figure 1 and Figure 2	1.8	2.4	3	ns
t_{PHL}	High-to-low propagation delay		1.8	2.5	3	
$t_{sk(o)}$	Output skew ⁽²⁾			50	100	ps
t_{jitter}	Additive phase jitter from input to output 1Y0	12 kHz to 5 MHz, $f_{out} = 30.72\text{ MHz}$		63		fs rms
		12 kHz to 20 MHz, $f_{out} = 125\text{ MHz}$		56		
$t_{sk(p)}$	Pulse skew	$V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$			150	ps
$t_{sk(pr)}$	Process skew			0.2	0.3	ns
$t_{sk(pp)}$	Part-to-part skew			0.25	0.4	ns
t_{high}	Clock high time, see Figure 4	66 MHz	6			ns
		140 MHz	3			
t_{low}	Clock low time, see Figure 4	66 MHz	6			ns
		140 MHz	3			
t_r	Output rise slew rate ⁽³⁾	$V_O = 0.4\text{ V}$ to 2 V	1.5	2.7	4	V/ns
t_f	Output fall slew rate ⁽³⁾	$V_O = 2\text{ V}$ to 0.4 V	1.5	2.7	4	V/ns

(1) All typical values are with respect to nominal V_{DD} .

(2) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

(3) This symbol is according to PCI-X terminology.

PARAMETER MEASUREMENT INFORMATION

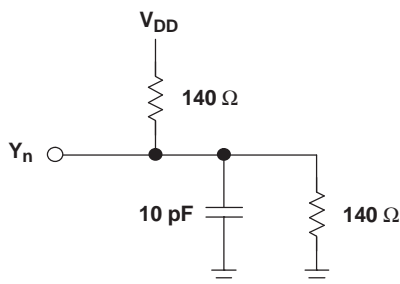


Figure 1. Test Load Circuit

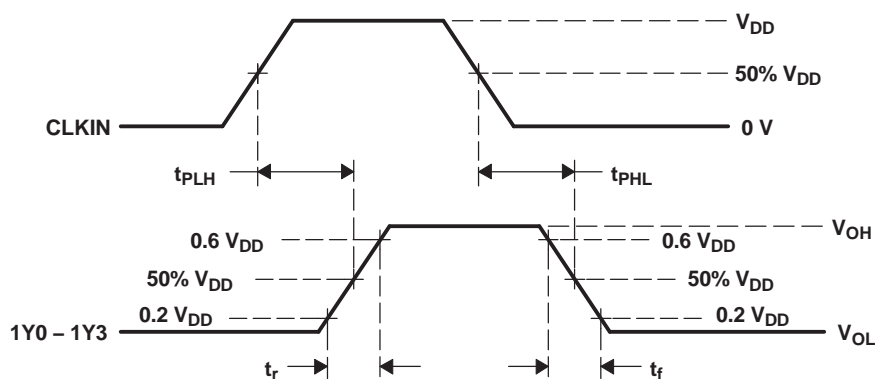


Figure 2. Voltage Waveforms Propagation Delay (t_{pd}) Measurements

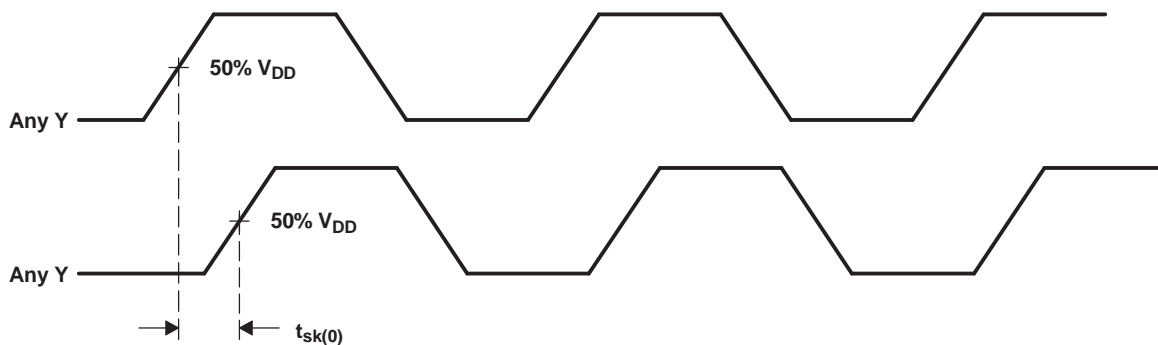
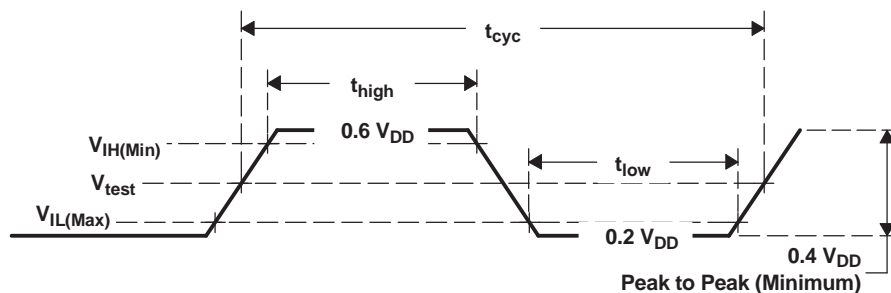


Figure 3. Output Skew

PARAMETER	VALUE	UNIT
$V_{IH}(\text{Min})$	$0.5 V_{DD}$	V
$V_{IL}(\text{Max})$	$0.35 V_{DD}$	V
V_{test}	$0.4 V_{DD}$	V



A. All parameters in [Figure 4](#) are according to PCI-X 1.0 specifications.

Figure 4. Clock Waveform

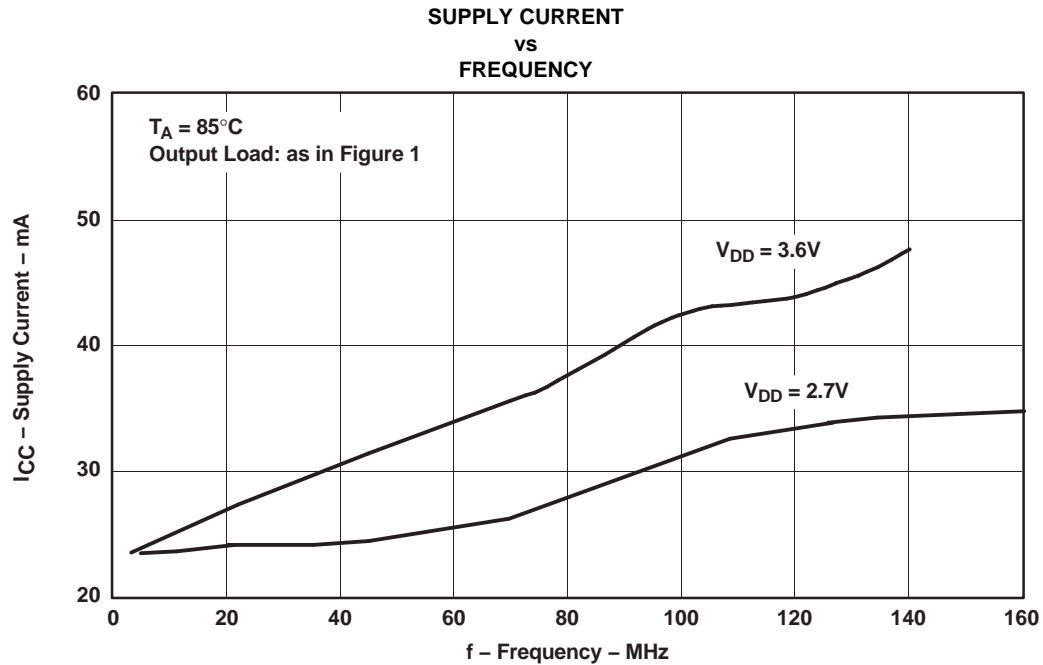


Figure 5.

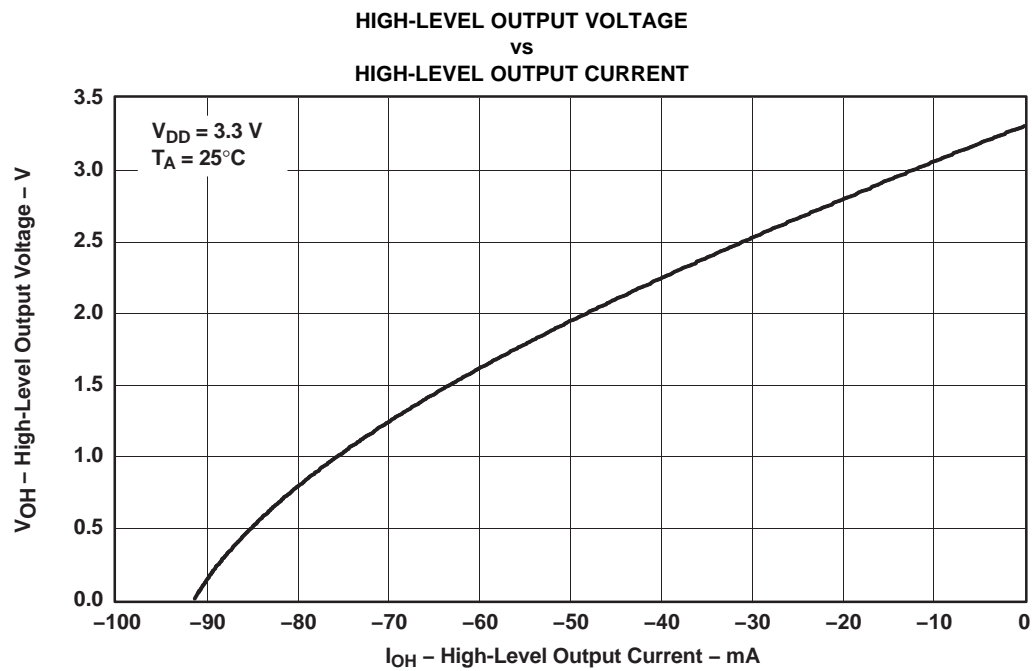


Figure 6.

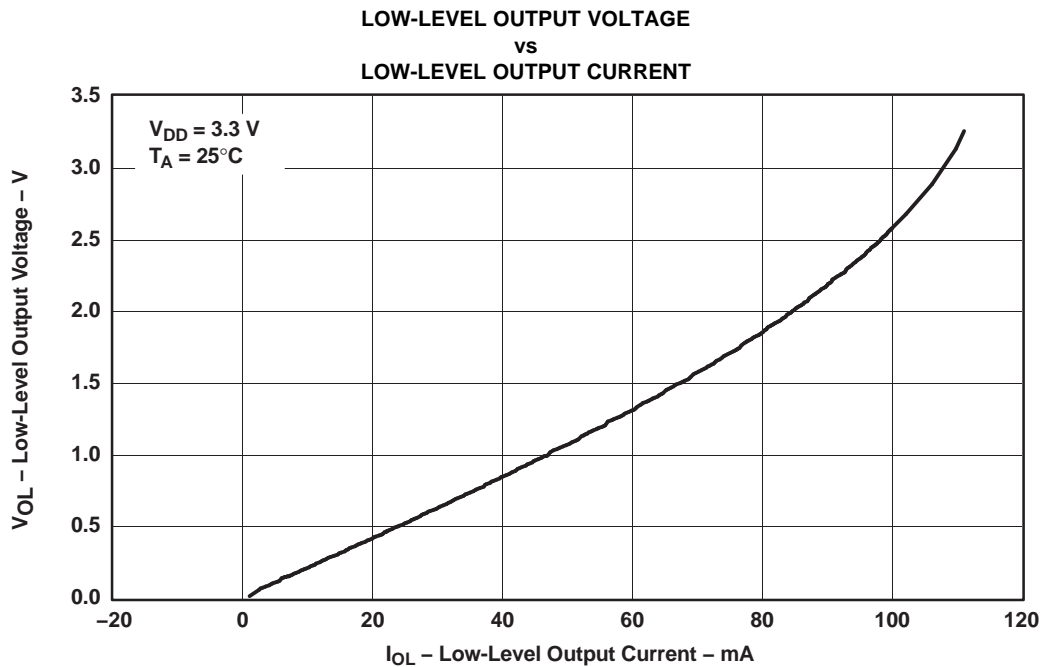


Figure 7.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDCV304PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV304PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV304PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCV304PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCV304PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCV304PWR	TSSOP	PW	8	2000	346.0	346.0	29.0

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

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