

Single, Low Voltage Digitally Controlled Potentiometer (XDCP™)

ISL23315

The ISL23315 is a volatile, low voltage, low noise, low power, I²C Bus™, 256 Taps, single digitally controlled potentiometer (DCP), which integrates DCP core, wiper switches and control logic on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I²C bus interface. The potentiometer has an associated volatile Wiper Register (WR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. When powered on, the ISL23315's wiper will always commence at mid-scale (128 tap position).

The low voltage, low power consumption, and small package of the ISL23315 make it an ideal choice for use in battery operated equipment. In addition, the ISL23315 has a V_{LOGIC} pin allowing down to 1.2V bus operation, independent from the V_{CC} value. This allows for low logic levels to be connected directly to the ISL23315 without passing through a voltage level shifter.

The DCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Applications

- Power supply margining
- RF power amplifier bias compensation
- LCD bias compensation
- Laser diode bias compensation

Features

- 256 resistor taps
- I²C serial interface
 - No additional level translator for low bus supply
 - Two address pins allow up to four devices per bus
- Wiper resistance: 70Ω typical @ V_{CC} = 3.3V
- Shutdown Mode - forces the DCP into an end-to-end open circuit and R_W is shorted to R_L internally
- Power-on preset to mid-scale (128 tap position)
- Standby current <2.5μA max
- Shutdown current <2μA max
- Power supply
 - V_{CC} = 1.7V to 5.5V analog power supply
 - V_{LOGIC} = 1.2V to 5.5V I²C bus/logic power supply
- DCP terminal voltage from 0V to V_{CC}
- 10kΩ, 50kΩ or 100kΩ total resistance
- Extended industrial temperature range: -40°C to +125°C
- 10 Ld MSOP or 10 Ld μTQFN packages
- Pb-free (RoHS compliant)

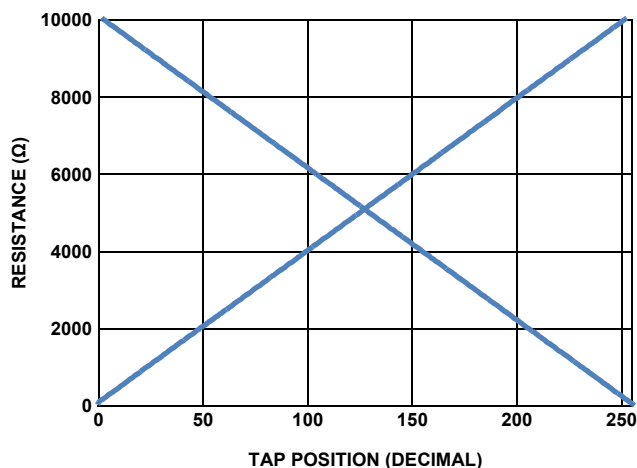


FIGURE 1. FORWARD AND BACKWARD RESISTANCE vs TAP POSITION, 10k DCP

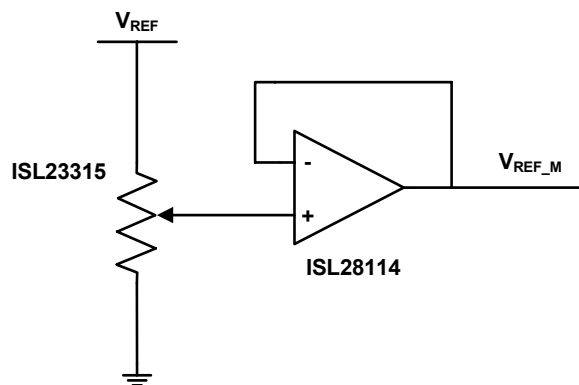
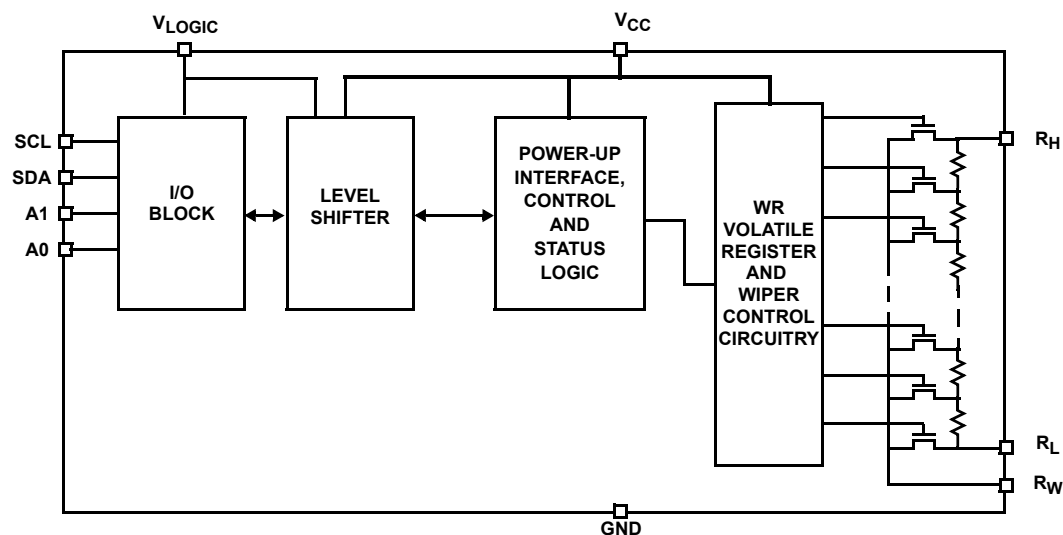
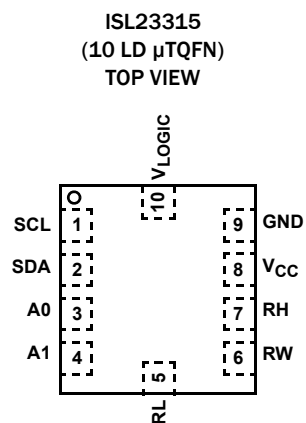
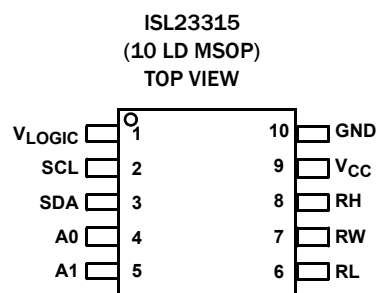


FIGURE 2. V_{REF} ADJUSTMENT

Block Diagram



Pin Configurations



Pin Descriptions

MSOP	μ TQFN	SYMBOL	DESCRIPTION
1	10	V _{LOGIC}	I ² C bus /logic supply. Range 1.2V to 5.5V
2	1	SCL	Logic Pin - Serial bus clock input
3	2	SDA	Logic Pin - Serial bus data input/open drain output
4	3	A0	Logic Pin - Hardwire slave address pin for I ² C serial bus. Range: V _{LOGIC} or GND
5	4	A1	Logic Pin - Hardwire slave address pin for I ² C serial bus. Range: V _{LOGIC} or GND
6	5	RL	DCP "low" terminal
7	6	RW	DCP wiper terminal
8	7	RH	DCP "high" terminal
9	8	V _{CC}	Analog power supply. Range 1.7V to 5.5V
10	9	GND	Ground pin

Ordering Information

PART NUMBER (Note 5)	PART MARKING	RESISTANCE OPTION (k Ω)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL23315TFUZ (Notes 1, 3)	3315T	100	-40 to +125	10 Ld MSOP	M10.118
ISL23315UFUZ (Notes 1, 3)	3315U	50	-40 to +125	10 Ld MSOP	M10.118
ISL23315WFUZ (Notes 1, 3)	3315W	10	-40 to +125	10 Ld MSOP	M10.118
ISL23315TFRUZ-T7A (Notes 2, 4)	HB	100	-40 to +125	10 Ld 2.1x1.6 μ TQFN	L10.2.1x1.6A
ISL23315TFRUZ-TK (Notes 2, 4)	HB	100	-40 to +125	10 Ld 2.1x1.6 μ TQFN	L10.2.1x1.6A
ISL23315UFRUZ-T7A (Notes 2, 4)	HA	50	-40 to +125	10 Ld 2.1x1.6 μ TQFN	L10.2.1x1.6A
ISL23315UFRUZ-TK (Notes 2, 4)	HA	50	-40 to +125	10 Ld 2.1x1.6 μ TQFN	L10.2.1x1.6A
ISL23315WFRUZ-T7A (Notes 2, 4)	GZ	10	-40 to +125	10 Ld 2.1x1.6 μ TQFN	L10.2.1x1.6A
ISL23315WFRUZ-TK (Notes 2, 4)	GZ	10	-40 to +125	10 Ld 2.1x1.6 μ TQFN	L10.2.1x1.6A

NOTES:

1. Add "-T*" suffix for Tape and Reel option. Please refer to [TB347](#) for details on reel specifications.
2. Please refer to [TB347](#) for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), please see device information page for [ISL23315](#). For more information on MSL please see techbrief [TB363](#).

Absolute Maximum Ratings

Supply Voltage Range	
V _{CC}	-0.3V to 6.0V
V _{LOGIC}	-0.3V to 6.0V
Voltage on Any DCP Terminal Pin	-0.3V to 6.0V
Voltage on Any Digital Pins	-0.3V to 6.0V
Wiper current I _W (10s)	±6mA
ESD Rating	
Human Body Model (Tested per JESD22-A114E)	6.5kV
CDM Model (Tested per JESD22-A114E)	1kV
Machine Model (Tested per JESD22-A115-A)	200V
Latch Up	
(Tested per JESD-78B; Class 2, Level A)	100mA @ +125°C

Thermal Information

Thermal Resistance (Typical)	θ _{JA} (°C/W)	θ _{JC} (°C/W)
10 Ld MSOP Package (Notes 6, 7)	170	70
10 Ld μTQFN Package (Notes 6, 7)	145	90
Maximum Junction Temperature (Plastic Package)	+150°C	
Storage Temperature Range	-65°C to +150°C	
Pb-Free Reflow Profile	see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp	

Recommended Operating Conditions

Temperature	-40°C to +125°C
V _{CC} Supply Voltage	1.7V to 5.5V
V _{LOGIC} Supply Voltage	1.2V to 5.5V
DCP Terminal Voltage	0 to V _{CC}
Max Wiper Current	±3mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. For θ_{JC}, the “case temp” location is the center top of the package.

Analog Specifications

V_{CC} = 2.7V to 5.5V, V_{LOGIC} = 1.2V to 5.5V over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
R _{TOTAL}	R _H to R _L resistance	W option		10		kΩ
		U option		50		kΩ
		T option		100		kΩ
	R _H to R _L resistance tolerance		-20	±2	+20	%
	End-to-End Temperature Coefficient	W option		175		ppm/°C
		U option		85		ppm/°C
		T option		70		ppm/°C
V _{RH} , V _R	DCP terminal voltage	V _{RH} or V _R to GND	0		V _{CC}	V
R _W	Wiper resistance	R _H - floating, V _R = 0V, force I _W current to the wiper, I _W = (V _{CC} - V _R)/R _{TOTAL} , V _{CC} = 2.7V to 5.5V		70	200	Ω
		V _{CC} = 1.7V		580		Ω
C _H /C _L /C _W	Terminal capacitance	See “DCP Macro Model” on page 8		22/22/32		pF
I _{LkgDCP}	Leakage on DCP pins	Voltage at pin from GND to V _{CC}	-0.4	< 0.1	0.4	μA
Noise	Resistor noise density	Wiper at middle point, W option		120		nV/√Hz
		Wiper at middle point, U option		190		nV/√Hz
		Wiper at middle point, T option		220		nV/√Hz
Feed Thru	Digital feed-through from bus to wiper	Wiper at middle point		-65		dB
PSRR	Power Supply Reject Ratio	Wiper output change if V _{CC} change ±10%; wiper at middle point		-75		dB

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SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
VOLTAGE DIVIDER MODE (0V @ RL; V _{CC} @ RH; measured at RW, unloaded)						
INL (Note 13)	Integral non-linearity, guaranteed monotonic	W option	-1.0	±0.5	+1.0	LSB (Note 9)
		U, T option	-0.5	±0.15	+0.5	LSB (Note 9)
DNL (Note 12)	Differential non-linearity, guaranteed monotonic	W option	-1	±0.4	+1	LSB (Note 9)
		U, T option	-0.4	±0.1	+0.4	LSB (Note 9)
FSerror (Note 11)	Full-scale error	W option	-3.5	-2	0	LSB (Note 9)
		U, T option	-2	-0.5	0	LSB (Note 9)
ZSerror (Note 10)	Zero-scale error	W option	0	2	3.5	LSB (Note 9)
		U, T option	0	0.4	2	LSB (Note 9)
TC _y (Notes 14)	Ratiometric temperature coefficient	W option, Wiper Register set to 80 hex		8		ppm/°C
		U option, Wiper Register set to 80 hex		4		ppm/°C
		T option, Wiper Register set to 80 hex		2.3		ppm/°C
	Large Signal Wiper Settling Time	From code 0 to FF hex		300		ns
f _{cutoff}	-3dB cutoff frequency	Wiper at middle point W option		1200		kHz
		Wiper at middle point U option		250		kHz
		Wiper at middle point T option		120		kHz
RHEOSTAT MODE (Measurements between RW and RL pins with RH not connected, or between RW and RH with RL not connected)						
R _{INL} (Note 18)	Integral non-linearity, Guaranteed monotonic	W option; V _{CC} = 2.7V to 5.5V	-2.0	±1	+2.0	MI (Note 15)
		W option; V _{CC} = 1.7V		10.5		MI (Note 15)
		U, T option; V _{CC} = 2.7V to 5.5V	-1.0	±0.3	+1.0	MI (Note 15)
		U, T option; V _{CC} = 1.7V		2.1		MI (Note 15)
R _{DNL} (Note 17)	Differential non-linearity, Guaranteed monotonic	W option; V _{CC} = 2.7V to 5.5V	-1	±0.4	+1	MI (Note 15)
		W option; V _{CC} = 1.7V		±0.6		MI (Note 15)
		U, T option; V _{CC} = 2.7V to 5.5V	-0.5	±0.15	+0.5	MI (Note 15)
		U, T option; V _{CC} = 1.7V		±0.35		MI (Note 15)

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Analog Specifications

$V_{CC} = 2.7V$ to $5.5V$, $V_{LOGIC} = 1.2V$ to $5.5V$ over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, $-40^{\circ}C$ to $+125^{\circ}C$.** (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
R_{offset} (Note 16)	Offset, wiper at 0 position	W option; $V_{CC} = 2.7V$ to $5.5V$	0	3	5.5	MI (Note 15)
		W option; $V_{CC} = 1.7V$		6.3		MI (Note 15)
		U, T option; $V_{CC} = 2.7V$ to $5.5V$	0	0.5	2	MI (Note 15)
		U, T option; $V_{CC} = 1.7V$		1.1		MI (Note 15)
TCR (Note 19)	Resistance temperature coefficient	W option; Wiper register set between 32 hex and FF hex		220		ppm/ $^{\circ}C$
		U option; Wiper register set between 32 hex and FF hex		100		ppm/ $^{\circ}C$
		T option; Wiper register set between 32 hex and FF hex		75		ppm/ $^{\circ}C$

Operating Specifications

$V_{CC} = 2.7V$ to $5.5V$, $V_{LOGIC} = 1.2V$ to $5.5V$ over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, $-40^{\circ}C$ to $+125^{\circ}C$.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
I_{LOGIC}	V_{LOGIC} supply current (write/read)	$V_{LOGIC} = 5.5V$, $V_{CC} = 5.5V$, $f_{SCL} = 400$ kHz (for I ² C active read and write)			200	μA
		$V_{LOGIC} = 1.2V$, $V_{CC} = 1.7V$, $f_{SCL} = 400$ kHz (for I ² C active read and write)			5	μA
I_{CC}	V_{CC} supply current (write/read)	$V_{LOGIC} = 5.5V$, $V_{CC} = 5.5V$			18	μA
		$V_{LOGIC} = 1.2V$, $V_{CC} = 1.7V$			10	μA
$I_{LOGIC\ SB}$	V_{LOGIC} standby current	$V_{LOGIC} = V_{CC} = 5.5V$, I ² C interface in standby			1	μA
		$V_{LOGIC} = 1.2V$, $V_{CC} = 1.7V$, I ² C interface in standby			0.5	μA
$I_{CC\ SB}$	V_{CC} standby current	$V_{LOGIC} = V_{CC} = 5.5V$, I ² C interface in standby			1.5	μA
		$V_{LOGIC} = 1.2V$, $V_{CC} = 1.7V$, I ² C interface in standby			1	μA
$I_{LOGIC\ SHDN}$	V_{LOGIC} shutdown current	$V_{LOGIC} = V_{CC} = 5.5V$, I ² C interface in standby			1.3	μA
		$V_{LOGIC} = 1.2V$, $V_{CC} = 1.7V$, I ² C interface in standby			0.4	μA
$I_{CC\ SHDN}$	V_{CC} shutdown current	$V_{LOGIC} = V_{CC} = 5.5V$, I ² C interface in standby			0.7	μA
		$V_{LOGIC} = 1.2V$, $V_{CC} = 1.7V$, I ² C interface in standby			0.5	μA
I_{LkgDig}	Leakage current, at pins A0, A1, SDA, SCL	Voltage at pin from GND to V_{LOGIC}	-0.4	<0.1	0.4	μA
t_{DCP}	Wiper response time	SCL rising edge of the acknowledge bit after data byte to wiper new position		1.5		μs

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SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
tShdnRec	DCP recall time from shutdown mode	SCL rising edge of the acknowledge bit after ACR data byte to wiper recalled position and RH connection		1.5		μs
V_{CC}, V_{LOGIC} Ramp (Note 21)	V_{CC}, V_{LOGIC} ramp rate	Ramp monotonic at any level	0.01		50	V/ms

Serial Interface Specification for SCL, SDA, A0, A1 Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
V_{IL}	Input LOW Voltage		-0.3		$0.3 \times V_{LOGIC}$	V
V_{IH}	Input HIGH Voltage		$0.7 \times V_{LOGIC}$		$V_{LOGIC} + 0.3$	V
Hysteresis	SDA and SCL Input Buffer Hysteresis	$V_{LOGIC} > 2V$	$0.05 \times V_{LOGIC}$			V
		$V_{LOGIC} < 2V$	$0.1 \times V_{LOGIC}$			
V_{OL}	SDA Output Buffer LOW Voltage	$I_{OL} = 3mA, V_{LOGIC} > 2V$	0		0.4	V
		$I_{OL} = 1.5mA, V_{LOGIC} < 2V$			$0.2 \times V_{LOGIC}$	V
C_{pin}	SDA, SCL Pin Capacitance			10		pF
f_{SCL}	SCL Frequency				400	kHz
t_{sp}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{LOGIC} , until SDA exits the 30% to 70% of V_{LOGIC} window			900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{LOGIC} during a STOP condition, to SDA crossing 70% of V_{LOGIC} during the following START condition	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{LOGIC} crossing	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{LOGIC} crossing	600			ns
$t_{SU:STA}$	START Condition Set-up Time	SCL rising edge to SDA falling edge; both crossing 70% of V_{LOGIC}	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{LOGIC} to SCL falling edge crossing 70% of V_{LOGIC}	600			ns
$t_{SU:DAT}$	Input Data Set-up Time	From SDA exiting the 30% to 70% of V_{LOGIC} window, to SCL rising edge crossing 30% of V_{LOGIC}	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0			ns

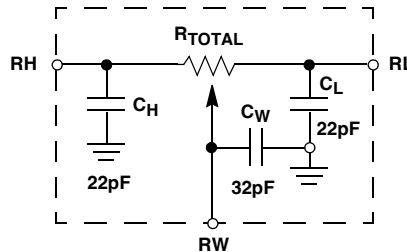
Serial Interface Specification for SCL, SDA, A0, A1 Unless Otherwise Noted. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
$t_{SU:STO}$	STOP Condition Set-up Time	From SCL rising edge crossing 70% of V_{LOGIC} , to SDA rising edge crossing 30% of V_{LOGIC}	600			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read or Write	From SDA rising edge to SCL falling edge; both crossing 70% of V_{CC} (Note 11)	1300			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{LOGIC} , until SDA enters the 30% to 70% of V_{LOGIC} window. $I_{OL} = 3mA, V_{LOGIC} > 2V$. $I_{OL} = 0.5mA, V_{LOGIC} < 2V$	0			ns
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{LOGIC}	$20 + 0.1 \times C_b$		250	ns
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{LOGIC}	$20 + 0.1 \times C_b$		250	ns
C_b	Capacitive Loading of SDA or SCL	Total on-chip and off-chip (Note 11)	10		400	pF
$t_{SU:A}$	A1, A0 setup time	Before START condition	600			ns
$t_{HD:A}$	A1, A0 hold time	After STOP condition	600			ns

NOTES:

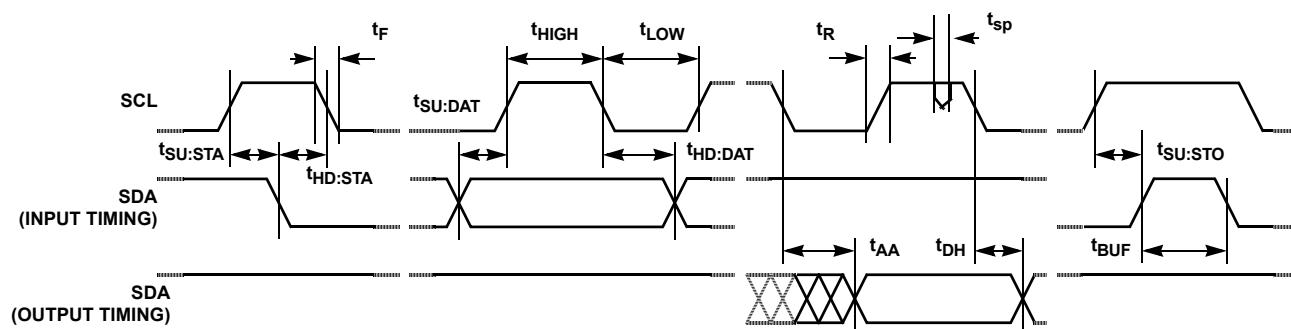
- Typical values are for $T_A = +25^\circ C$ and 3.3V supply voltages.
- $LSB = [V(RW)_{255} - V(RW)_0]/255$. $V(RW)_{255}$ and $V(RW)_0$ are $V(RW)$ for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
- ZS error = $V(RW)_0/LSB$.
- FS error = $[V(RW)_{255} - V_{CC}]/LSB$.
- $DNL = [V(RW)_i - V(RW)_{i-1}]/LSB - 1$, for $i = 1$ to 255. i is the DCP register setting.
- $INL = [V(RW)_i - i \cdot LSB - V(RW)_0]/LSB$ for $i = 1$ to 255
- $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{V(RW)_i(+25^\circ C)} \times \frac{10^6}{+165^\circ C}$ for $i = 16$ to 255 decimal, $T = -40^\circ C$ to $+125^\circ C$. $Max()$ is the maximum value of the wiper voltage and $Min()$ is the minimum value of the wiper voltage over the temperature range.
- $MI = [RW_{255} - RW_0]/255$. MI is a minimum increment. RW_{255} and RW_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively.
- $R_{offset} = RW_0/MI$, when measuring between RW and RL .
 $R_{offset} = RW_{255}/MI$, when measuring between RW and RH .
- $RDNL = (RW_i - RW_{i-1})/MI - 1$, for $i = 16$ to 255.
- $RINL = [RW_i - (MI \cdot i) - RW_0]/MI$, for $i = 16$ to 255.
- $TC_R = \frac{[Max(R_i) - Min(R_i)]}{R_i(+25^\circ C)} \times \frac{10^6}{+165^\circ C}$ for $i = 16$ to 255, $T = -40^\circ C$ to $+125^\circ C$. $Max()$ is the maximum value of the resistance and $Min()$ is the minimum value of the resistance over the temperature range.
- Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
- It is preferable to ramp up both the V_{LOGIC} and the V_{CC} supplies at the same time. If this is not possible it is recommended to ramp-up the V_{LOGIC} first followed by the V_{CC} .

DCP Macro Model

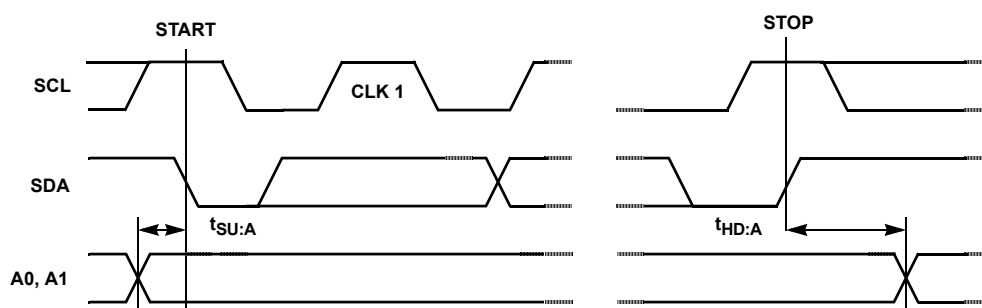


Timing Diagrams

SDA vs SCL Timing



A0 and A1 Pin Timing



Typical Performance Curves

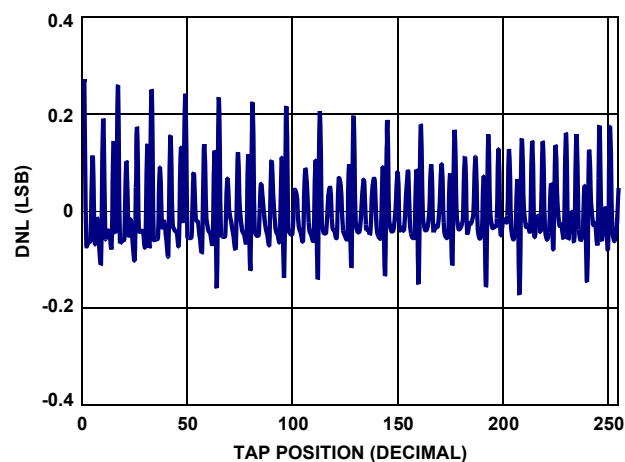


FIGURE 3. 10k DNL vs TAP POSITION, $V_{CC} = 5V$

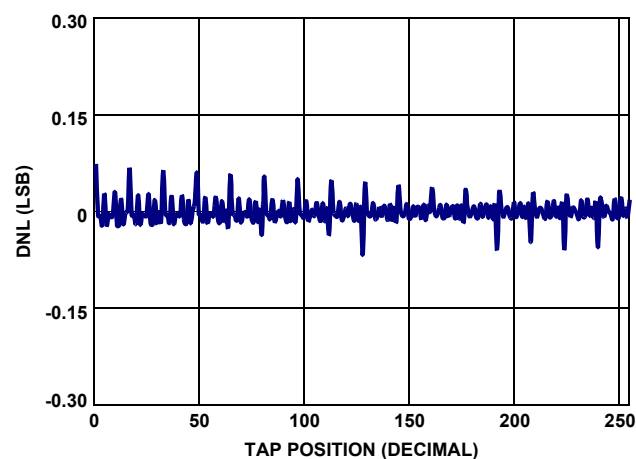


FIGURE 4. 50k DNL vs TAP POSITION, $V_{CC} = 5V$

Typical Performance Curves (Continued)

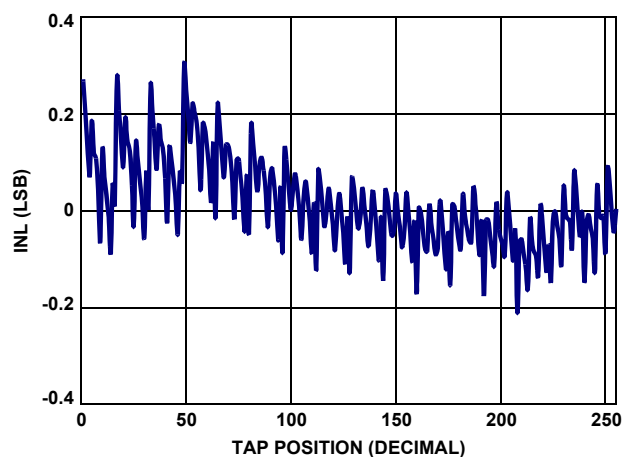


FIGURE 5. 10k INL vs TAP POSITION, $V_{CC} = 5V$

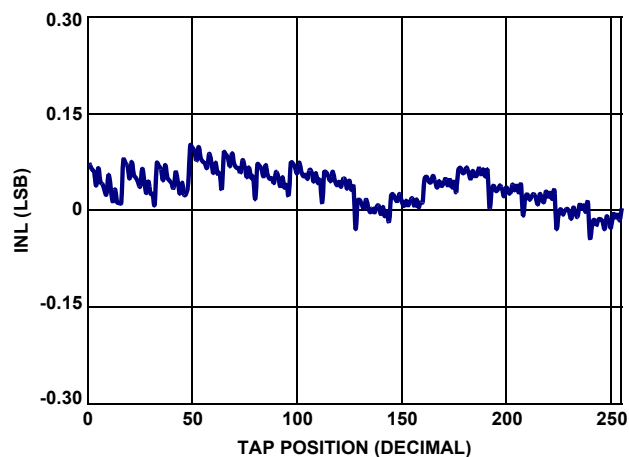


FIGURE 6. 50k INL vs TAP POSITION, $V_{CC} = 5V$

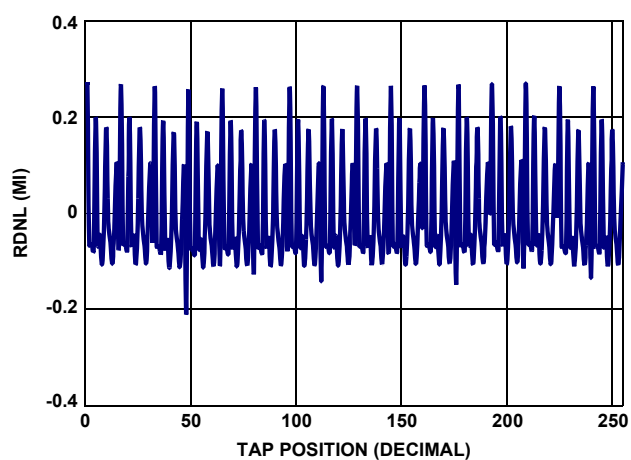


FIGURE 7. 10k RDNL vs TAP POSITION, $V_{CC} = 5V$

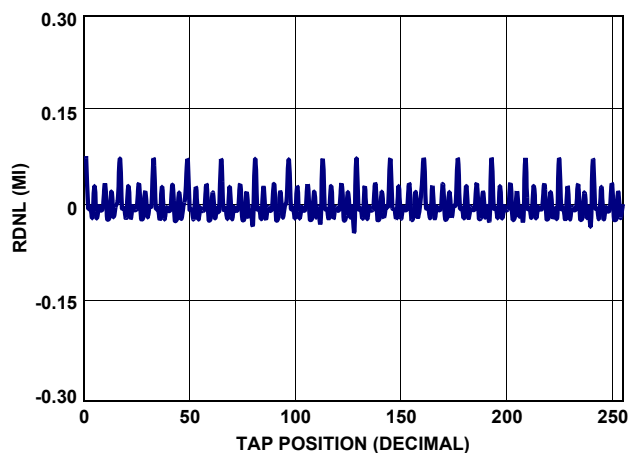


FIGURE 8. 50k RDNL vs TAP POSITION, $V_{CC} = 5V$

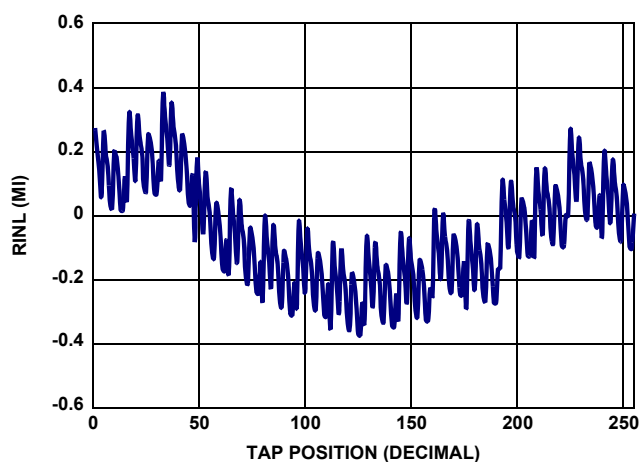


FIGURE 9. 10k RINL vs TAP POSITION, $V_{CC} = 5V$

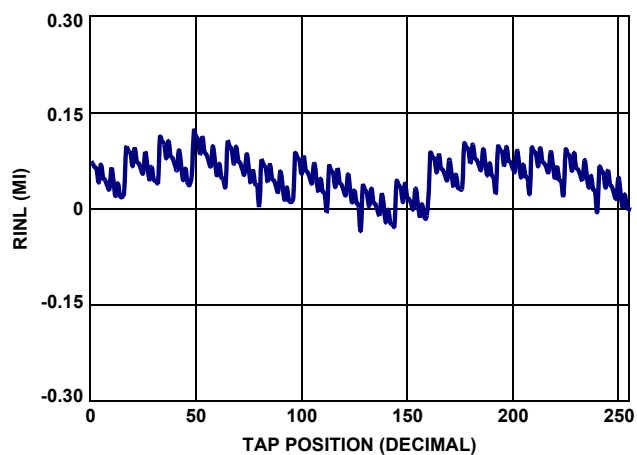


FIGURE 10. 50k RINL vs TAP POSITION, $V_{CC} = 5V$

Typical Performance Curves (Continued)

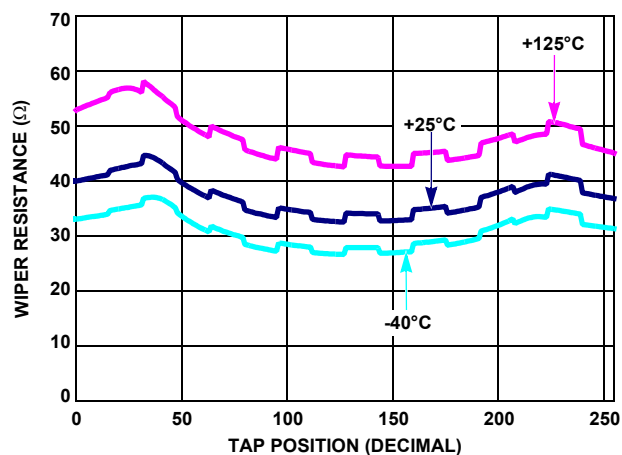


FIGURE 11. 10k WIPER RESISTANCE vs TAP POSITION, $V_{CC} = 5V$

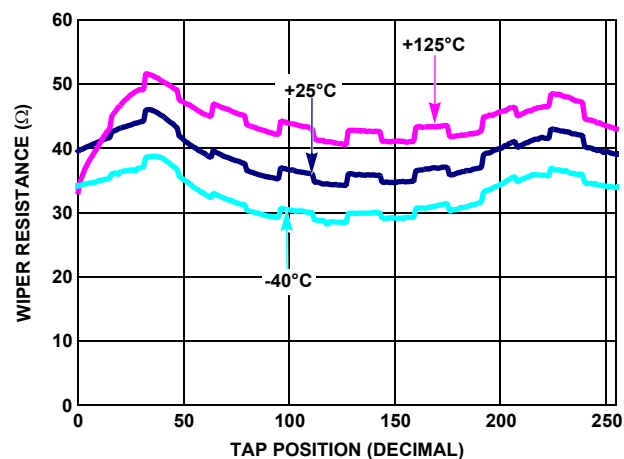


FIGURE 12. 50k WIPER RESISTANCE vs TAP POSITION, $V_{CC} = 5V$

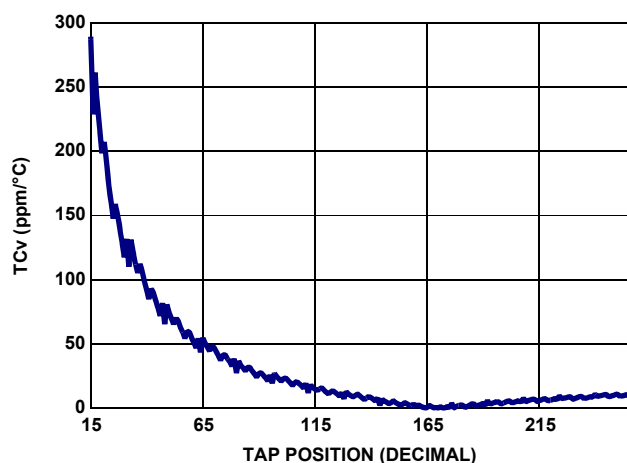


FIGURE 13. 10k TCv vs TAP POSITION

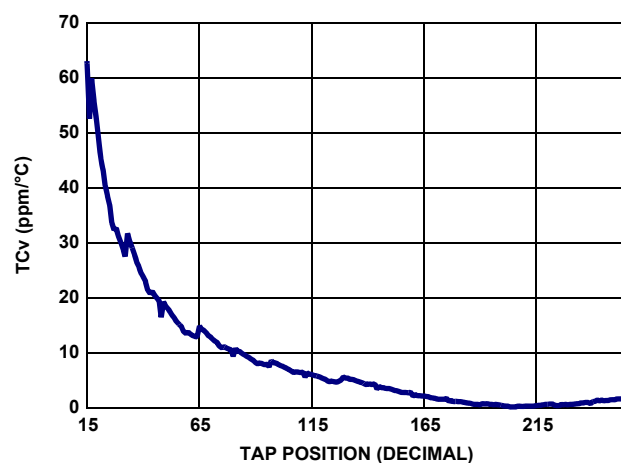


FIGURE 14. 50k TCv vs TAP POSITION

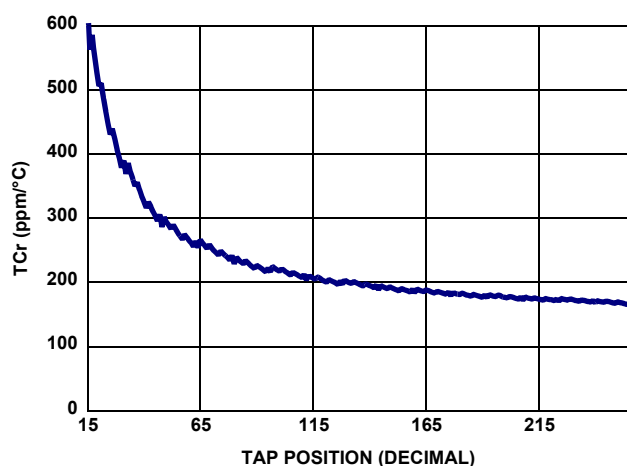


FIGURE 15. 10k TCr vs TAP POSITION

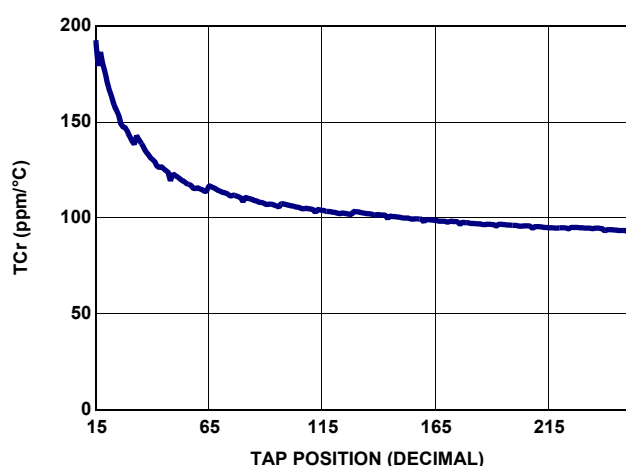


FIGURE 16. 50k TCr vs TAP POSITION

Typical Performance Curves (Continued)

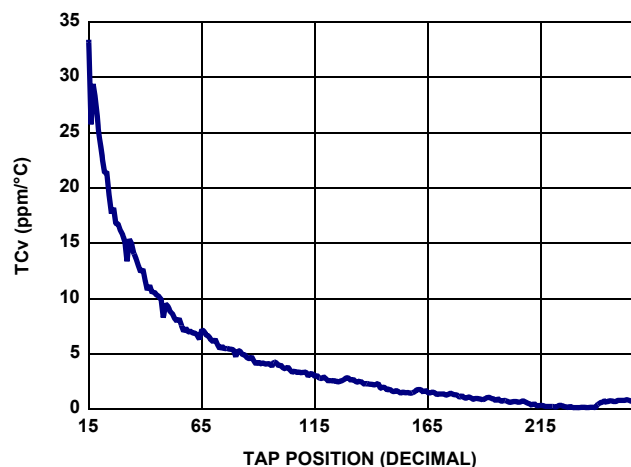


FIGURE 17. 100k TCv vs TAP POSITION

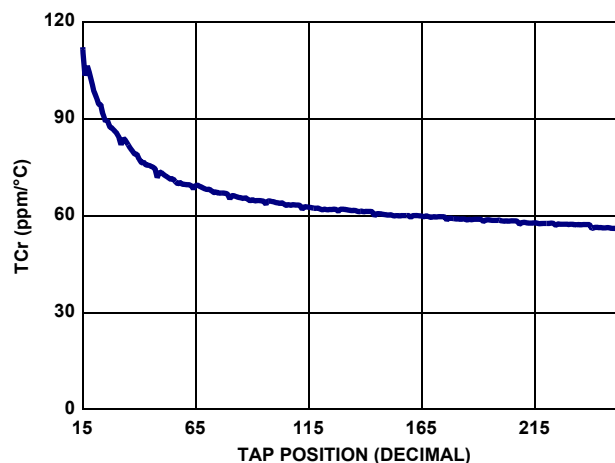


FIGURE 18. 100k TCr vs TAP POSITION

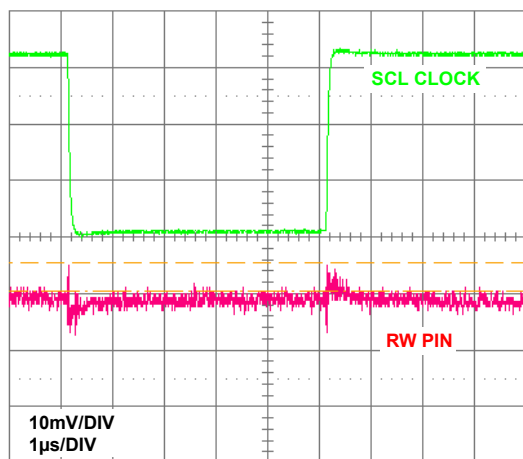


FIGURE 19. WIPER DIGITAL FEED-THROUGH

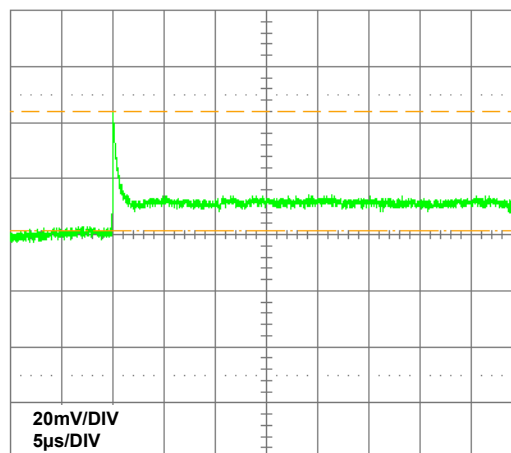


FIGURE 20. WIPER TRANSITION GLITCH

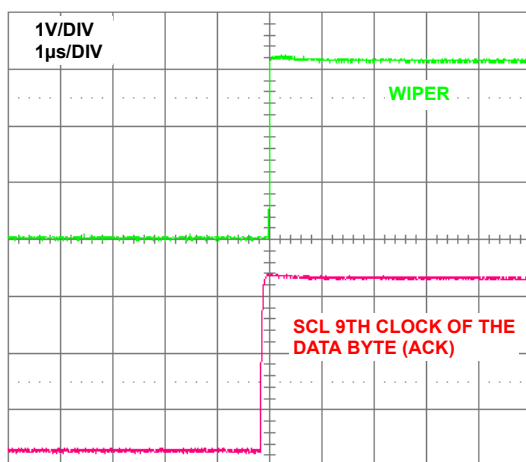


FIGURE 21. WIPER LARGE SIGNAL SETTLING TIME

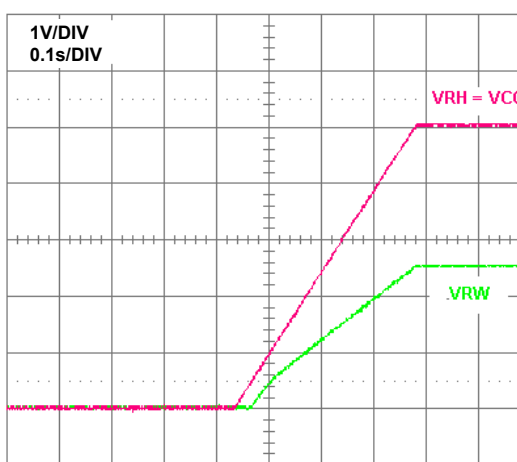


FIGURE 22. POWER-ON START-UP IN VOLTAGE DIVIDER MODE

Typical Performance Curves (Continued)

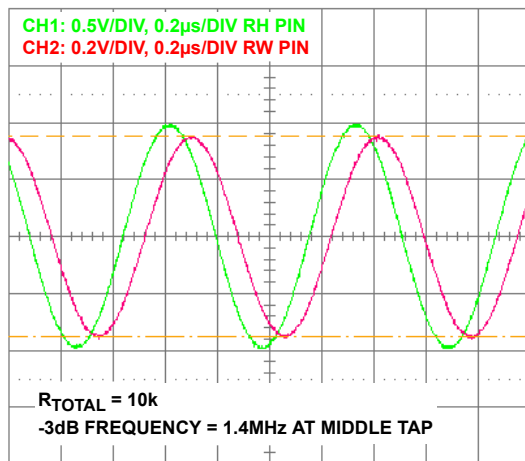


FIGURE 23. 10k -3dB CUT OFF FREQUENCY

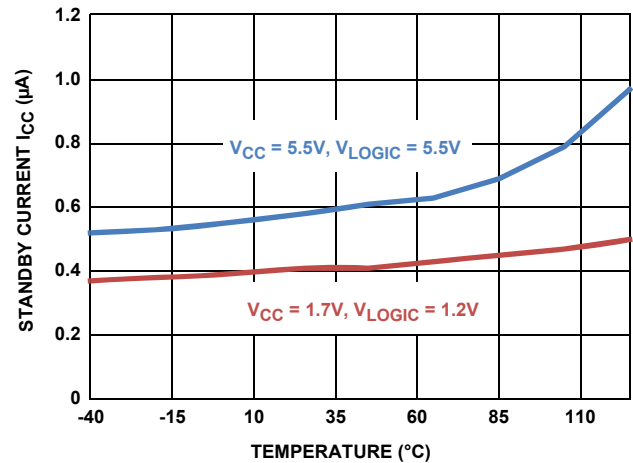


FIGURE 24. STANDBY CURRENT vs TEMPERATURE

Functional Pin Descriptions

Potentiometers Pins

RH AND RL

The high (R_H) and low (R_L) terminals of the ISL23315 are equivalent to the fixed terminals of a mechanical potentiometer. R_H and R_L are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WR set to 255 decimal, the wiper will be closest to R_H , and with the WR set to 0, the wiper is closest to R_L .

RW

RW is the wiper terminal, and it is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR register.

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for I²C interface. It receives device address, operation code, wiper address and data from an I²C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

SERIAL CLOCK (SCL)

This input is the serial clock of the I²C serial interface. SCL requires an external pull-up resistor, since a master is an open drain output.

DEVICE ADDRESS (A1, A0)

The address inputs are used to set the least significant 2 bits of the 7-bit I²C interface slave address. A match in the slave address serial data stream must match with the Address input pins in order to initiate communication with the ISL23315. A maximum of four ISL23315 devices may occupy the I²C serial bus (see Table 3).

V_{LOGIC}

This is an input pin, that supply internal level translator for serial bus operation from 1.2V to 5.5V.

Principles of Operation

The ISL23315 is an integrated circuit incorporating one DCP with its associated registers and an I²C serial interface providing direct communication between a host and the potentiometer. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

Voltage at any DCP pins, R_H , R_L or R_W , should not exceed V_{CC} level at any conditions during power-up and normal operation.

The V_{LOGIC} pin needs to be connected to the I²C bus supply which allows reliable communication with the wide range of microcontrollers and independent of the V_{CC} level. This is extremely important in systems where the master supply has lower levels than DCP analog supply.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L pins). The RW pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). When the WR of a DCP contains all zeroes (WR[7:0] = 00h), its wiper terminal (RW) is closest to its “Low” terminal (R_L). When the WR register of a DCP contains all ones (WR[7:0] = FFh), its wiper terminal (RW) is closest to its “High” terminal (R_H). As the value of the WR increases from all zeroes (0) to all ones (255 decimal), the wiper moves monotonically from the position closest to R_L to the position closest to R_H . At the same time, the

resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the ISL23315 is being powered up, the WR is reset to 80h (128 decimal), which locates RW roughly at the center between R_L and R_H .

The WR can be read or written to directly using the I²C serial interface as described in the following sections.

Memory Description

The ISL23315 contains two volatile 8-bit registers: Wiper Register (WR) and Access Control Register (ACR). Memory map of ISL23315 is in Table 1. The Wiper Register (WR) at address 0, contains current wiper position. The Access Control Register (ACR) at address 10h contains information and control bits described in Table 2.

TABLE 1. MEMORY MAP

ADDRESS (hex)	VOLATILE REGISTER NAME	DEFAULT SETTING (hex)
10	ACR	42
0	WR	80

TABLE 2. ACCESS CONTROL REGISTER (ACR)

BIT #	7	6	5	4	3	2	1	0
NAME/VALUE	0	SHDN	0	0	0	0	1	0

The SHDN bit (ACR[6]) disables or enables Shutdown mode. When this bit is 0, i.e. DCP is forced to end-to-end open circuit and RW is shorted to RL as shown in Figure 25. Default value of the SHDN bit is 1.

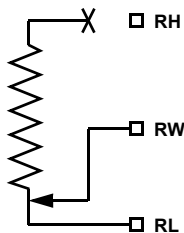


FIGURE 25. DCP CONNECTION IN SHUTDOWN MODE

I²C Serial Interface

The ISL23315 supports an I²C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL23315 operates as a slave device in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for

indicating START and STOP conditions (see Figure 26). On power-up of the ISL23315, the SDA pin is in the input mode.

All I²C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH. The ISL23315 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 26). A START condition is ignored during the power-up of the device.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 26). A STOP condition at the end of a read operation or at the end of a write operation places the device in its standby mode.

An ACK (Acknowledge) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 27).

The ISL23315 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL23315 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 10100 as the five MSBs, and the following two bits matching the logic values present at pins A1 and A0. The LSB is the Read/Write bit. Its value is "1" for a Read operation and "0" for a Write operation (see Table 3).

TABLE 3. IDENTIFICATION BYTE FORMAT
LOGIC VALUES AT PINS A1 AND A0, RESPECTIVELY

1	0	1	0	0	A1	A0	R/W
(MSB)					(LSB)		

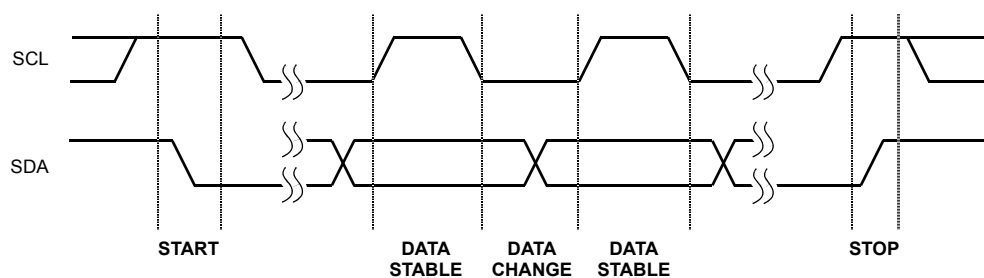


FIGURE 26. VALID DATA CHANGES, START AND STOP CONDITIONS

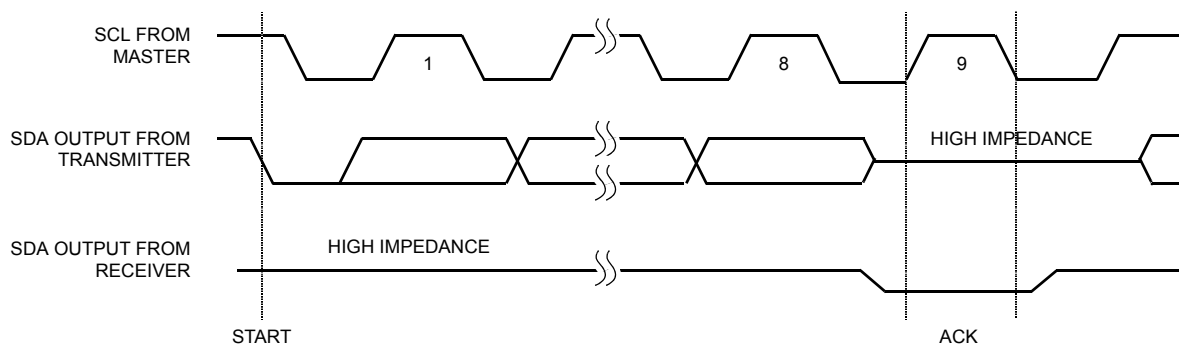


FIGURE 27. ACKNOWLEDGE RESPONSE FROM RECEIVER

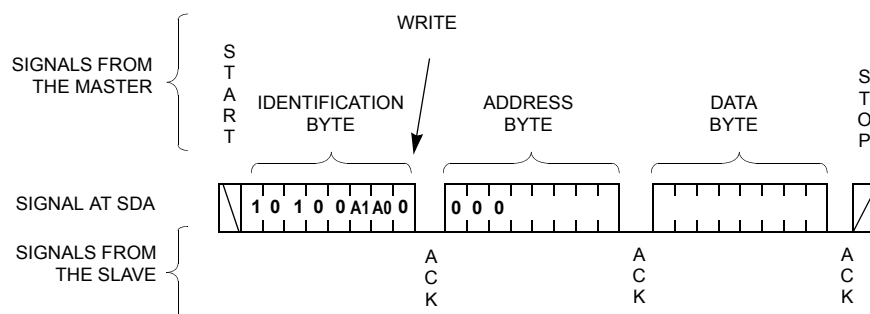


FIGURE 28. BYTE WRITE SEQUENCE

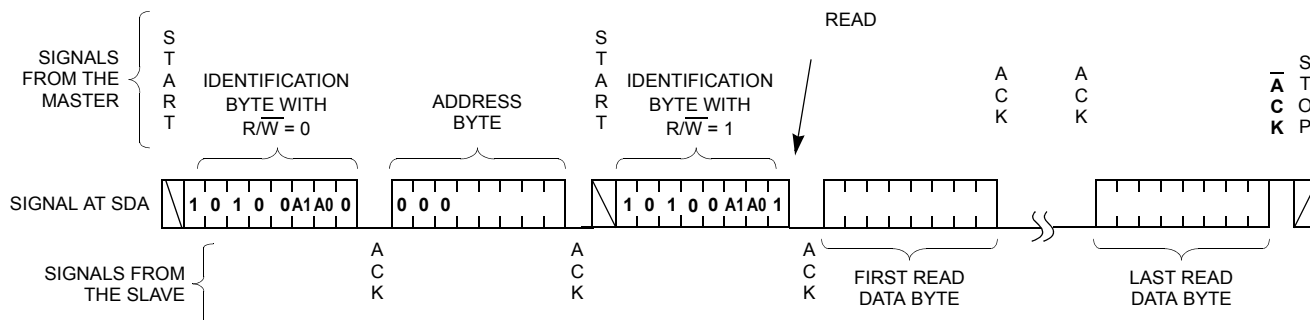


FIGURE 29. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL23315 responds with an ACK. The data is transferred from I²C block to the corresponding register at the 9th clock of the data byte and device enters its standby state (see Figures 27 and 28).

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 29). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/W bit set to "0", an Address Byte, a second START, and a second Identification byte with the R/W bit set to "1". After each of the three bytes, the ISL23315 responds with an ACK; then the ISL23315 transmits Data Byte. The master terminates the read operation issuing a NACK ($\overline{\text{ACK}}$) and a STOP condition following the last bit of the last Data Byte (see Figure 29).

Applications Information

V_{LOGIC} Requirements

It is recommended to keep V_{LOGIC} powered all the time during normal operation. In a case where turning V_{LOGIC} OFF is necessary, it is recommended to ground the V_{LOGIC} pin of the ISL23315. Grounding the V_{LOGIC} pin or both V_{LOGIC} and V_{CC} does not affect other devices on the same bus. It is good practice to put a 1μF cap in parallel to 0.1μF as close to the V_{LOGIC} pin as possible.

V_{CC} Requirements and Placement

It is recommended to put a 1μF capacitor in parallel with 0.1μF decoupling capacitor close to the V_{CC} pin.

Wiper Transition

When stepping up through each tap in voltage divider mode, some tap transition points can result in noticeable voltage transients, or overshoot/undershoot, resulting from the sudden transition from a very low impedance "make" to a much higher impedance "break" within a short period of time (<1μs). There are several code transitions such as 0Fh to 10h, 1Fh to 20h, ..., EFh to FFh, which have higher transient glitch. Note, that all switching transients will settle well within the settling time as stated in the datasheet. A small capacitor can be added externally to reduce the amplitude of these voltage transients. However, that will also reduce the useful bandwidth of the circuit, thus may not be a good solution for some applications. It may be a good idea, in that case, to use fast amplifiers in a signal chain for fast recovery.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
12/15/10	FN7778.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL23315](http://www.intersil.com/ISL23315)

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at <http://rel.intersil.com/reports/search.php>

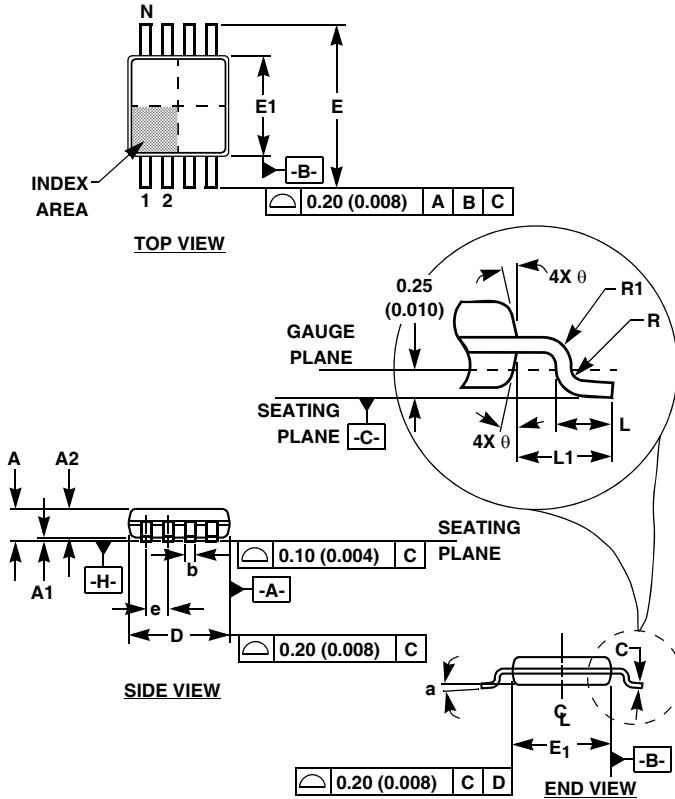
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Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)
10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5°	15°	5°	15°	-
α	0°	6°	0°	6°	-

Rev. 0 12/02

NOTES:

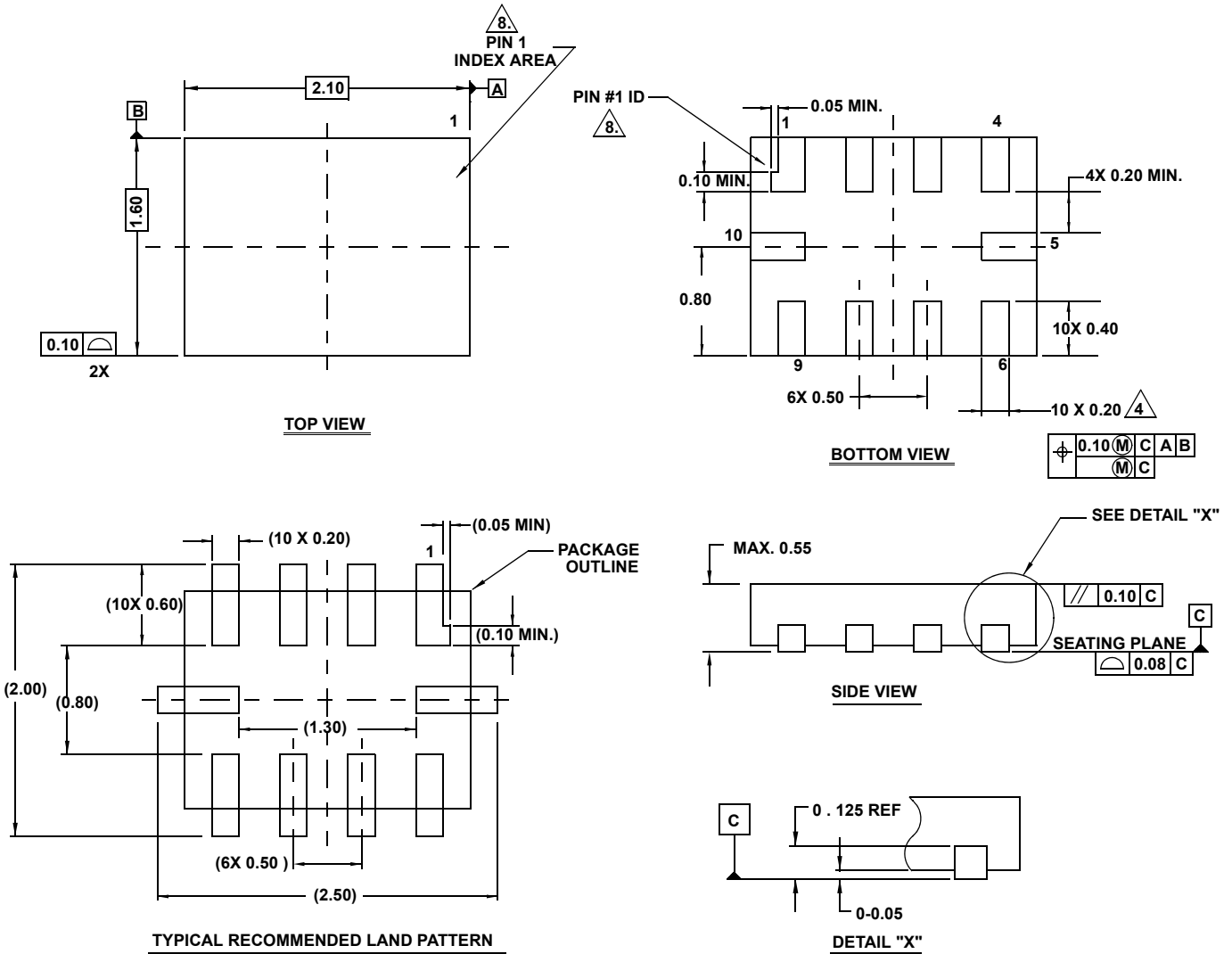
- These package dimensions are within allowable dimensions of JEDEC MO-187BA.
- Dimensioning and tolerancing per ANSI Y14.5M-1994.
- Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. $\boxed{-H-}$ Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
- Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
- "L" is the length of terminal for soldering to a substrate.
- "N" is the number of terminal positions.
- Terminal numbers are shown for reference only.
- Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
- Datums $\boxed{-A-}$ and $\boxed{-B-}$ to be determined at Datum plane $\boxed{-H-}$.
- Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

Package Outline Drawing

L10.2.1x1.6A

10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 5, 3/10



NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All Dimensions are in millimeters. Angles are in degrees. Dimensions in () for Reference Only.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Maximum package warpage is 0.05mm.
6. Maximum allowable burrs is 0.076mm in all directions.
7. Same as JEDEC MO-255UABD except:
No lead-pull-back, MIN. Package thickness = 0.45 not 0.50mm
Lead Length dim. = 0.45mm max. not 0.42mm.
8. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.