30V, N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD17301Q5A

FEATURES

- **Optimized for 5V Gate Drive**
- **Ultralow Q_g and Q_{gd}**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 5-mm × 6-mm Plastic Package**

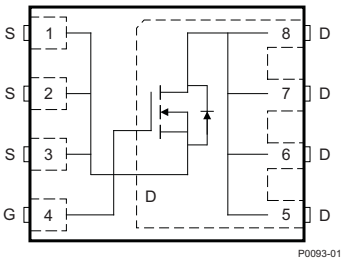
APPLICATIONS

- **Notebook Point of Load**
- **Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems**
- **Optimized for Synchronous FET Applications**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications, and optimized for 5V gate drive applications.

Top View



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	30		V
Q_g	Gate Charge Total (4.5V)	19		nC
Q_{gd}	Gate Charge Gate to Drain	4.3		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3V	2.9	mΩ
		V_{GS} = 4.5V	2.3	mΩ
		V_{GS} = 8V	2	mΩ
$V_{GS(th)}$	Threshold Voltage	1.1		V

ORDERING INFORMATION

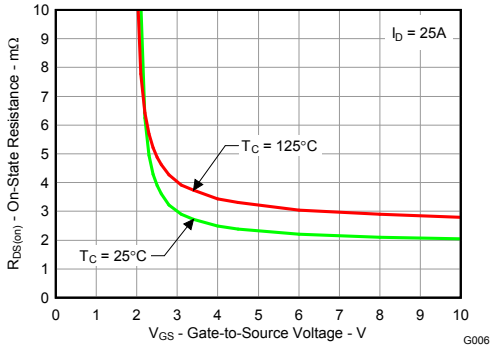
Device	Package	Media	Qty	Ship
CSD17301Q5A	SON 5-mm × 6-mm Plastic Package	13-inch reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

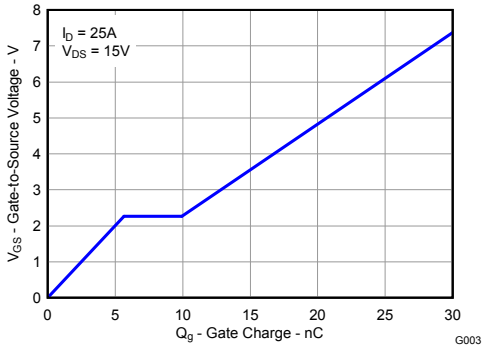
T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	+10 / –8	V
I_D	Continuous Drain Current, T_C = 25°C	100	A
	Continuous Drain Current(1)	28	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	118	A
P_D	Power Dissipation(1)	3.2	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 91A, L = 0.1mH, R_G = 25Ω	414	mJ

(1) Typical $R_{\theta JA}$ = 39°C/W on 1in² Cu (2 oz) on 0.060" thick FR4 PCB.
(2) Pulse width ≤300μs, duty cycle ≤2%

$R_{DS(on)}$ vs V_{GS}



GATE CHARGE



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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

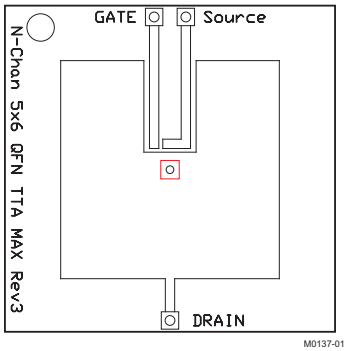
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250μA	30			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 24V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +10/-8V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	0.9	1.1	1.55	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3V, I_D = 25A		2.9	3.7	mΩ
		V_{GS} = 4.5V, I_D = 25A		2.3	3	mΩ
		V_{GS} = 8V, I_D = 25A		2	2.6	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_D = 25A		149		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		2660	3480	pF
C_{oss}	Output Capacitance			1420	1850	pF
C_{rss}	Reverse Transfer Capacitance			80	105	pF
R_G	Series Gate Resistance			1.3	2.6	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 15V, I_D = 25A		19	25	nC
Q_{gd}	Gate Charge Gate to Drain			4.3		nC
Q_{gs}	Gate Charge Gate to Source			5.7		nC
$Q_{g(th)}$	Gate Charge at Vth			2.9		nC
Q_{oss}	Output Charge	V_{DS} = 14V, V_{GS} = 0V		35		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15V, V_{GS} = 4.5V, I_D = 25A R_G = 2Ω		10.7		ns
t_r	Rise Time			16.2		ns
$t_{d(off)}$	Turn Off Delay Time			28		ns
t_f	Fall Time			10.5		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 25A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD}= 14V, I_F = 25A, di/dt = 300A/μs		50		nC
t_{rr}	Reverse Recovery Time			33		ns

THERMAL CHARACTERISTICS

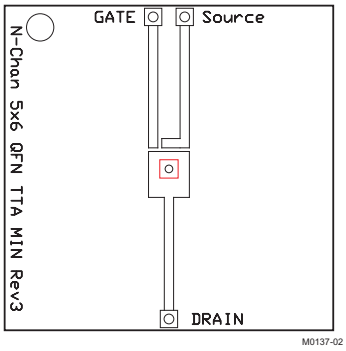
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			2.2	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			49	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 × 1.5 in 0.060 inch thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 Material with 1 $inch^2$ of 2 oz. Cu.



Max $R_{\theta JA}$ = 49°C/W when mounted on 1inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 120°C/W when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

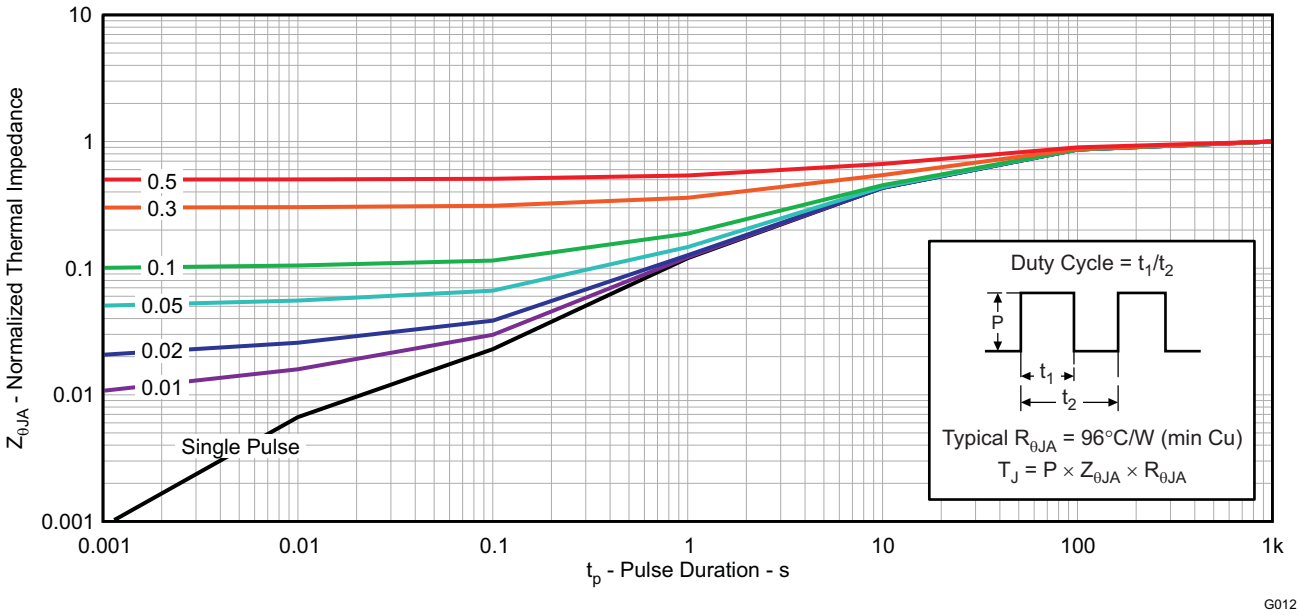


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

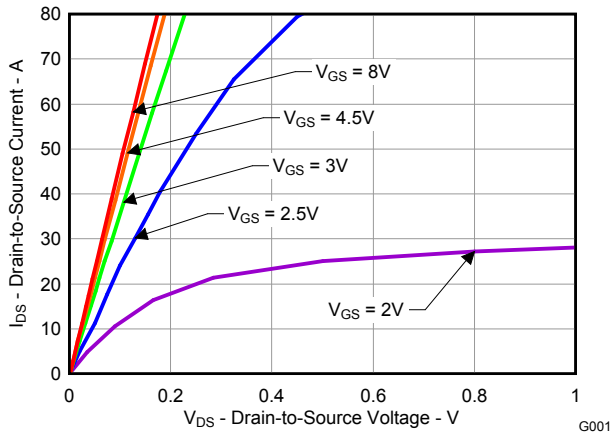


Figure 2. Saturation Characteristics

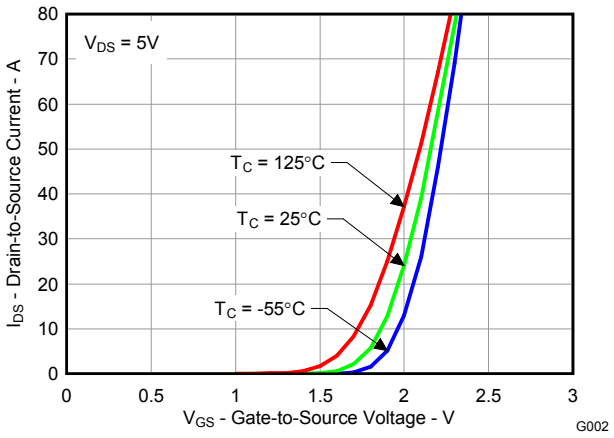


Figure 3. Transfer Characteristics

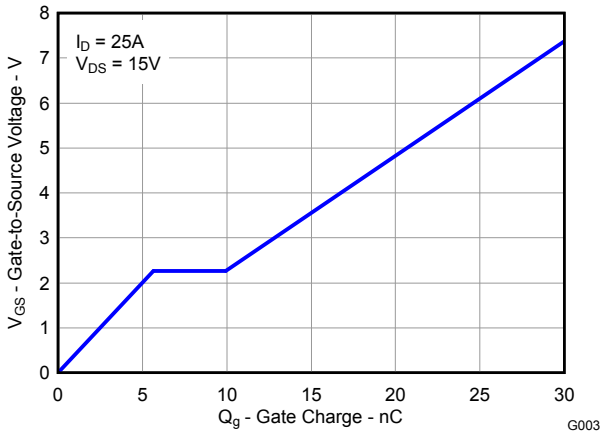


Figure 4. Gate Charge

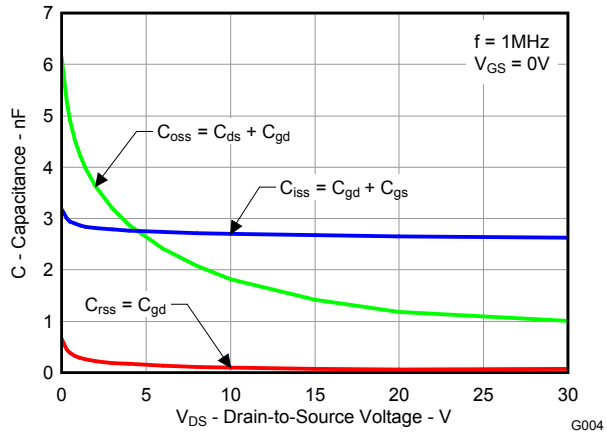


Figure 5. Capacitance

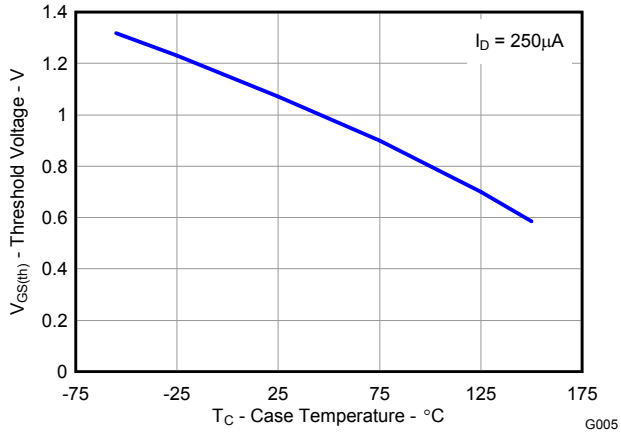


Figure 6. Threshold Voltage vs. Temperature

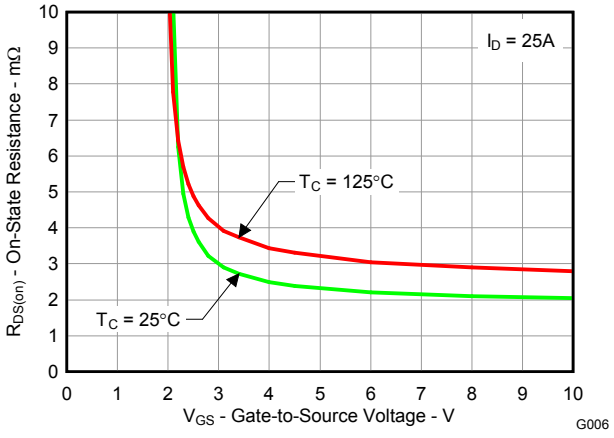


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

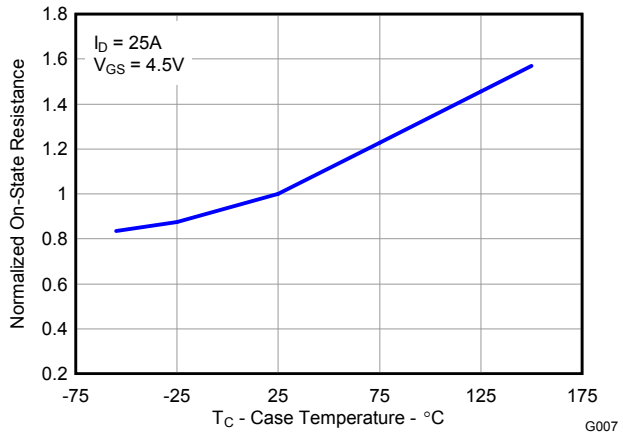


Figure 8. On Resistance vs. Temperature

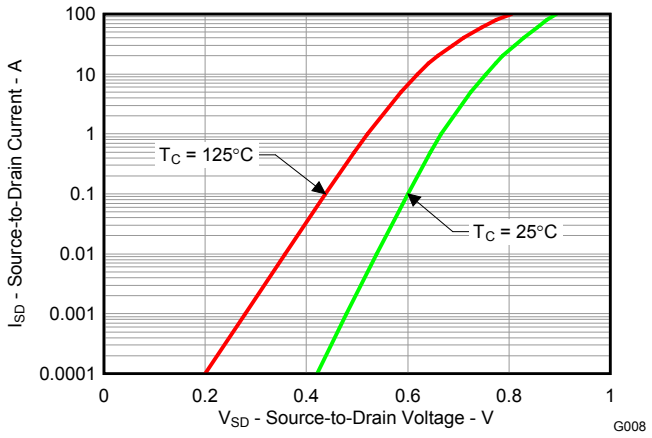


Figure 9. Typical Diode Forward Voltage

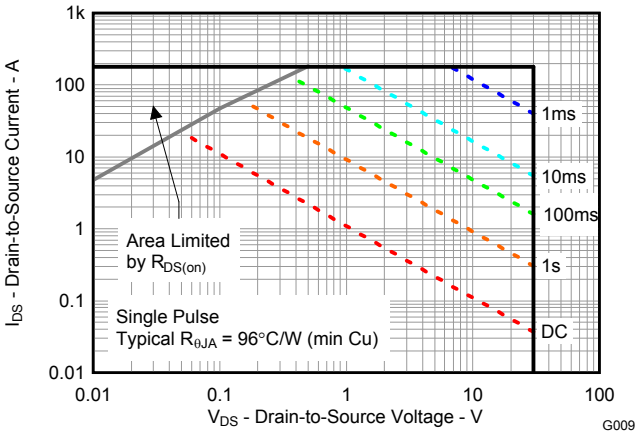


Figure 10. Maximum Safe Operating Area

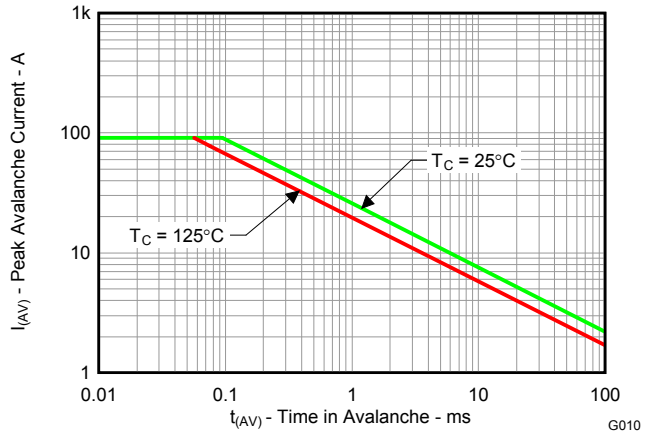


Figure 11. Single Pulse Unclamped Inductive Switching

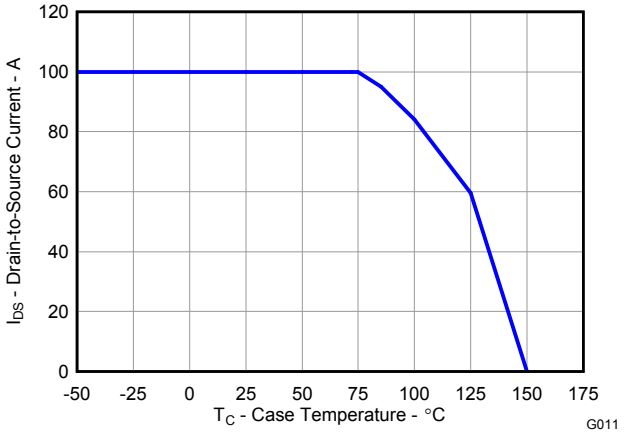
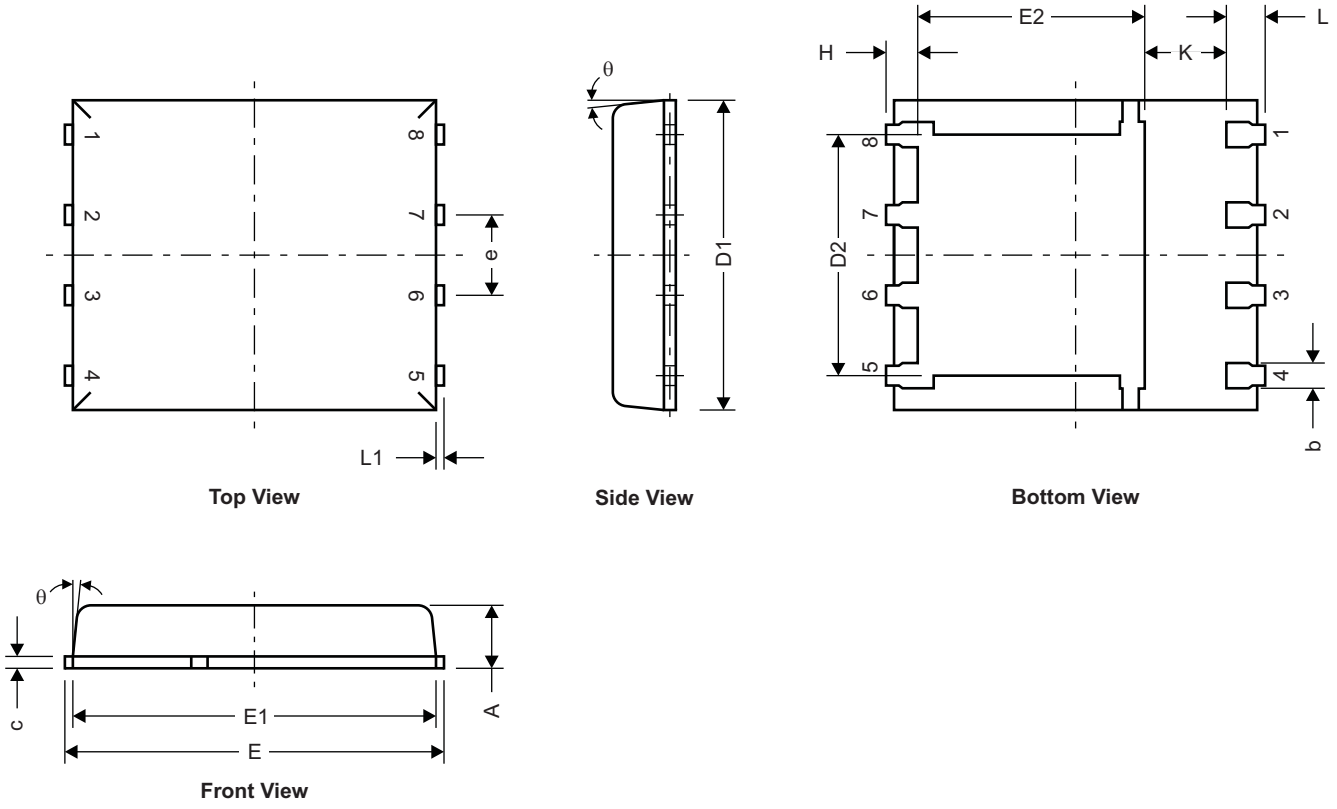


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

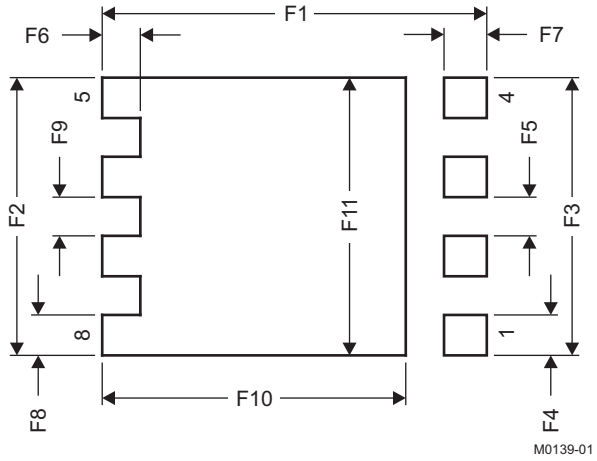
Q5A Package Dimensions



M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e		1.27 BSC	
H	0.41	0.51	0.61
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

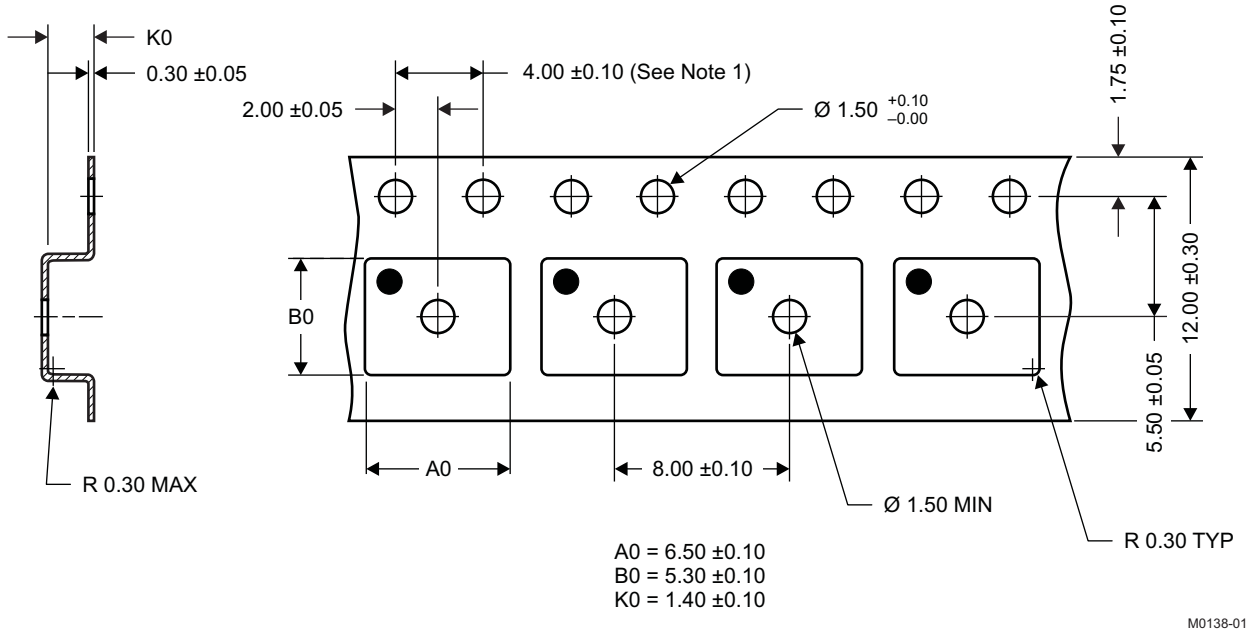
Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q5A Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
6. MSL1 260°C (IR and convection) PbF reflow compatible

Package Marking Information

Location

1st Line

CSD = Fixed Characters

NNNNN = Product Code

2nd Line (Date Code)

YY = Last 2 digits of the Year

WW = 2-digit Work Week

C = Country of Origin

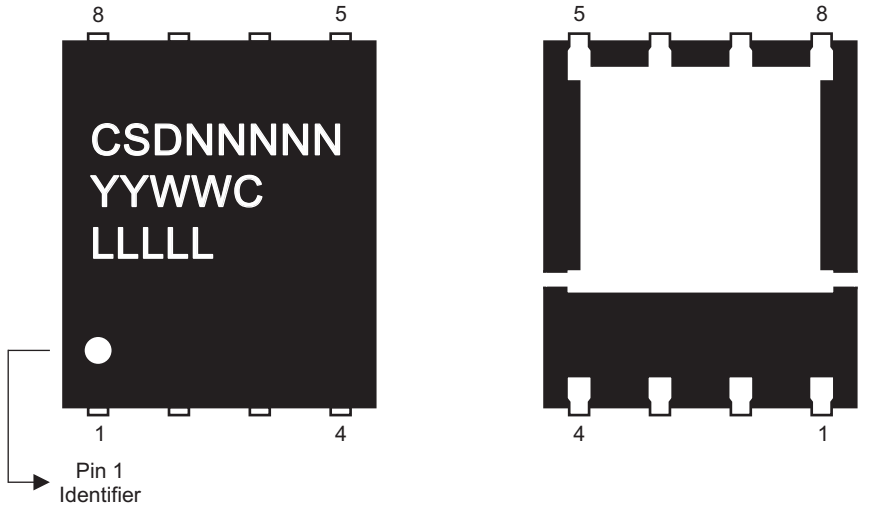
> Philippines = P

> Taiwan = T

> China = C

3rd Line

LLLLL = Last 5 digits of the Wafer Lot #



REVISION HISTORY

Changes from Original (January) to Revision A **Page**

- Changed the Abs Max Ratings table, Avalanche Energy, single pulse From: I_D = 85A, L = 0.1mH, R_G = 25Ω Value = 361 To: I_D = 91A, L = 0.1mH, R_G = 25Ω Value = 414 1
- Changed Figure 11 5

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