Dual N-Channel NexFET™ Power MOSFET

Check for Samples: CSD86311W1723

FEATURES

- **Dual N-Ch MOSFETs**
- **Common Source Configuration**
- **Small Footprint 1.7 mm × 2.3 mm**
- **Ultra Low Q_g and Q_{gd}**
- **Pb Free**
- **RoHS Compliant**
- **Halogen Free**

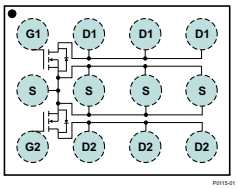
APPLICATIONS

- **Battery Management**
- **Battery Protection**
- **DC-DC Converters**

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with thermal characteristics in an ultra low profile. Low on resistance and gate charge coupled with the small footprint and low profile make the device ideal for battery operated space constrained application in load management as well as DC-DC converter applications

Top View



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5V)	3.1		nC
Q_{gd}	Gate Charge Gate to Drain	0.33		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 2.5V	37	mΩ
		V_{GS} = 4.5V	31	mΩ
		V_{GS} = 8V	29	mΩ
$V_{GS(th)}$	Threshold Voltage	1		V

ORDERING INFORMATION

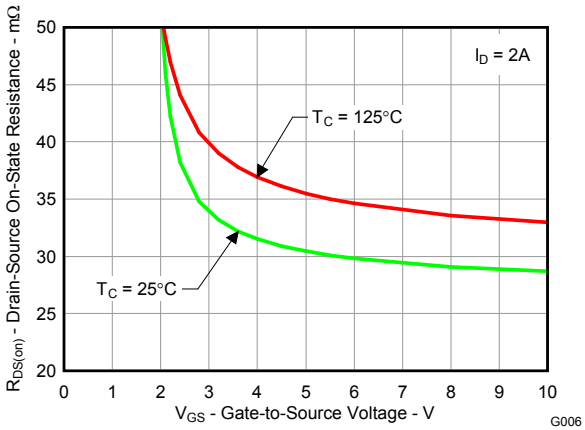
Device	Package	Media	Qty	Ship
CSD86311W1723	1.7-mm × 2.3-mm Wafer Level Package	7-inch reel	3000	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

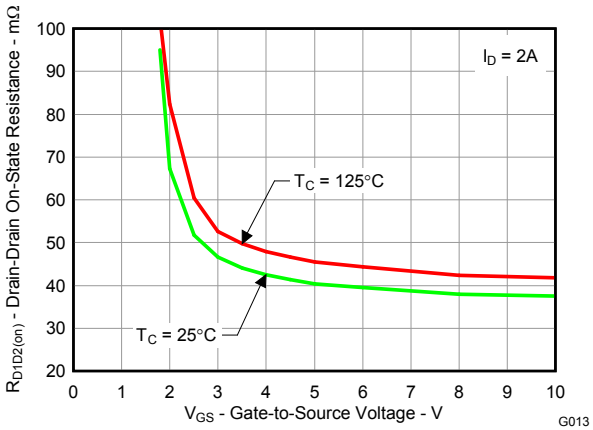
T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / -8	V
I_D	Continuous Drain Current (1) (2)(3)	4.5	A
	Pulsed Drain Current (1) (2)(3)		
I_G	Continupus Gate Clamp Current (4)	6	A
	Pulsed Gate Clamp Current (4)		
P_D	Power Dissipation (1)	1.5	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) May be limited by Max source current
(2) Based on Min Cu footprint
(3) Per MOSFET
(4) Total for device

$R_{DS(on)}$ vs V_{GS}



$R_{D1D2(on)}$ vs V_{GS}



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

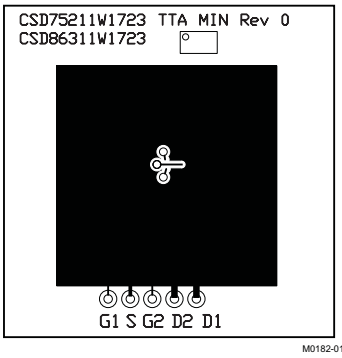
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	25			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +10 / -8V			±100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.85	1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 2.5V, I_{DS} = 2A		37	51	mΩ
		V_{GS} = 4.5V, I_{DS} = 2A		31	42	mΩ
		V_{GS} = 8V, I_{DS} = 2A		29	39	mΩ
$R_{DD(on)}$	Drain to Drain On Resistance	V_{GS} = 2.5V, I_D = 2A		52	75	mΩ
		V_{GS} = 4.5V, I_{DS} = 2A		41	55	mΩ
		V_{GS} = 8V, I_{DS} = 2A		38	50	mΩ
g_{fs}	Transconductance	V_{DS} = 10V, I_D = 2A		6.4		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz		450	585	pF
C_{OSS}	Output Capacitance			250	325	pF
C_{RSS}	Reverse Transfer Capacitance			10	13	pF
R_G	Seried Gate Resistance			1.4	2.8	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 12.5V, I_D = 2A		3.1	4	nC
Q_{gd}	Gate Charge Gate to Drain			0.33		nC
Q_{gs}	Gate Charge Gate to Source			0.85		nC
$Q_{g(th)}$	Gate Charge at Vth			0.48		nC
Q_{OSS}	Output Charge	V_{DS} = 12.2V, V_{GS} = 0V		4.5		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 2A, R_G = 2Ω		5.4		ns
t_r	Rise Time			4.3		ns
$t_{d(off)}$	Turn Off Delay Time			13.2		ns
t_f	Fall Time			2.9		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = 2A, V_{GS} = 0V		0.78	1	V
Q_{rr}	Reverse Recovery Charge	V_{dd}= 12.2V, I_F = 2A, di/dt = 300A/µs		4.2		nC
t_{rr}	Reverse Recovery Time			13.4		ns

THERMAL CHARACTERISTICS

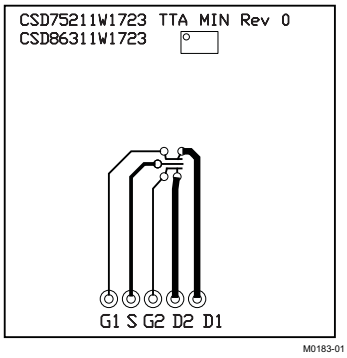
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Minimum Cu area) (1) (2)			165	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (1 in^2 Cu area) (2) (3)			68	°C/W

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Measured with both devices biased in a parallel condition.
(3) Device mounted on FR4 material with 1 in^2 of 2oz. Cu.



Max $R_{\theta JA}$ = 68°C/W when mounted on 1inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 165°C/W when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

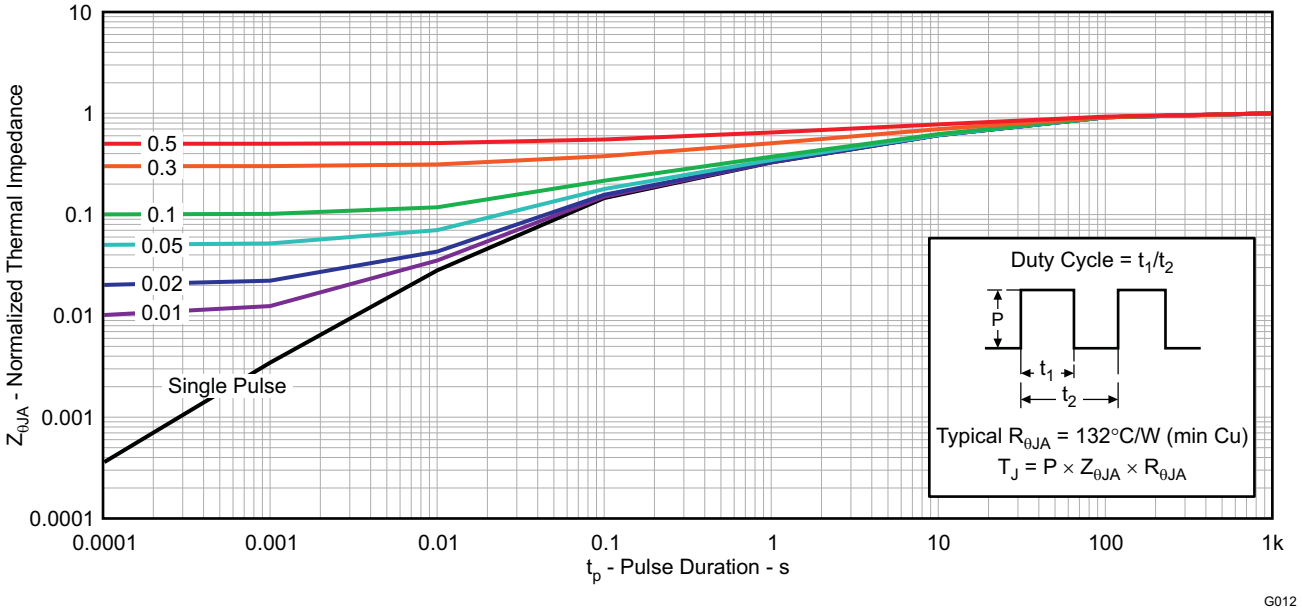


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

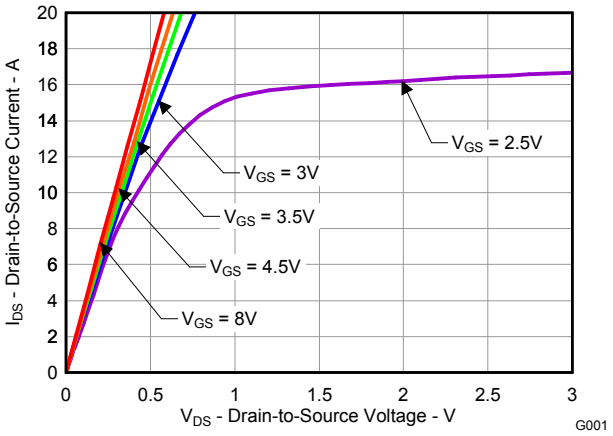


Figure 2. Saturation Characteristics

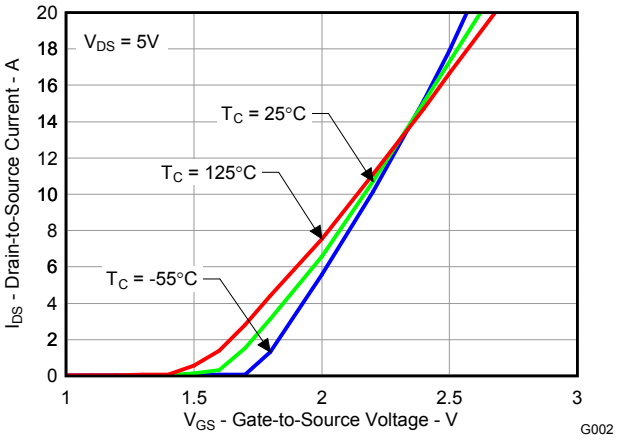


Figure 3. Transfer Characteristics

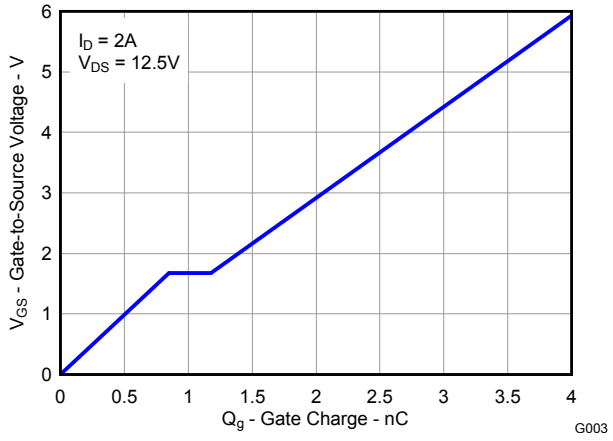


Figure 4. Gate Charge

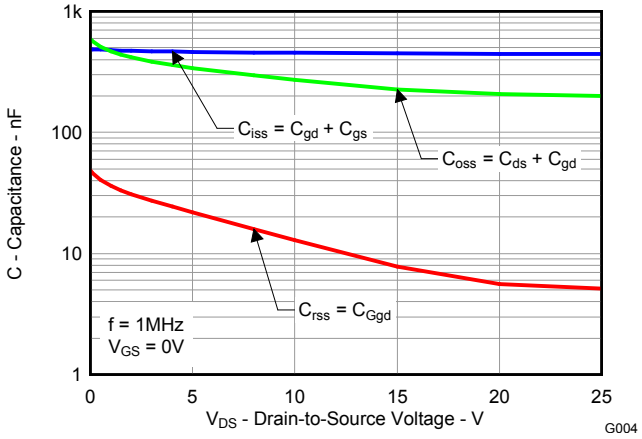


Figure 5. Capacitance

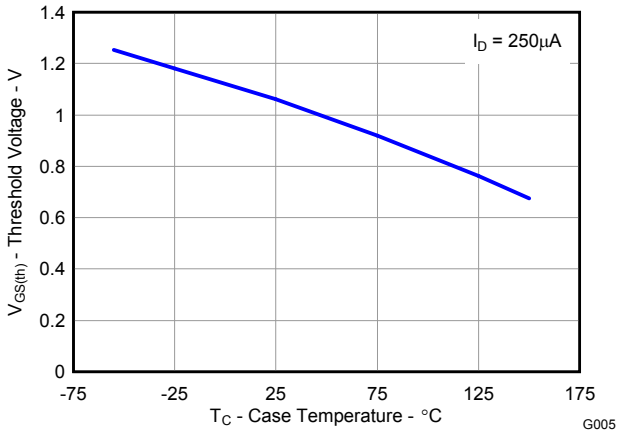


Figure 6. Threshold Voltage vs. Temperature

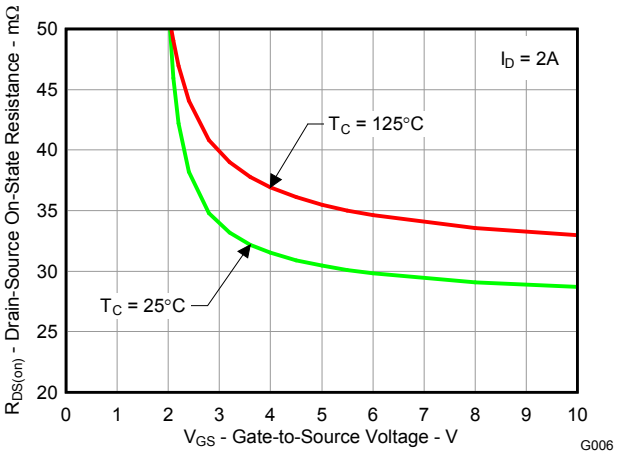


Figure 7. $R_{DS(on)}$ vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

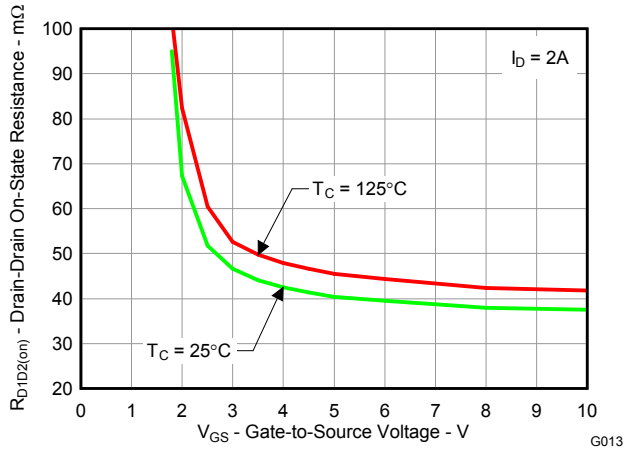


Figure 8. $R_{D1D2(on)}$ vs. Gate-to-Source Voltage

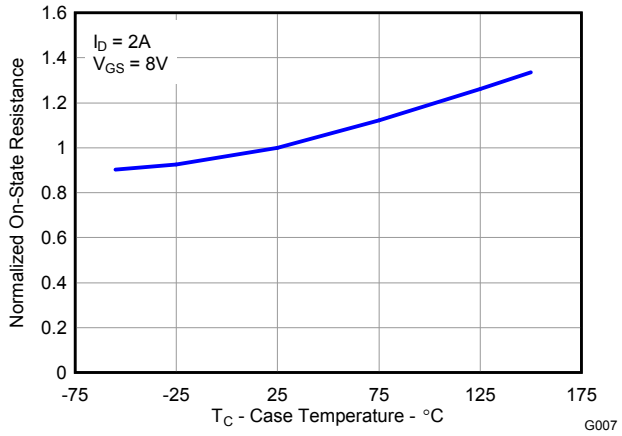


Figure 9. On Resistance vs. Temperature

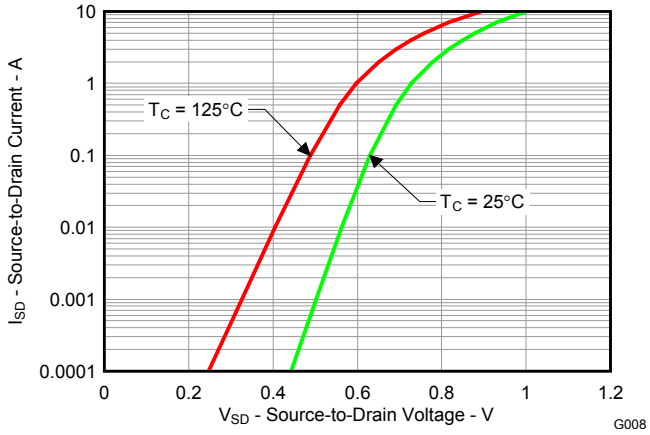


Figure 10. Typical Diode Forward Voltage

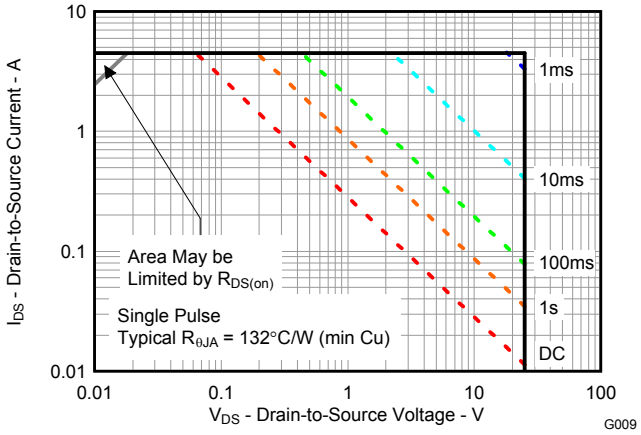


Figure 11. Maximum Safe Operating Area

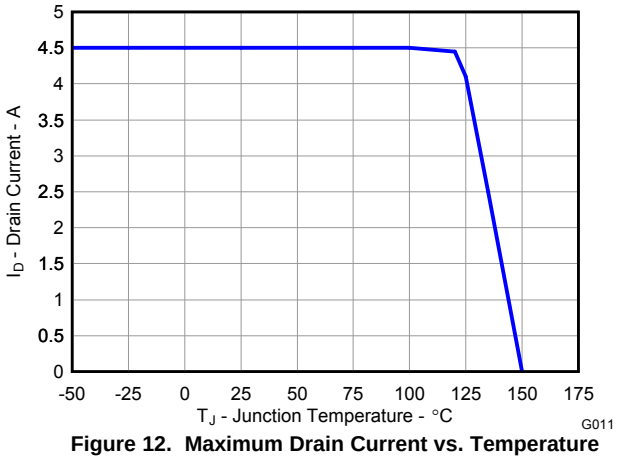
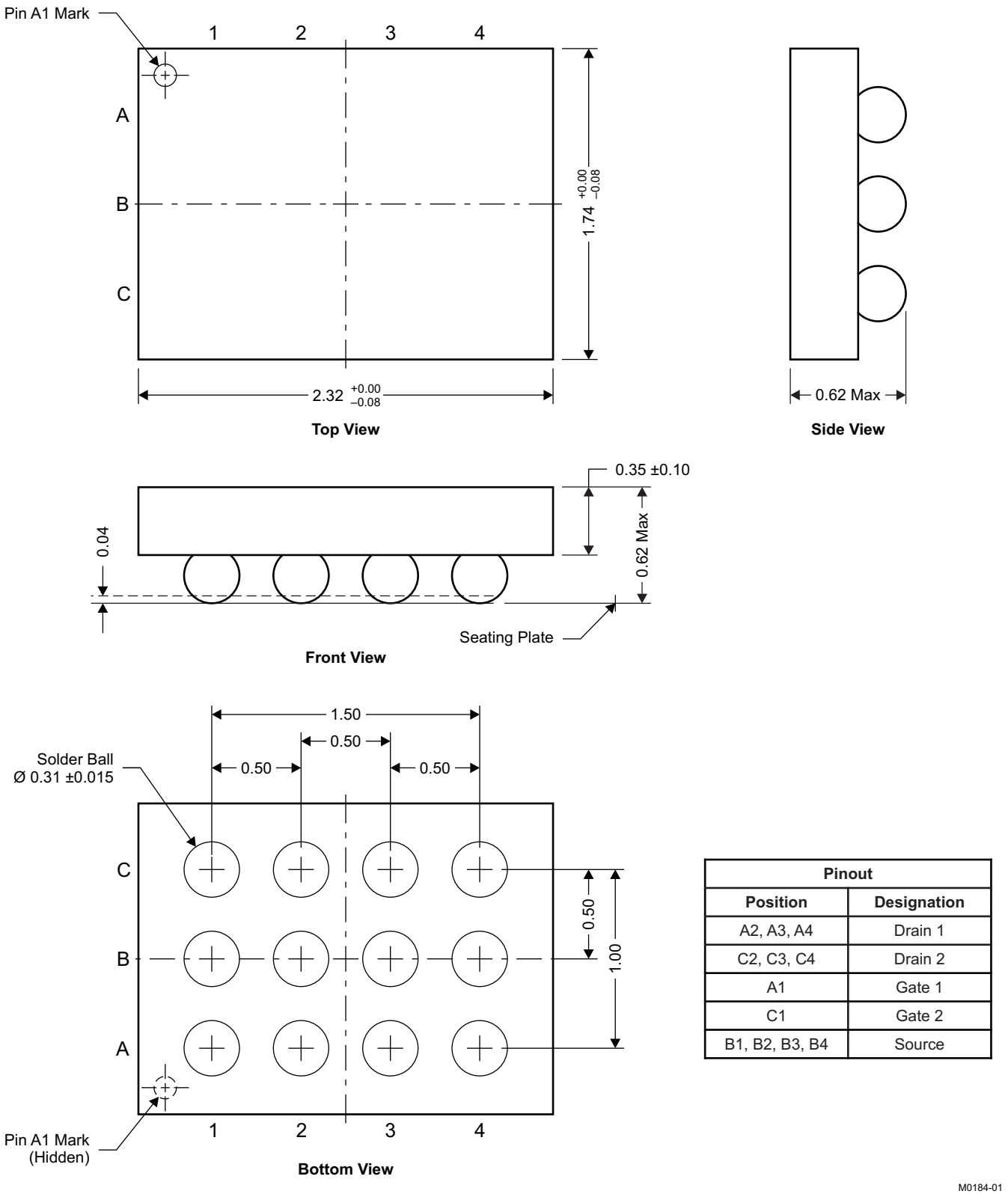


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

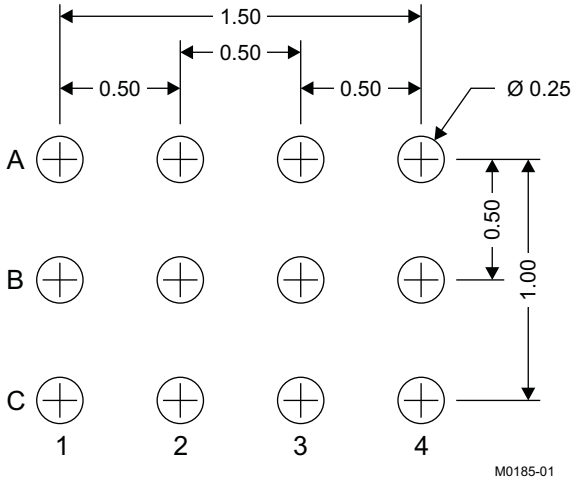
CSD86311W1723 Package Dimensions



Pinout	
Position	**Designation**
A2, A3, A4	Drain 1
C2, C3, C4	Drain 2
A1	Gate 1
C1	Gate 2
B1, B2, B3, B4	Source

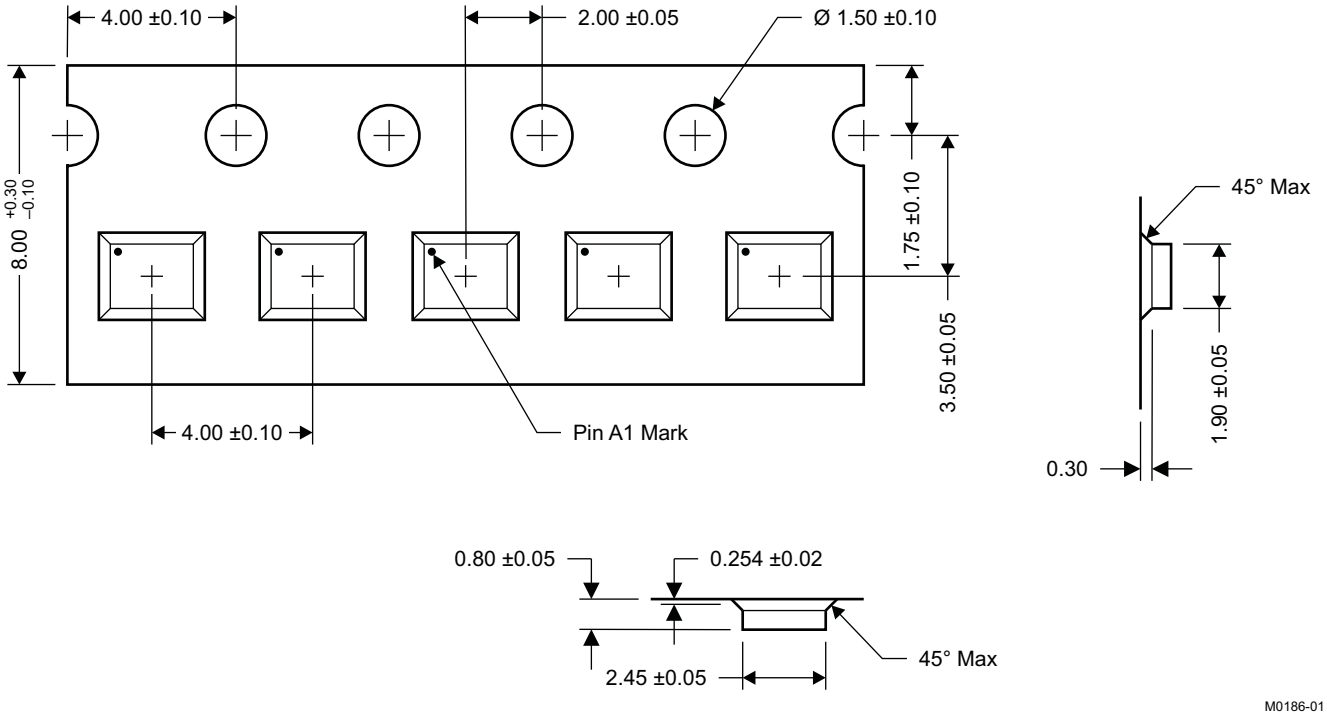
NOTE: All dimensions are in mm (unless otherwise specified)

Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified)

PACKAGING INFORMATION

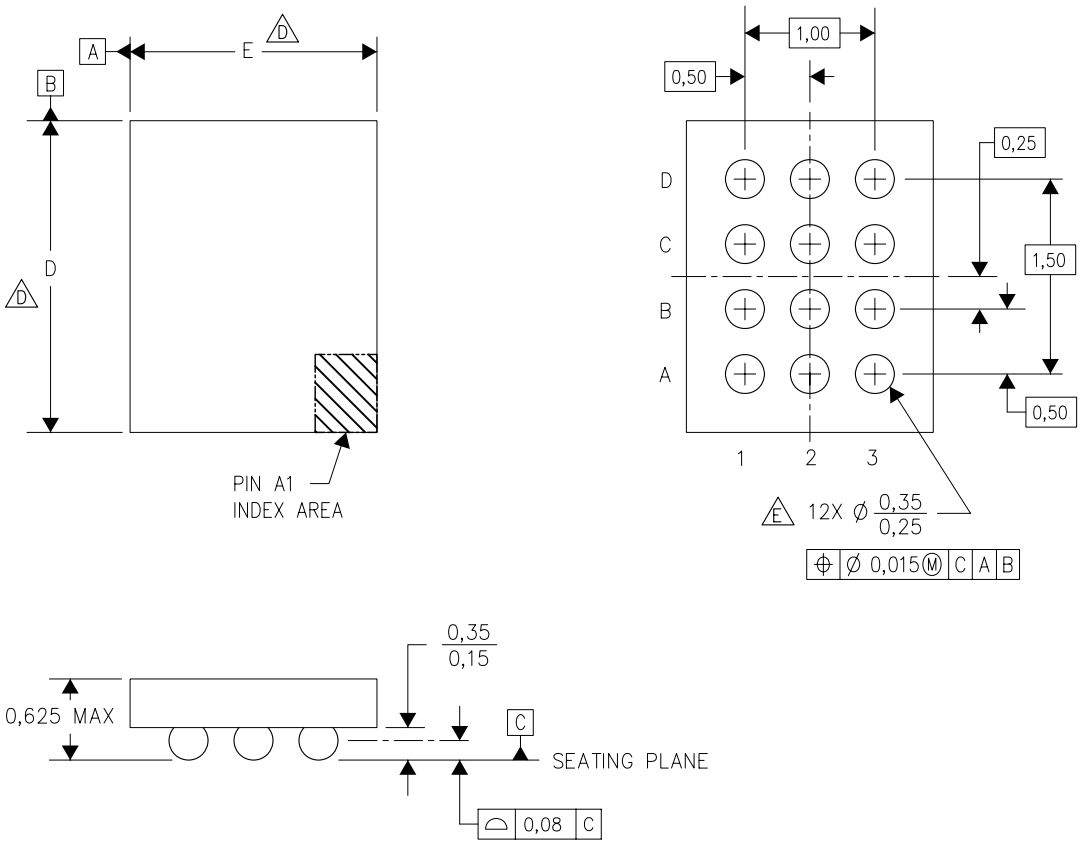
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
CSD86311W1723	ACTIVE	DSBGA	YZG	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

YZG (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZG package can have dimension D ranging from 1.94 to 2.65 mm and dimension E ranging from 1.44 to 2.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 4 x 3 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEG (Drawing #4204182) for tin–lead (SnPb) balls.

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