FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13734-9E

16-bit Microcontroller

CMOS

F²MC-16LX MB90330A Series

MB90333A/F334A/F335A/V330A

■ DESCRIPTION

The MB90330A series are 16-bit microcontrollers designed for applications, such as personal computer peripheral devices, that require USB communications. The USB feature supports not only 12-Mbps Function operation but also HOST operation. It is equipped with functions that are suitable for personal computer peripheral devices such as displays and audio devices, and control of mobile devices that support USB communications. While inheriting the AT architecture of the F²MC family, the instruction set supports the C language and extended addressing modes and contains enhanced signed multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, long word processing is now available by introducing a 32-bit accumulator.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- **Clock**
  - Built-in oscillation circuit and PLL clock frequency multiplication circuit
  - Oscillation clock
  - The main clock is the oscillation clock divided into 2 (for oscillation 6 MHz : 3 MHz)
  - Clock for USB is 48 MHz
  - Machine clock frequency of 6 MHz, 12 MHz, or 24 MHz selectable
  - Minimum execution time of instruction : 41.7 ns (6 MHz oscillation clock, 4-time multiplied : machine clock 24 MHz and at operating V_{CC} = 3.3 V).
- **The maximum memory space : 16 Mbytes**
- **24-bit addressing**

(Continued)

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

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- **Bank addressing**
- **Instruction system**
  - Data types : Bit, Byte, Word and Long word
  - Addressing mode (23 types)
  - Enhanced high-precision computing with 32-bit accumulator
  - Enhanced Multiply/Divide instructions with sign and the RETI instruction
- **Instruction system compatible with high-level language (C language) and multi-task**
  - Employing system stack pointer
  - Instruction set symmetry and barrel shift instructions
- **Program Patch Function (2 address pointer)**
- **4-byte instruction queue**
- **Interrupt function**
  - Priority levels are programmable
  - 32 interrupts function
- **Data transfer function**
  - Extended intelligent I/O service function (EI²OS) : Maximum of 16 channels
  - μDMAC : Maximum 16 channels
- **Low Power Consumption Mode**
  - Sleep mode (with the CPU operating clock stopped)
  - Time-base timer mode (with the oscillator clock and time-base timer operating)
  - Stop mode (with the oscillator clock stopped)
  - CPU intermittent operation mode (with the CPU operating at fixed intervals of set cycles)
  - Watch mode (with 32 kHz oscillator clock and watch timer operating)
- **Package**
  - LQFP-120P (FPT-120P-M24 : 0.40 mm pin pitch)
  - LQFP-120P (FPT-120P-M21 : 0.50 mm pin pitch)
- **Process : CMOS technology**
- **Operation guaranteed temperature : − 40 °C to + 85 °C (0 °C to + 70 °C when USB is in use)**

■ INTERNAL PERIPHERAL FUNCTION (RESOURCE)

- **I/O port : Max 94 ports**
- **Time-base timer : 1 channel**
- **Watchdog timer : 1 channel**
- **Watch timer : 1 channel**
- **16-bit reload timer : 3 channels**
- **Multi-functional timer**
  - 16-bit free run timer : 1 channel
  - Output compare : 4 channels
    An interrupt request can be output when the 16-bit free-run timer value matches the compare register value.
  - Input capture : 4 channels
    Upon detection of the effective edge of the signal input to the external input pin, the input capture unit sets the input capture data register to the 16-bit free-run timer value to output an interrupt request.
  - 8/16-bit PPG timer (8-bit × 6 channels or 16-bit × 3 channels) the period and duty of the output pulse can be set by the program.
  - 16-bit PWC timer : 1 channel
    Timer function and pulse width measurement function
- **UART : 4 channels**
  - Full-duplex double buffer (8-bit length)
  - Asynchronous transfer or clock-synchronous serial (Extended I/O serial) transfer can be set.
- **Extended I/O serial interface : 1 channel**
- **DTP/External interrupt circuit (8 channels)**
  - Activate the extended intelligent I/O service by external interrupt input
  - Interrupt output by external interrupt input
- **Delay interrupt output module**
  - Output an interrupt request for task switching
- **8/10-bit A/D converter : 16 channels**
  - 8-bit resolution or 10-bit resolution can be set.
- **USB : 1 channel**
  - USB function (correspond to USB Full Speed)
  - Full Speed is supported/Endpoint are specifiable up to six.
  - Dual port RAM (The FIFO mode is supported).
  - Transfer type : Control, Interrupt, Bulk, or Isochronous transfer possible
  - USB HOST function
- **I^2C Interface : 3 channels**
  - Supports Intel SM bus standard and Phillips I^2C bus standards
  - Two-wire data transfer protocol specification
  - Master and slave transmission/reception

■ PRODUCT LINEUP

Part number	MB90V330A	MB90F334A	MB90F335A	MB90333A
Type	For evaluation	Built-in Flash memory	Built-in Flash memory	Built-in MASK ROM
ROM capacity	No	384 Kbytes	512 Kbytes	256 Kbytes
RAM capacity	28 Kbytes	24 Kbytes	30 Kbytes	16 Kbytes
Emulator-specific power supply *	Yes	—		
CPU functions	Number of basic instructions : 351 instructions Minimum instruction execution time : 41.7 ns/at oscillation of 6 MHz (When 4 times are used : Machine clock of 24 MHz) Addressing type : 23 types Program Patch Function : For 2 address pointers Maximum memory space : 16 Mbytes			
Ports	I/O Ports (CMOS) 94 ports			
UART	Equipped with full-duplex double buffer Clock synchronous or asynchronous operation selectable It can also be used for I/O serial Built-in special baud-rate generator Built-in 4 channels			
16-bit reload timer	16-bit reload timer operation Built-in 3 channels			
Multi-functional timer	16-bit free run timer × 1 channel Output compare × 4 channels Input capture × 4 channels 8/16-bit PPG timer (8-bit mode × 6 channels, 16-bit mode × 3 channels) 16-bit PWC timer × 1 channel			
8/10-bit A/D converter	16 channels (input multiplex) 8-bit resolution or 10-bit resolution can be set. Conversion time : 7.16 μs at minimum (24 MHz machine clock at maximum)			
DTP/External interrupt	8 channels Interrupt factor : “L”→“H” edge/“H”→“L” edge/“L” level/“H” level selectable			
I^2C	3 channels			
Extended I/O serial interface	1 channel			
USB	1 channel USB function (correspond to USB Full Speed) USB HOST function			
External bus interface	For multi-bus/non-multi-bus			
Withstand voltage of 5 V	16 ports (excluding UTEST and I/O for I^2C)			
Low Power Consumption Mode	Sleep mode/Time-base timer mode/Stop mode/CPU intermittent mode/ Watch mode			
Process	CMOS			
Operating voltage	3.3 V ± 0.3 V (at maximum machine clock 24 MHz)			

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used. Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.

■ PACKAGES AND PRODUCT MODELS

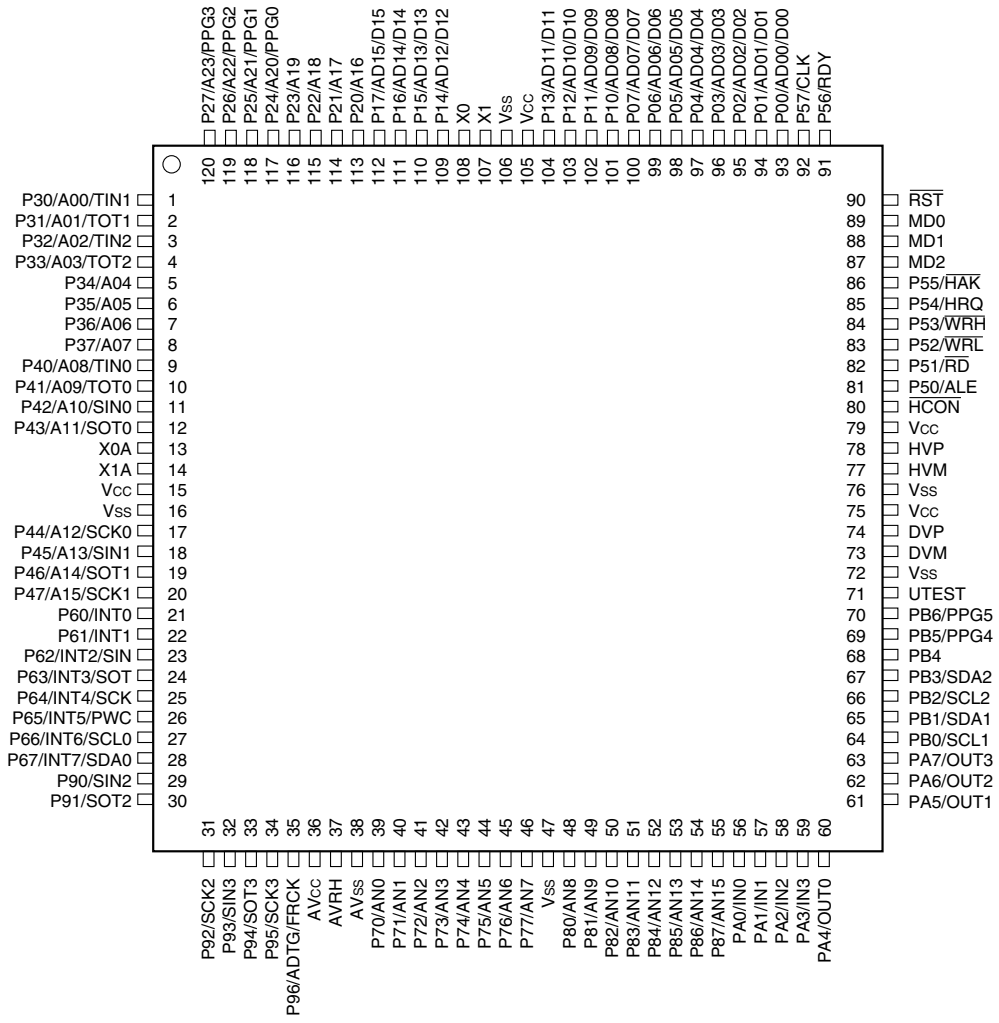
Package	MB90333A	MB90F334A	MB90F335A	MB90V330A
FPT-120P-M24 (LQFP-0.40 mm)	○	○	○	×
FPT-120P-M21 (LQFP-0.50 mm)	○	○	○	×
PGA-299C-A01 (PGA)	×	×	×	○

○ : Yes × : No

Note : For detailed information on each package, refer to “■ PACKAGE DIMENSIONS”.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-120P-M24 / FPT-120P-M21)

■ PIN DESCRIPTION

Pin no.	Pin name	I/O Circuit type*	Function
108, 107	X0, X1	A	Terminals to connect the oscillator. When connecting an external clock, leave the X1 pin side unconnected.
13, 14	X0A, X1A	A	32 kHz oscillation terminals.
90	$\overline{\text{RST}}$	F	External reset input pin.
93 to 100	P00 to P07	H	General purpose input/output port. The ports can be set to be added with a pull-up resistor (RD00 to RD07 = 1) by the pull-up resistor setting register (RDR0). (When the power output is set, it is invalid.)
	AD00 to AD07		Function as an I/O pin for the low-order external address and data bus in multiplex mode.
	D00 to D07		Function as an output pin for the low-order external data bus in non-multiplex mode.
101 to 104	P10 to P13	H	General purpose input/output port. The ports can be set to be added with a pull-up resistor (RD10 to RD13 = 1) by the pull-up resistor setting register (RDR1). (When the power output is set, it is invalid.)
	AD08 to AD11		Function as an I/O pin for the high-order external address and data bus in multiplex mode.
	D08 to D11		Function as an output pin for the high-order external data bus in non-multiplex mode.
109 to 112	P14 to P17	H	General purpose input/output port. The ports can be set to be added with a pull-up resistor (RD14 to RD17 = 1) by the pull-up resistor setting register (RDR1). (When the power output is set, it is invalid.)
	AD12 to D15		Function as an I/O pin for the high-order external address and data bus in multiplex mode.
	D12 to D15		Function as an output pin for the high-order external data bus in non-multiplex mode.
113 to 116	P20 to P23	D	This is a general purpose I/O port. When the bits of external address output control register (HACR) are set to “1” in external bus mode, these pins function as general purpose I/O ports.
	A16 to A19		When the bits of external address output control register (HACR) are set to “0” in multiplex mode, these pins function as address high output pins.
			When the bits of external address output control register (HACR) are set to “0” in non-multiplex mode, these pins function as address high output pins.

(Continued)

Pin no.	Pin name	I/O Circuit type*	Function
117 to 120	P24 to P27	D	This is a general purpose I/O port. When the bits of external address output control register (HACR) are set to “1” in external bus mode, these pins function as general purpose I/O ports.
	A20 to A23		When the bits of external address output control register (HACR) are set to “0” in multiplex mode, these pins function as address high output pins.
			When the bits of external address output control register (HACR) are set to “0” in non-multiplex mode, these pins function as address high output pins.
	PPG0 to PPG3		Function as ch.0 to ch.3 output pins for the 8-bit PPG timer.
1	P30	D	General purpose input/output port.
	A00		Function as the external address pin in non-multi-bus mode.
	TIN1		Function as an event input pin for 16-bit reload timer ch.1.
2	P31	D	General purpose input/output port.
	A01		Function as the external address pin in non-multi-bus mode.
	TOT1		Function as the output pin for 16-bit reload timer ch.1.
3	P32	D	General purpose input/output port.
	A02		Function as the external address pin in non-multi-bus mode.
	TIN2		Function as an event input pin for 16-bit reload timer ch.2.
4	P33	D	General purpose input/output port.
	A03		Function as the external address pin in non-multi-bus mode.
	TOT2		Function as the output pin for 16-bit reload timer ch.2.
5 to 8	P34 to P37	D	General purpose input/output port.
	A04 to A07		Function as the external address pin in non-multi-bus mode.
9	P40	G	General purpose input/output port.
	A08		Function as the external address pin in non-multi-bus mode.
	TIN0		Function as an event input pin for 16-bit reload timer ch.0.
10	P41	G	General purpose input/output port.
	A09		Function as the external address pin in non-multi-bus mode.
	TOT0		Function as the output pin for 16-bit reload timer ch.0.
11	P42	G	General purpose input/output port.
	A10		Function as the external address pin in non-multi-bus mode.
	SIN0		Function as a data input pin for UART ch.0.
12	P43	G	General purpose input/output port.
	A11		Function as the external address pin in non-multi-bus mode.
	SOT0		Function as a data output pin for UART ch.0.
17	P44	G	General purpose input/output port.
	A12		Function as the external address pin in non-multi-bus mode.
	SCK0		Function as a clock I/O pin for UART ch.0.

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Pin no.	Pin name	I/O Circuit type*	Function
18	P45	G	General purpose input/output port.
	A13		Function as the external address pin in non-multi-bus mode.
	SIN1		Function as a data input pin for UART ch.1.
19	P46	G	General purpose input/output port.
	A14		Function as the external address pin in non-multi-bus mode.
	SOT1		Function as a data output pin for UART ch.1.
20	P47	G	General purpose input/output port.
	A15		Function as the external address pin in non-multi-bus mode.
	SCK1		Function as a clock I/O pin for UART ch.1.
81	P50	L	General purpose input/output port.
	ALE		Function as the address latch enable signal pin in external bus mode.
82	P51	L	General purpose input/output port.
	$\overline{RD}$		Function as the read strobe output pin in external bus mode.
83	P52	L	General purpose input/output port.
	$\overline{WRL}$		Function as the data write strobe output pin on the lower side in external bus mode. This pin functions as a general-purpose I/O port when the WRE bit in the EPCR register is “0”.
84	P53	L	General purpose input/output port.
	$\overline{WRH}$		Function as the data write strobe output pin on the higher side in bus width 16-bit external bus mode. This pin functions as a general-purpose I/O port when the WRE bit in the EPCR register is “0”.
85	P54	L	General purpose input/output port.
	HRQ		Function as the hold request input pin in external bus mode. This pin functions as a general-purpose I/O port when the HDE bit in the EPCR register is “0”.
86	P55	L	General purpose input/output port.
	$\overline{HAK}$		Function as the hold acknowledge output pin in external bus mode. This pin functions as a general-purpose I/O port when the HDE bit in the EPCR register is “0”.
91	P56	L	General purpose input/output port.
	RDY		Function as the external ready input pin in external bus mode. This pin functions as a general-purpose I/O port when the RYE bit in the EPCR register is “0”.
92	P57	L	General purpose input/output port.
	CLK		Function as the machine cycle clock output pin in external bus mode. This pin functions as a general-purpose I/O port when the CKE bit in the EPCR register is “0”.
21, 22	P60, P61	C	General purpose input/output port. (With stand voltage of 5 V)
	INT0, INT1		Function as external interrupt ch.0 and ch.1 input pins.

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Pin no.	Pin name	I/O Circuit type*	Function
23	P62	C	General purpose input/output ports. (Withstand voltage of 5 V)
	INT2		Function as an external interrupt ch.2 input pin.
	SIN		Extended I/O serial interface data input pin.
24	P63	C	General purpose input/output port. (Withstand voltage of 5 V)
	INT3		Function as an external interrupt ch.3 input pin.
	SOT		Extended I/O serial interface data output pin.
25	P64	C	General purpose input/output port. (Withstand voltage of 5 V)
	INT4		Function as an external interrupt ch.4 input pin.
	SCK		Extended I/O serial interface clock input/output pin.
26	P65	C	General purpose input/output port. (Withstand voltage of 5 V)
	INT5		Function as an external interrupt ch.5 input pin.
	PWC		Function as the PWC input pin.
27	P66	C	General purpose input/output port. (Withstand voltage of 5 V)
	INT6		Function as an external interrupt ch.6 input pin.
	SCL0		Function as the ch.0 clock I/O pin for the I^2C interface. Set port output to High-Z during I^2C interface operations.
28	P67	C	General purpose input/output port. (Withstand voltage of 5 V)
	INT7		Function as an external interrupt ch.7 input pin.
	SDA0		Function as the ch.0 data I/O pin for the I^2C interface. Set port output to High-Z during I^2C interface operations.
39 to 46	P70 to P77	I	General purpose input/output port.
	AN0 to AN7		Function as input pins for analog ch.0 to ch.7.
48 to 55	P80 to P87	I	General purpose input/output port.
	AN8 to AN15		Function as input pins for analog ch.8 to ch.15.
29	P90	D	General purpose input/output port.
	SIN2		Function as a data input pin for UART ch.2.
30	P91	D	General purpose input/output port.
	SOT2		Function as a data output pin for UART ch.2.
31	P92	D	General purpose input/output port.
	SCK2		Function as a clock I/O pin for UART ch.2.
32	P93	D	General purpose input/output port.
	SIN3		Function as a data input pin for UART ch.3.
33	P94	D	General purpose input/output port.
	SOT3		Function as a data output pin for UART ch.3.
34	P95	D	General purpose input/output port.
	SCK3		Function as a clock I/O pin for UART ch.3.
35	P96	C	General purpose input/output port. (Withstand voltage of 5 V)
	ADTG		Function as the external trigger input pin when the A/D converter is being used.
	FRCK		Function as the external clock input pin when the free-run timer is being used.

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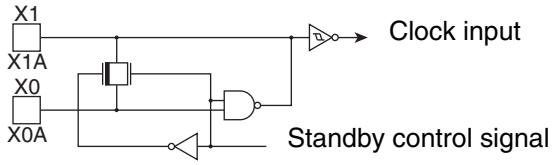
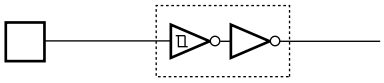
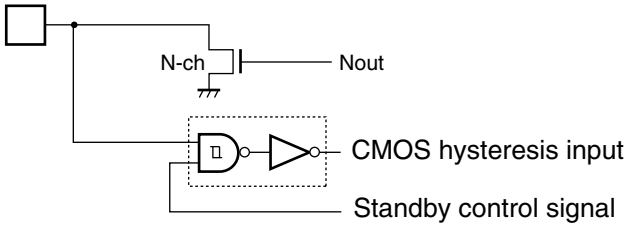
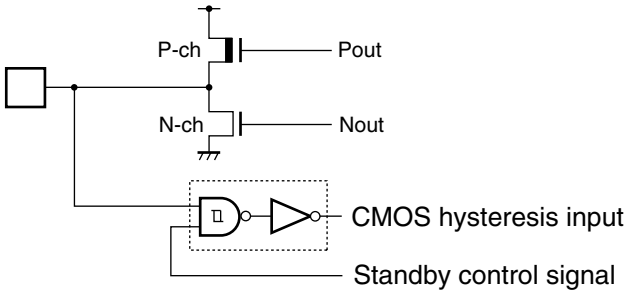
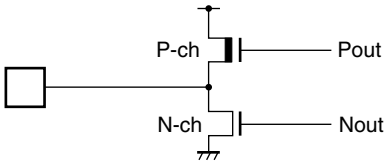
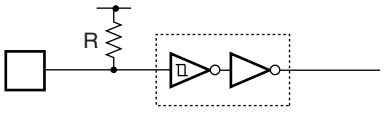
Pin no.	Pin name	I/O Circuit type*	Function
56 to 59	PA0 to PA3	C	General purpose input/output port. (Withstand voltage of 5 V)
	IN0 to IN3		Function as the input capture ch.0 to ch.3 trigger inputs.
60 to 63	PA4 to PA7	C	General purpose input/output port. (Withstand voltage of 5 V)
	OUT0 to OUT3		Function as the output compare ch.0 to ch.3 event output pins.
64	PB0	C	General purpose input/output port. (Withstand voltage of 5 V)
	SCL1		Function as the ch.1 clock I/O pin for the I²C interface. Set port output to High-Z during I²C interface operations.
65	PB1	C	General purpose input/output port. (Withstand voltage of 5 V)
	SDA1		Function as the ch.1 data I/O pin for the I²C interface. Set port output to High-Z during I²C interface operations.
66	PB2	C	General purpose input/output port. (Withstand voltage of 5 V)
	SCL2		Function as the ch.2 clock I/O pin for the I²C interface. Set port output to High-Z during I²C interface operations.
67	PB3	C	General purpose input/output port. (Withstand voltage of 5 V)
	SDA2		Function as the ch.2 data I/O pin for the I²C interface. Set port output to High-Z during I²C interface operations.
68	PB4	C	General purpose input/output port. (Withstand voltage of 5 V)
69, 70	PB5, PB6	D	General purpose input/output port.
	PPG4, PPG5		Function as ch.4 and ch.5 output pins for the 8-bit PPG timer.
71	UTEST	C	USB test pin. Connect this to a pull-down resistor during normal usage.
73	DVM	K	USB function D– pin.
74	DVP	K	USB function D+ pin.
77	HVM	K	USB HOST D– pin.
78	HVP	K	USB HOST D+ pin.
80	$\overline{\text{HCON}}$	E	External pull-up resistor connect pin.
36	AVcc	—	A/D converter power supply pin.
37	AVRH	J	A/D converter external reference power supply pin.
38	AVss	—	A/D converter power supply pin.
87 to 89	MD2 to MD0	B	Operation mode select input pin.
15, 75, 79, 105	Vcc	—	Power supply pin.
16, 47, 72, 76, 106	Vss	—	Power supply pin (GND).

* : For circuit information, refer to “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• High-rate oscillation feedback resistor, approx.1 MΩ • Low-rate oscillation feedback resistor, approx.10 MΩ • With standby control
B		CMOS hysteresis input
C		• CMOS hysteresis input • N-ch open drain output
D		• CMOS output • CMOS hysteresis input (With input interception function at standby) Notes : • Share one output buffer because both output of I/O port and internal resource are used. • Share one input buffer because both input of I/O port and internal resource are used.
E		CMOS output
F		CMOS hysteresis input with pull-up resistor

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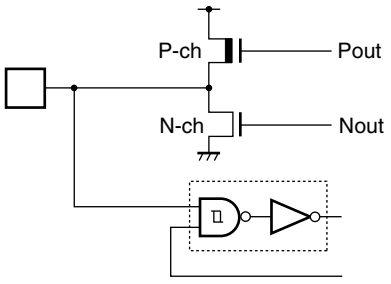
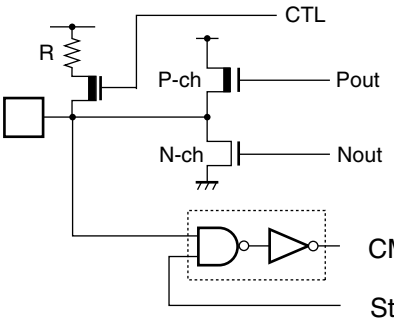
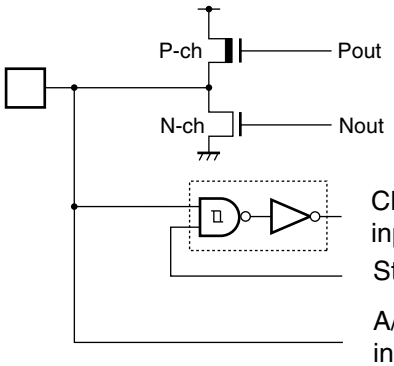
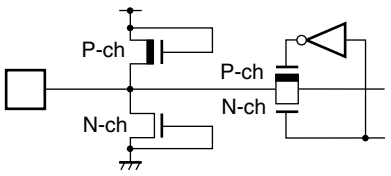
Type	Circuit	Remarks
G	 Open drain control signal CMOS hysteresis input Standby control signal	• CMOS output • CMOS hysteresis input (With input interception function at standby) With open drain control signal
H	 CMOS input Standby control signal	• CMOS output • CMOS input (With input interception function at standby) • With input pull-up register control
I	 CMOS hysteresis input Standby control signal A/D converter analog input	• CMOS output • CMOS hysteresis input (With input interception function at standby) • Analog input (The A/D converter analog input is enabled when the corresponding bit in the analog input enable register (ADER) is 1.) Notes: • Because the output of the I/O port and the output of internal resources are used combinedly, one output buffer is shared. • Because the input of the I/O port and the input of internal resources are used combinedly, one input buffer is shared.
J	 AVRH input A/D converter analog input enable signal	A/D converter (AVRH) voltage input pin

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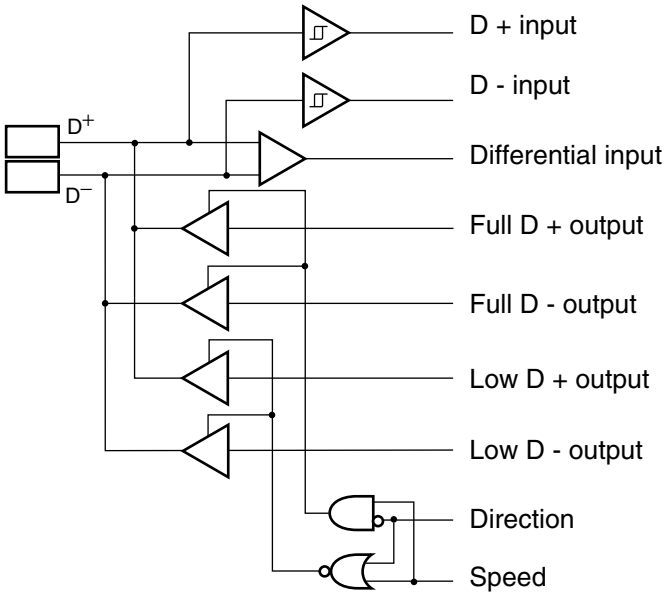
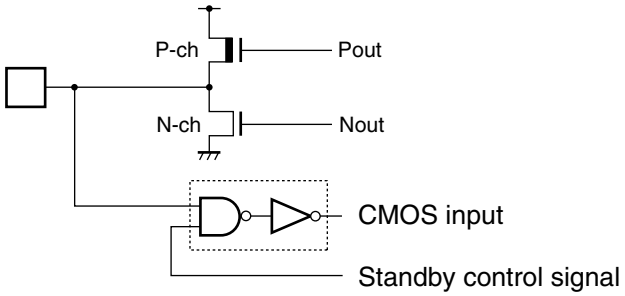
Type	Circuit	Remarks
K		USB I/O pin
L		• CMOS output • CMOS input • With standby control

■ HANDLING DEVICES

1. Preventing latch-up and turning on power supply

Latch-up may occur on CMOS IC under the following conditions:

- If a voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins.
- A voltage higher than the rated voltage is applied between V_{CC} pin and V_{SS} pin.
- If the AV_{CC} power supply is turned on before the V_{CC} voltage.

Ensure that you apply a voltage to the analog power supply at the same time as V_{CC} or after you turn on the digital power supply (when you perform power-off, turn off the analog power supply first or at the same time as V_{CC} and the digital power supply).

If latch-up occurs, the supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Use meticulous care not to let any voltage exceed the maximum rating.

2. Treatment of unused pins

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leading to permanent damage.
Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

3. Treatment of power supply pins on models with A/D converters

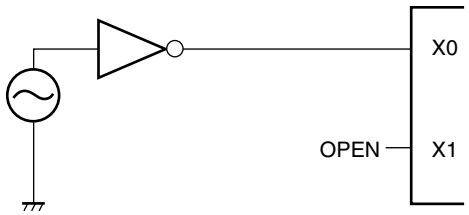
Even when the A/D converters are not in use, be sure to make the necessary connections AV_{CC} = AVRH = V_{CC}, and AV_{SS} = V_{SS}.

4. About the attention when the external clock is used

Even when using an external clock signal, an oscillation stabilization delay is applied after a power-on reset or when recovering from sub clock or stop mode. When suing an external clock, 25 MHz should be the upper frequency limit.

The following figure shows a sample use of external clock signals.

- Using external clock



5. Treatment of power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 μF between V_{CC} pin and V_{SS} pin near this device.

6. About Crystal oscillator circuit

Noise near the X0/X1 pins and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1 pins and X0A/X1A pins, the crystal oscillator (or the ceramic oscillator) and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0/X1 pins and X0A/X1A pins surrounded by ground plane because stable operation can be expected with such a layout.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

7. Caution on Operations during PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

8. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. For stabilization reference, the supply voltage should be stabilized so that V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard V_{CC} supply voltage and the transient regulation does not exceed 0.1 V/ms at temporary changes such as power supply switching.

9. When the dual-supply is used as a single-supply device

If you are using only a single-system of the MB90330A series that come in the dual-system product, use it with X0A = V_{SS} : X1A = OPEN.

10. Writing to flash memory

For serial writing to flash memory, always make sure that the operating voltage V_{CC} is between 3.13 V and 3.6 V.

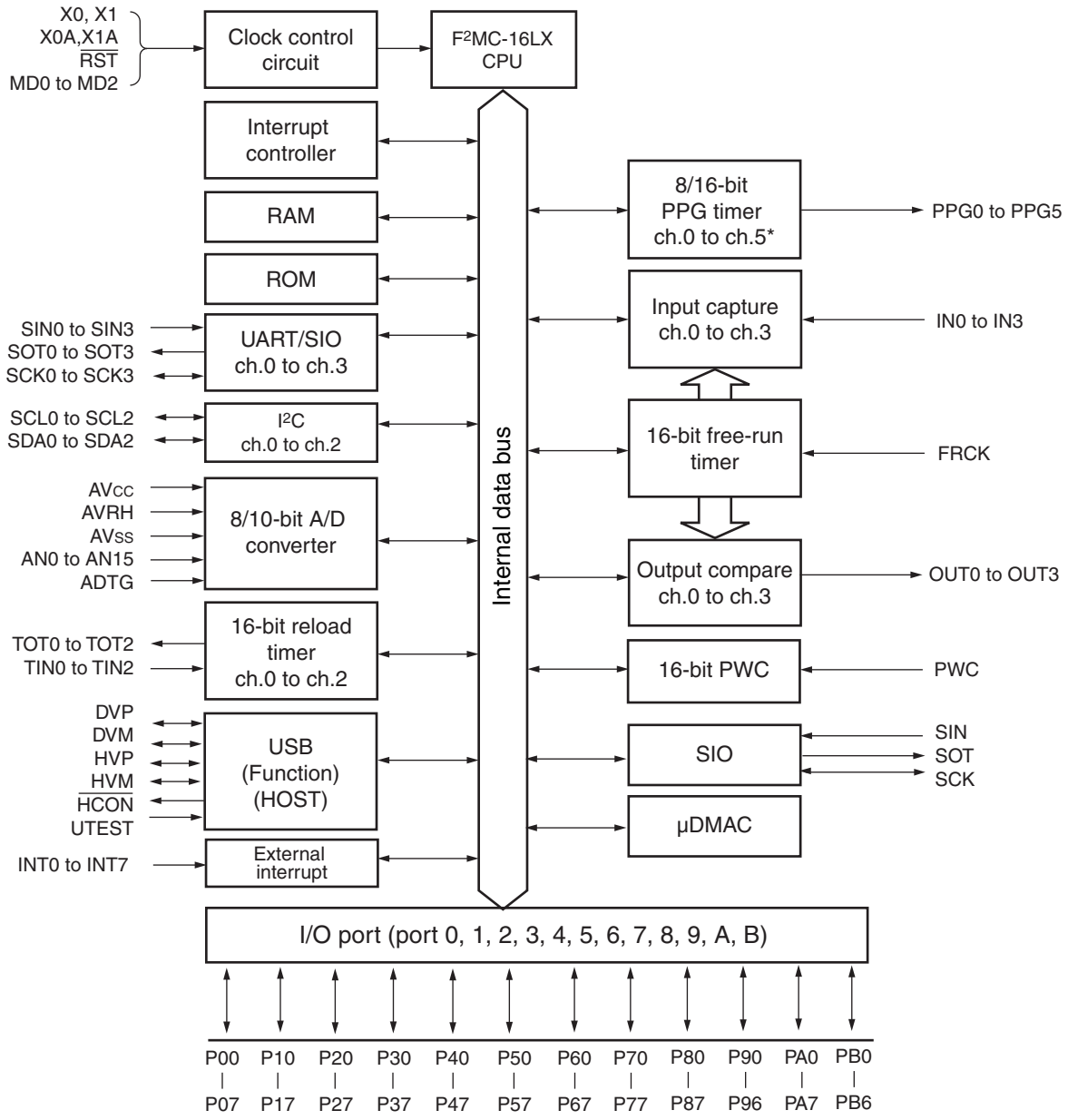
For normal writing to flash memory, always make sure that the operating voltage V_{CC} is between 3.0 V and 3.6 V.

11. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example, apply a checksum to detect an error. If an error is detected, retransmit the data.

■ BLOCK DIAGRAM



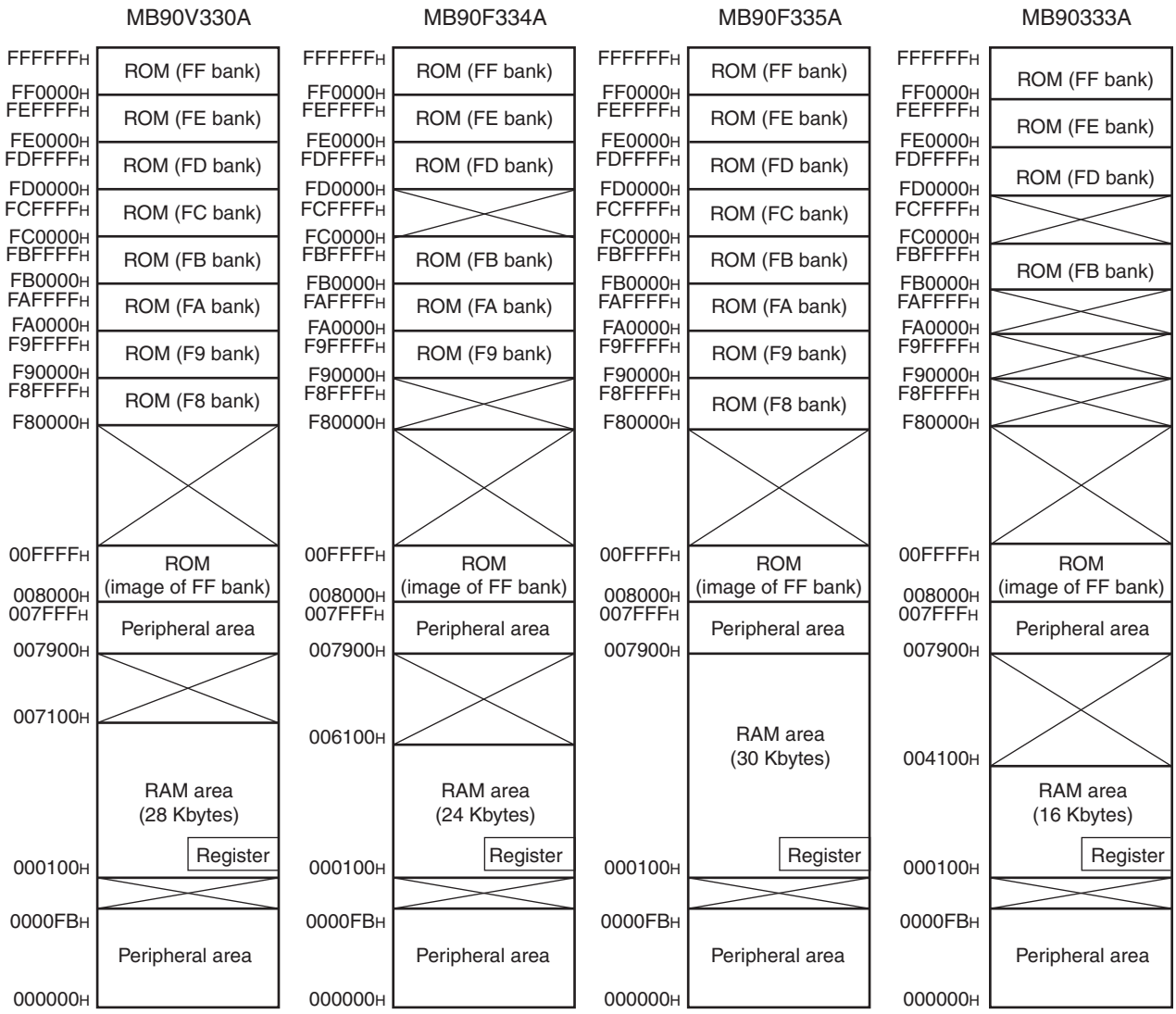
* : Channel for use in 8-bit mode. 3 channels (ch.1, ch.3, ch.5) are used in 16-bit mode.

Note : I/O ports share pins with peripheral function (resources) .
For details, refer to “■ PIN ASSIGNMENT” and “■ PIN DESCRIPTION”.
Note also that pins used for peripheral function (resources) cannot serve as I/O ports.

■ MEMORY MAP

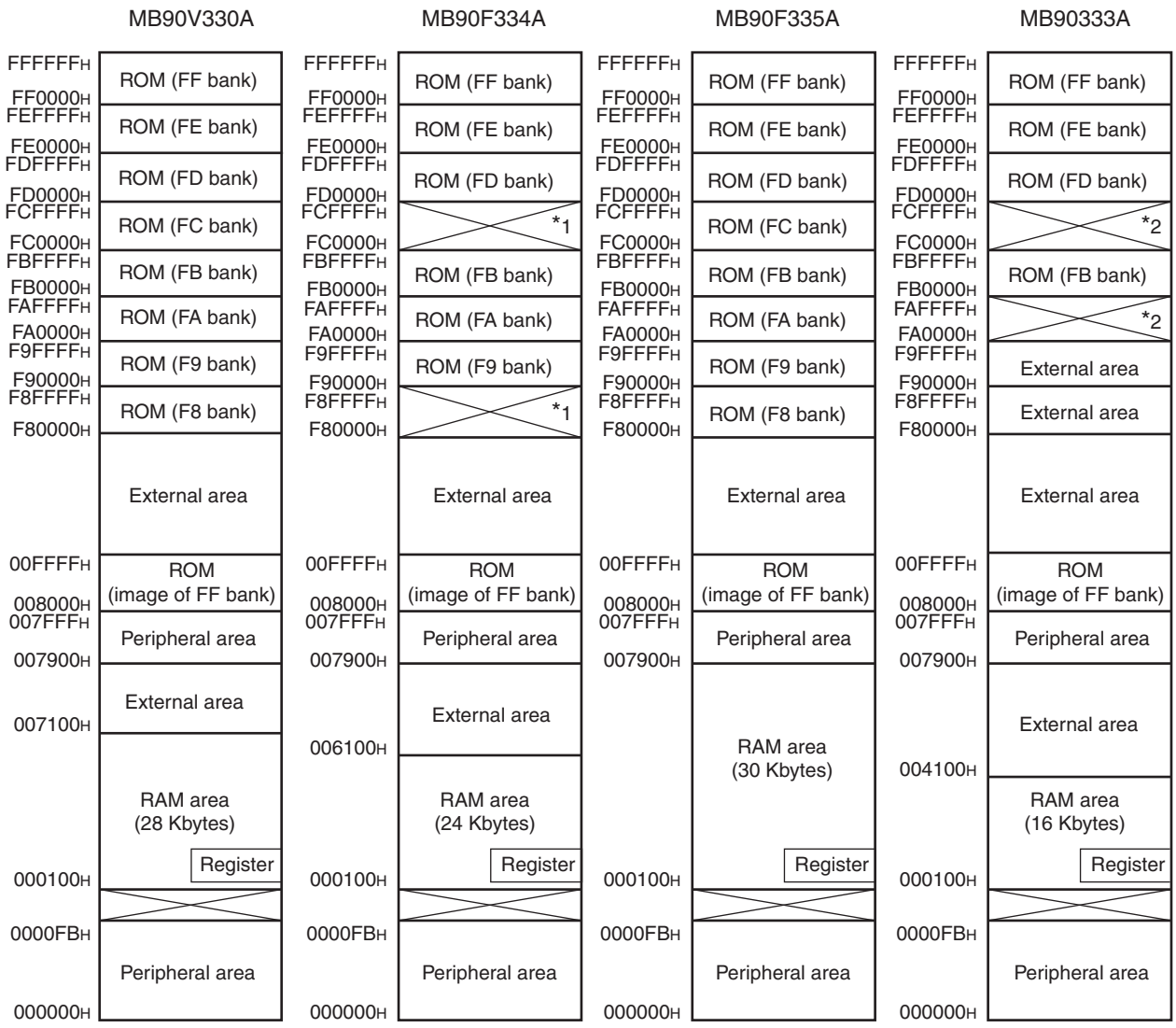
Memory map of MB90330A series (1/3)

Single chip mode (with ROM mirror function)



Memory map of MB90330A series (2/3)

Internal ROM external bus mode (with ROM mirror function)

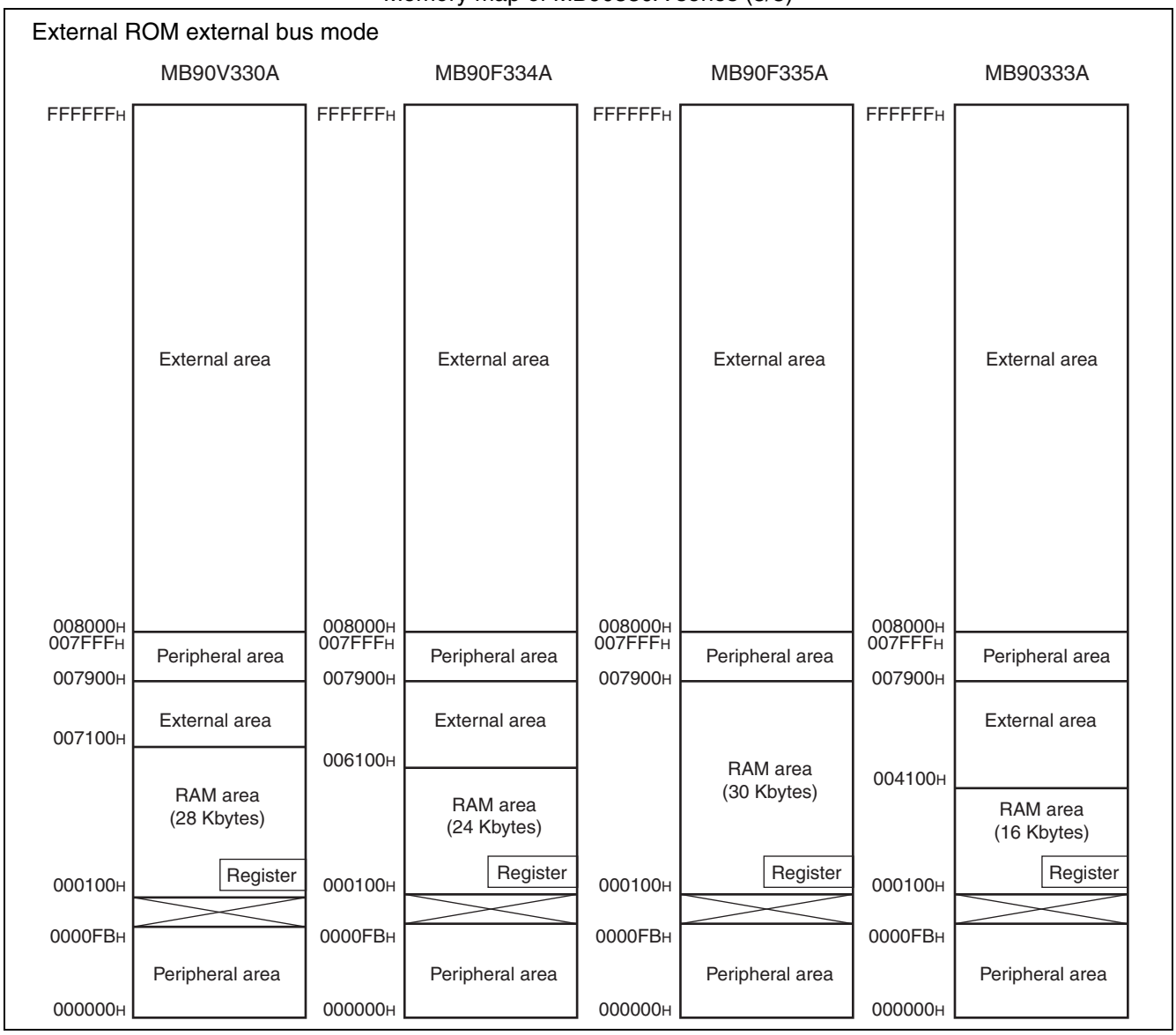


*1 : In the area of F80000H to F8FFFFH and FC0000H to FCFFFFH at MB90F334A, a value of “1” is read at read operating.

*2 : In the area of FA0000H to FAFFFFH and FC0000H to FCFFFFH at MB90333A, a value of “1” is read at read operating.

Memory map of MB90330A series (3/3)

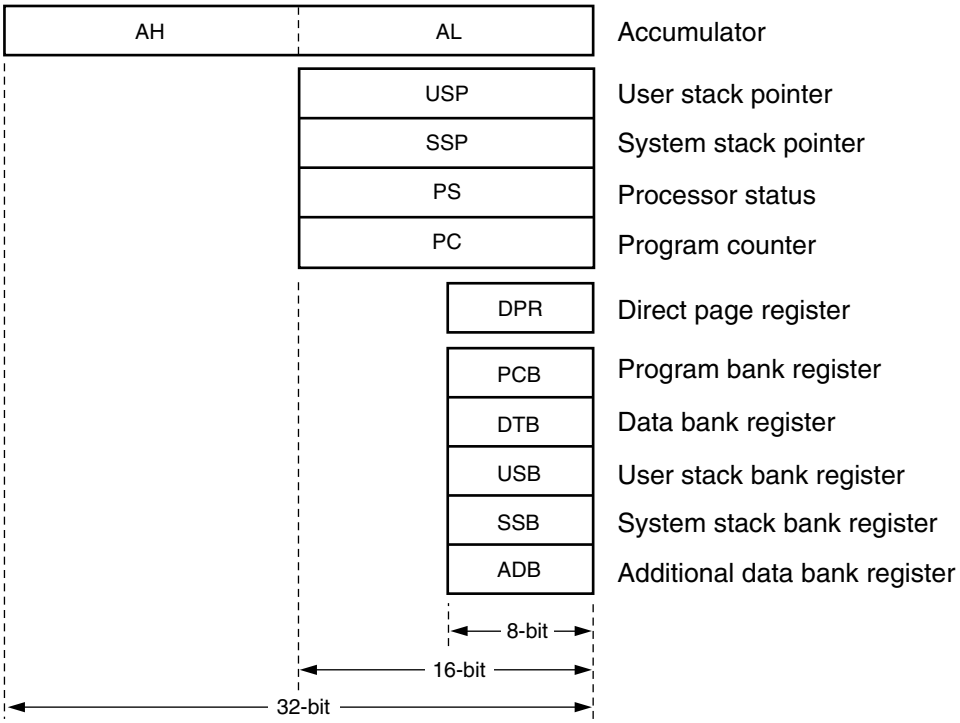
External ROM external bus mode



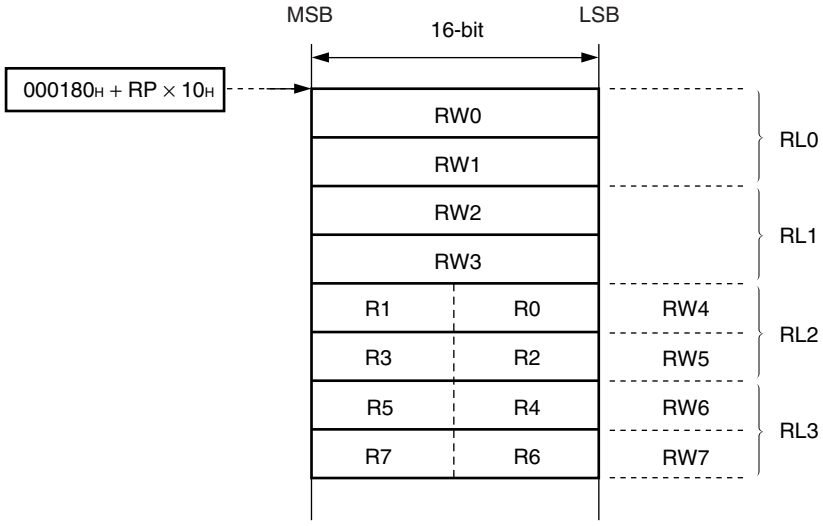
Notes:
- When the ROM mirror function register has been set, the mirror image data at higher addresses ("FF8000H to FFFFFFH") of bank FF is visible from the higher addresses ("008000H to 00FFFFH") of bank 00.
- The ROM mirror function is effective for using the C compiler small model.
- The lower 16-bit addresses of bank FF are equivalent to those of bank 00. Since the ROM area in bank FF exceeds 48 Kbytes, however, the mirror image of all the data in the ROM area cannot be reproduced in bank 00.
- When the C compiler small model is used, the data table mirror image can be shown at "008000H to 00FFFFH" by storing the data table at "FF8000H to FFFFFFH". Therefore, data tables in the ROM area can be referred without declaring the far addressing with the pointer.
- MB90F335A has the larger size of RAM area than MB90V330A, so that the emulation memory area needs to be set in the tools for a larger size of emulation area than 007100H.
  For details of setting, please refer to "Notes on Debug Environment Setting for MB90330A Series" by clicking "Application note" at the following URL.
  http://edevice.fujitsu.com/micom/en-support/
- 3 cycles are required to access to the emulation memory area (007100H to 0078FFH), which is 1 cycle more than to the mounted RAM area.

■ F²MC-16LX CPU PROGRAMMING MODEL

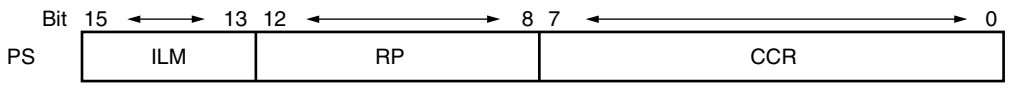
• Dedicated register



• General purpose register



• Processor status



■ I/O MAP

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000000H	PDR0	Port 0 Data Register	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 Data Register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 Data Register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 Data Register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 Data Register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 Data Register	R/W	Port 5	XXXXXXXXB
000006H	PDR6	Port 6 Data Register	R/W	Port 6	XXXXXXXXB
000007H	PDR7	Port 7 Data Register	R/W	Port 7	XXXXXXXXB
000008H	PDR8	Port 8 Data Register	R/W	Port 8	XXXXXXXXB
000009H	PDR9	Port 9 Data Register	R/W	Port 9	- XXXXXXXB
00000AH	PDRA	Port A Data Register	R/W	Port A	XXXXXXXXB
00000BH	Prohibited				
00000CH	PDRB	Port B Data Register	R/W	Port B	- XXXXXXXB
00000DH	DDRB	Port B Direction Register	R/W	Port B	- 0 0 0 0 0 0 0B
00000EH	Prohibited				
00000FH					
000010H	DDR0	Port 0 Direction Register	R/W	Port 0	0 0 0 0 0 0 0 0B
000011H	DDR1	Port 1 Direction Register	R/W	Port 1	0 0 0 0 0 0 0 0B
000012H	DDR2	Port 2 Direction Register	R/W	Port 2	0 0 0 0 0 0 0 0B
000013H	DDR3	Port 3 Direction Register	R/W	Port 3	0 0 0 0 0 0 0 0B
000014H	DDR4	Port 4 Direction Register	R/W	Port 4	0 0 0 0 0 0 0 0B
000015H	DDR5	Port 5 Direction Register	R/W	Port 5	0 0 0 0 0 0 0 0B
000016H	DDR6	Port 6 Direction Register	R/W	Port 6	0 0 0 0 0 0 0 0B
000017H	DDR7	Port 7 Direction Register	R/W	Port 7	0 0 0 0 0 0 0 0B
000018H	DDR8	Port 8 Direction Register	R/W	Port 8	0 0 0 0 0 0 0 0B
000019H	DDR9	Port 9 Direction Register	R/W	Port 9	- 0 0 0 0 0 0 0B
00001AH	DDRA	Port A Direction Register	R/W	Port A	0 0 0 0 0 0 0 0B
00001BH	ODR4	Port 4 Output Pin Register	R/W	Port 4 (open drain control)	0 0 0 0 0 0 0 0B
00001CH	RDR0	Port 0 Pull-up Resistance Register	R/W	Port 0 (PULL-UP)	0 0 0 0 0 0 0 0B
00001DH	RDR1	Port 1 Pull-up Resistance Register	R/W	Port 1 (PULL-UP)	0 0 0 0 0 0 0 0B
00001EH	ADER0	Analog Input Enable Register 0	R/W	Port 7, 8, A/D	1 1 1 1 1 1 1 1B
00001FH	ADER1	Analog Input Enable Register 1	R/W	Port 7, 8, A/D	1 1 1 1 1 1 1 1B
000020H	SMR0	Serial Mode Register 0	R/W	UART0	0 0 1 0 0 0 0 0B
000021H	SCR0	Serial Control Register 0	R/W		0 0 0 0 0 1 0 0B
000022H	SIDR0	Serial Input Data Register 0	R		XXXXXXXXB
	SODR0	Serial Output Data Register 0	W		
000023H	SSR0	Serial Status Register 0	R/W		0 0 0 0 1 0 0 0B
000024H	UTRLR0	UART Prescaler Reload Register 0	R/W	Communication Prescaler (UART0)	0 0 0 0 0 0 0 0B
000025H	UTCR0	UART Prescaler Control Register 0	R/W		0 0 0 0 - 0 0 0B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000026H	SMR1	Serial Mode Register 1	R/W	UART1	0 0 1 0 0 0 0 0B
000027H	SCR1	Serial Control Register 1	R/W		0 0 0 0 0 1 0 0B
000028H	SIDR1	Serial Input Data Register 1	R		XXXXXXXXB
	SODR1	Serial Output Data Register 1	W		
000029H	SSR1	Serial Status Register 1	R/W		0 0 0 0 1 0 0 0B
00002AH	UTRLR1	UART Prescaler Reload Register 1	R/W	Communication Prescaler (UART1)	0 0 0 0 0 0 0 0B
00002BH	UTCR1	UART Prescaler Control Register 1	R/W		0 0 0 0 - 0 0 0B
00002CH	SMR2	Serial Mode Register 2	R/W	UART2	0 0 1 0 0 0 0 0B
00002DH	SCR2	Serial Control Register 2	R/W		0 0 0 0 0 1 0 0B
00002EH	SIDR2	Serial Input Data Register 2	R		XXXXXXXXB
	SODR2	Serial Output Data Register 2	W		
00002FH	SSR2	Serial Status Register 2	R/W		0 0 0 0 1 0 0 0B
000030H	UTRLR2	UART Prescaler Reload Register 2	R/W	Communication Prescaler (UART2)	0 0 0 0 0 0 0 0B
000031H	UTCR2	UART Prescaler Control Register 2	R/W		0 0 0 0 - 0 0 0B
000032H	SMR3	Serial Mode Register 3	R/W	UART3	0 0 1 0 0 0 0 0B
000033H	SCR3	Serial Control Register 3	R/W		0 0 0 0 0 1 0 0B
000034H	SIDR3	Serial Input Data Register 3	R		XXXXXXXXB
	SODR3	Serial Output Data Register 3	W		
000035H	SSR3	Serial Status Register 3	R/W		0 0 0 0 1 0 0 0B
000036H	UTRLR3	UART Prescaler Reload Register 3	R/W	Communication Prescaler (UART3)	0 0 0 0 0 0 0 0B
000037H	UTCR3	UART Prescaler Control Register 3	R/W		0 0 0 0 - 0 0 0B
000038H to 00003BH	Prohibited				
00003CH	ENIR	DTP/Interrupt Enable Register	R/W	DTP/External Interrupt	0 0 0 0 0 0 0 0B
00003DH	EIRR	DTP/Interrupt Source Register	R/W		0 0 0 0 0 0 0 0B
00003EH	ELVR	Request Level Setting Register Lower	R/W		0 0 0 0 0 0 0 0B
00003FH		Request Level Setting Register Upper	R/W		0 0 0 0 0 0 0 0B
000040H	ADCS0	A/D Control Status Register Lower	R/W	8/10-bit A/D Converter	0 0 - - - - - 0B
000041H	ADCS1	A/D Control Status Register Upper	R/W		0 0 0 0 0 0 0 0B
000042H	ADCR0	A/D Data Register Lower	R/W		XXXXXXXXB
000043H	ADCR1	A/D Data Register Upper	R/W		0 0 1 0 1 XXXB
000044H	Prohibited				
000045H	ADMR	A/D Conversion Channel Selection Register	R/W	8/10-bit A/D Converter	0 0 0 0 0 0 0 0B
000046H	PPGC0	PPG0 Operation Mode Control Register	R/W	PPG ch.0	0X0 0 0XX1B
000047H	PPGC1	PPG1 Operation Mode Control Register	R/W	PPG ch.1	0X0 0 0 0 0 1B
000048H	PPGC2	PPG2 Operation Mode Control Register	R/W	PPG ch.2	0X0 0 0XX1B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000049H	PPGC3	PPG3 Operation Mode Control Register	R/W	PPG ch.3	0X0 0 0 0 0 1B
00004AH	PPGC4	PPG4 Operation Mode Control Register	R/W	PPG ch.4	0X0 0 0XX1B
00004BH	PPGC5	PPG5 Operation Mode Control Register	R/W	PPG ch.5	0X0 0 0 0 0 1B
00004CH	PPG01	PPG0 and PPG1 Output Control Register	R/W	PPG ch.0/ch.1	0 0 0 0 0 0XXB
00004DH	Prohibited				
00004EH	PPG23	PPG2 and PPG3 Output Control Register	R/W	PPG ch.2/ch.3	0 0 0 0 0 0 XXB
00004FH	Prohibited				
000050H	PPG45	PPG4 and PPG5 Output Control Register	R/W	PPG ch.4/ch.5	0 0 0 0 0 0 XXB
000051H	Prohibited				
000052H	ICS01	Input Capture Control Status Register 01	R/W	Input Capture ch.0/ch.1	0 0 0 0 0 0 0 0B
000053H	ICS23	Input Capture Control Status Register 23	R/W	Input Capture ch.2/ch.3	0 0 0 0 0 0 0 0B
000054H	OCS0	Output Compare Control Register ch.0 Lower	R/W	Output Compare ch.0/ch.1	0 0 0 0 - - 0 0B
000055H	OCS1	Output Compare Control Register ch.1 Upper	R/W		- - - 0 0 0 0 0B
000056H	OCS2	Output Compare Control Register ch.2 Lower	R/W	Output Compare ch.2/ch.3	0 0 0 0 - - 0 0B
000057H	OCS3	Output Compare Control Register ch.3 Upper	R/W		- - - 0 0 0 0 0B
000058H	SMCS	Serial Mode Control Status Register	R/W	Extended Serial I/O	XXXX0 0 0 0B
000059H					0 0 0 0 0 0 1 0B
00005AH	SDR	Serial Data Register	R/W		XXXXXXXXB
00005BH	SDCR	Communication Prescaler Control Register	R/W	Communication Prescaler	0XXX0 0 0 0B
00005CH	PWCSR	PWC Control Status Register	R/W	16-bit PWC Timer	0 0 0 0 0 0 0 0B
00005DH					0 0 0 0 0 0 0 XB
00005EH	PWCR	PWC Data Buffer Register	R/W		0 0 0 0 0 0 0 0B
00005FH					0 0 0 0 0 0 0 0B
000060H	DIVR	PWC Dividing Ratio Control Register	R/W		- - - - - - 0 0B
000061H	Prohibited				
000062H	TMCSR0	Timer Control Status Register 0	R/W	16-bit Reload Timer ch.0	0 0 0 0 0 0 0 0B
000063H					XXXX 0 0 0 0B
000064H	TMR0	16-bit Timer Register 0 Lower	R		XXXXXXXXB
	TMRLR0	16-bit Reload Register 0 Lower	W		XXXXXXXXB
000065H	TMR0	16-bit Timer Register 0 Upper	R		XXXXXXXXB
	TMRLR0	16-bit Reload Register 0 Upper	W		XXXXXXXXB

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000066H	TMCSR1	Timer Control Status Register 1	R/W	16-bit Reload Timer ch.1	0 0 0 0 0 0 0 0B
000067H					XXXX 0 0 0 0B
000068H	TMR1	16-bit Timer Register 1 Lower	R		XXXXXXXXB
	TMRLR1	16-bit Reload Register 1 Lower	W		XXXXXXXXB
000069H	TMR1	16-bit Timer Register 1 Upper	R		XXXXXXXXB
	TMRLR1	16-bit Reload Register 1 Upper	W		XXXXXXXXB
00006AH	TMCSR2	Timer Control Status Register 2	R/W	16-bit Reload Timer ch.2	0 0 0 0 0 0 0 0B
00006BH					XXXX 0 0 0 0B
00006CH	TMR2	16-bit Timer Register 2 Lower	R		XXXXXXXXB
	TMRLR2	16-bit Reload Register 2 Lower	W		XXXXXXXXB
00006DH	TMR2	16-bit Timer Register 2 Upper	R		XXXXXXXXB
	TMRLR2	16-bit Reload Register 2 Upper	W		XXXXXXXXB
00006EH	Prohibited				
00006FH	ROMM	ROM Mirror Function Selection Register	W	ROM Mirror Function Selection Module	- - - - - - 1 1B
000070H	IBSR0	I²C Bus Status Register 0	R	I²C Bus Interface ch.0	0 0 0 0 0 0 0 0B
000071H	IBCR0	I²C Bus Control Register 0	R/W		0 0 0 0 0 0 0 0B
000072H	ICCR0	I²C Bus Clock Control Register 0	R/W		XX 0 XXXXXB
000073H	IADR0	I²C Bus Address Register 0	R/W		XXXXXXXXB
000074H	IDAR0	I²C Bus Data Register 0	R/W		XXXXXXXXB
000075H	Prohibited				
000076H	IBSR1	I²C Bus Status Register 1	R	I²C Bus Interface ch.1	0 0 0 0 0 0 0 0B
000077H	IBCR1	I²C Bus Control Register 1	R/W		0 0 0 0 0 0 0 0B
000078H	ICCR1	I²C Bus Clock Control Register 1	R/W		XX 0 XXXXXB
000079H	IADR1	I²C Bus Address Register 1	R/W		XXXXXXXXB
00007AH	IDAR1	I²C Bus Data Register 1	R/W		XXXXXXXXB
00007BH	Prohibited				
00007CH	IBSR2	I²C Bus Status Register 2	R	I²C Bus Interface ch.2	0 0 0 0 0 0 0 0B
00007DH	IBCR2	I²C Bus Control Register 2	R/W		0 0 0 0 0 0 0 0B
00007EH	ICCR2	I²C Bus Clock Control Register 2	R/W		XX 0 XXXXXB
00007FH	IADR2	I²C Bus Address Register 2	R/W		XXXXXXXXB
000080H	IDAR2	I²C Bus Data Register 2	R/W		XXXXXXXXB
000081H to 000085H	Prohibited				

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000086H	TCDT	Timer Data Register Lower	R/W	16-bit Free-Run Timer	0 0 0 0 0 0 0 0B
000087H		Timer Data Register Upper	R/W		0 0 0 0 0 0 0 0B
000088H	TCCS	Timer Control Status Register Lower	R/W		0 0 0 0 0 0 0 0B
000089H		Timer Control Status Register Upper	R/W		0 - - 0 0 0 0 0B
00008AH	CPCLR	Compare Clear Register Lower	R/W		XXXXXXXXB
00008BH		Compare Clear Register Upper	R/W		XXXXXXXXB
00008CH to 00009AH	Prohibited				
00009BH	DCSR	DMA Descriptor Channel Specification Register	R/W	µDMAC	0 0 0 0 0 0 0 0B
00009CH	DSRL	DMA Status Register Lower	R/W		0 0 0 0 0 0 0 0B
00009DH	DSRH	DMA Status Register Upper	R/W		0 0 0 0 0 0 0 0B
00009EH	PACSR	Program Address Detection Control Status Register	R/W	Address Match Detection	0 0 0 0 0 0 0 0B
00009FH	DIRR	Delay Interruption Factor Generation/ Release Register	R/W	Delay Interrupt	- - - - - - - 0B
0000A0H	LPMCR	Low Power Consumption Mode Control Register	R/W	Low Power Consumption Control Circuit	0 0 0 1 1 0 0 0B
0000A1H	CKSCR	Clock Selection Register	R/W	Clock	1 1 1 1 1 1 0 0B
0000A2H	Prohibited				
0000A3H					
0000A4H	DSSR	DMA Stop Status Register	R/W	µDMAC	0 0 0 0 0 0 0 0B
0000A5H	ARSR	Automatic Ready Function Selection Register	W	External Pin	0 0 1 1- - 0 0B
0000A6H	HACR	External Address Output Control Register	W		* * * * * * * * B
0000A7H	EPCR	Bus Control Signal Selection Register	W		1 0 0 0 * 1 0 -B
0000A8H	WDTC	Watchdog Timer Control Register	R/W	Watchdog Timer	X - XXX 1 1 1B
0000A9H	TBTC	Time-base Timer Control Register	R/W	Time-base Timer	1 - - 0 0 1 0 0B
0000AAH	WTC	Watch Timer Control Register	R/W	Watch Timer	1 0 0 0 1 0 0 0B
0000ABH	Prohibited				
0000ACH	DERL	DMA Enable Register Lower	R/W	µDMAC	0 0 0 0 0 0 0 0B
0000ADH	DERH	DMA Enable Register Upper	R/W		0 0 0 0 0 0 0 0B
0000AEH	FMCS	Flash Memory Control Status Register	R/W	Flash Memory I/F	0 0 0 X 0 0 0 0B
0000AFH	Prohibited				

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000B0H	ICR00	Interrupt Control Register 00	R/W	Interrupt Controller	0 0 0 0 0 1 1 1B
0000B1H	ICR01	Interrupt Control Register 01	R/W		0 0 0 0 0 1 1 1B
0000B2H	ICR02	Interrupt Control Register 02	R/W		0 0 0 0 0 1 1 1B
0000B3H	ICR03	Interrupt Control Register 03	R/W		0 0 0 0 0 1 1 1B
0000B4H	ICR04	Interrupt Control Register 04	R/W		0 0 0 0 0 1 1 1B
0000B5H	ICR05	Interrupt Control Register 05	R/W		0 0 0 0 0 1 1 1B
0000B6H	ICR06	Interrupt Control Register 06	R/W		0 0 0 0 0 1 1 1B
0000B7H	ICR07	Interrupt Control Register 07	R/W		0 0 0 0 0 1 1 1B
0000B8H	ICR08	Interrupt Control Register 08	R/W		0 0 0 0 0 1 1 1B
0000B9H	ICR09	Interrupt Control Register 09	R/W		0 0 0 0 0 1 1 1B
0000BAH	ICR10	Interrupt Control Register 10	R/W		0 0 0 0 0 1 1 1B
0000BBH	ICR11	Interrupt Control Register 11	R/W		0 0 0 0 0 1 1 1B
0000BCH	ICR12	Interrupt Control Register 12	R/W		0 0 0 0 0 1 1 1B
0000BDH	ICR13	Interrupt Control Register 13	R/W		0 0 0 0 0 1 1 1B
0000BEH	ICR14	Interrupt Control Register 14	R/W		0 0 0 0 0 1 1 1B
0000BFH	ICR15	Interrupt Control Register 15	R/W		0 0 0 0 0 1 1 1B
0000C0H	HCNT0	Host Control Register 0	R/W	USB HOST	0 0 0 0 0 0 0 0B
0000C1H	HCNT1	Host Control Register 1	R/W		0 0 0 0 0 0 0 1B
0000C2H	HIRQ	Host Interruption Register	R/W		0 0 0 0 0 0 0 0B
0000C3H	HERR	Host Error Status Register	R/W		0 0 0 0 0 0 1 1B
0000C4H	HSTATE	Host State Status Register	R/W		XX 0 1 0 0 1 0B
0000C5H	HFCOMP	SOF Interrupt FRAME Compare Register	R/W		0 0 0 0 0 0 0 0B
0000C6H	HRTIMER	Retry Timer Setting Register	R/W		0 0 0 0 0 0 0 0B
0000C7H			R/W		0 0 0 0 0 0 0 0B
0000C8H			R/W		XXXXXX 0 0B
0000C9H	HADR	Host Address Register	R/W		X 0 0 0 0 0 0 0B
0000CAH	HEOF	EOF Setting Register	R/W		0 0 0 0 0 0 0 0B
0000CBH			R/W		XX 0 0 0 0 0 0B
0000CCH	HFRAME	FRAME Setting Register	R/W		0 0 0 0 0 0 0 0B
0000CDH			R/W		XXXXX 0 0 0B
0000CEH	HTOKEN	Host Token End Point Register	R/W		0 0 0 0 0 0 0 0B
0000CFH	Prohibited				
0000D0H	UDCC	UDC Control Register	R/W	USB Function	1 0 1 0 0 0 0 0B
0000D1H			R/W		0 0 0 0 0 0 0 0B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000D2H	EP0C	EP0 Control Register	R/W	USB Function	0 1 0 0 0 0 0 0B
0000D3H			R/W		XXXX 0 0 0 0B
0000D4H	EP1C	EP1 Control Register	R/W		0 0 0 0 0 0 0 0B
0000D5H			R/W		0 1 1 0 0 0 0 1B
0000D6H	EP2C	EP2 Control Register	R/W		0 1 0 0 0 0 0 0B
0000D7H			R/W		0 1 1 0 0 0 0 0B
0000D8H	EP3C	EP3 Control Register	R/W		0 1 0 0 0 0 0 0B
0000D9H			R/W		0 1 1 0 0 0 0 0B
0000DAH	EP4C	EP4 Control Register	R/W		0 1 0 0 0 0 0 0B
0000DBH			R/W		0 1 1 0 0 0 0 0B
0000DCH	EP5C	EP5 Control Register	R/W		0 1 0 0 0 0 0 0B
0000DDH			R/W		0 1 1 0 0 0 0 0B
0000DEH	TMSP	Time Stamp Register	R		0 0 0 0 0 0 0 0B
0000DFH			R		XXXXX0 0 0B
0000E0H	UDCS	UDC Status Register	R/W		XX0 0 0 0 0 0B
0000E1H	UDCIE	UDC Interrupt Enable Register	R/W, R		0 0 0 0 0 0 0 0B
0000E2H	EP0IS	EP0I Status Register	R/W		XXXXXXXXB
0000E3H			R/W		1 0 XXX 1 XXB
0000E4H	EP0OS	EP0O Status Register	R/W, R		0 XXXXXXXB
0000E5H			R/W		1 0 0 XX 0 0 0B
0000E6H	EP1S	EP1 Status Register	R		XXXXXXXXB
0000E7H			R/W, R		1 0 0 0 0 0 0 XB
0000E8H	EP2S	EP2 Status Register	R		XXXXXXXXB
0000E9H			R/W, R		1 0 0 0 0 0 0 0B
0000EAH	EP3S	EP3 Status Register	R		XXXXXXXXB
0000EBH			R/W, R		1 0 0 0 0 0 0 0B
0000ECH	EP4S	EP4 Status Register	R		XXXXXXXXB
0000EDH			R/W, R		1 0 0 0 0 0 0 0B
0000EEH	EP5S	EP5 Status Register	R		XXXXXXXXB
0000EFH			R/W, R		1 0 0 0 0 0 0 0B
0000F0H	EP0DT	EP0 Data Register	R/W		XXXXXXXXB
0000F1H			R/W		XXXXXXXXB
0000F2H	EP1DT	EP1 Data Register	R/W		XXXXXXXXB
0000F3H			R/W		XXXXXXXXB
0000F4H	EP2DT	EP2 Data Register	R/W		XXXXXXXXB
0000F5H			R/W		XXXXXXXXB
0000F6H	EP3DT	EP3 Data Register	R/W		XXXXXXXXB
0000F7H			R/W		XXXXXXXXB

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000F8H	EP4DT	EP4 Data Register	R/W	USB Function	XXXXXXXXB
0000F9H			R/W		XXXXXXXXB
0000FAH	EP5DT	EP5 Data Register	R/W		XXXXXXXXB
0000FBH			R/W		XXXXXXXXB
0000FCH to 0000FFH	Prohibited				
000100H to #H	RAM Area				
001FF0H	PADR0	Program Address Detection Register ch.0 Lower	R/W	Address Match Detection	XXXXXXXXB
001FF1H		Program Address Detection Register ch.0 Middle	R/W		XXXXXXXXB
001FF2H		Program Address Detection Register ch.0 Upper	R/W		XXXXXXXXB
001FF3H	PADR1	Program Address Detection Register ch.1 Lower	R/W		XXXXXXXXB
001FF4H		Program Address Detection Register ch.1 Middle	R/W		XXXXXXXXB
001FF5H		Program Address Detection Register ch.1 Upper	R/W		XXXXXXXXB
#H to 0078FFH	Unused Area				
007900H	PRLL0	PPG Reload Register Lower ch.0	R/W	PPG ch.0	XXXXXXXXB
007901H	PRLH0	PPG Reload Register Upper ch.0	R/W		XXXXXXXXB
007902H	PRLL1	PPG Reload Register Lower ch.1	R/W	PPG ch.1	XXXXXXXXB
007903H	PRLH1	PPG Reload Register Upper ch.1	R/W		XXXXXXXXB
007904H	PRLL2	PPG Reload Register Lower ch.2	R/W	PPG ch.2	XXXXXXXXB
007905H	PRLH2	PPG Reload Register Upper ch.2	R/W		XXXXXXXXB
007906H	PRLL3	PPG Reload Register Lower ch.3	R/W	PPG ch.3	XXXXXXXXB
007907H	PRLH3	PPG Reload Register Upper ch.3	R/W		XXXXXXXXB
007908H	PRLL4	PPG Reload Register Lower ch.4	R/W	PPG ch.4	XXXXXXXXB
007909H	PRLH4	PPG Reload Register Upper ch.4	R/W		XXXXXXXXB
00790AH	PRLL5	PPG Reload Register Lower ch.5	R/W	PPG ch.5	XXXXXXXXB
00790BH	PRLH5	PPG Reload Register Upper ch.5	R/W		XXXXXXXXB
00790CH to 00790FH	Prohibited				

(Continued)

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
007910H	IPCP0	Input Capture Data Register Lower ch.0	R	Input Capture ch.0/ch.1	XXXXXXXXB
007911H		Input Capture Data Register Upper ch.0	R		XXXXXXXXB
007912H	IPCP1	Input Capture Data Register Lower ch.1	R		XXXXXXXXB
007913H		Input Capture Data Register Upper ch.1	R		XXXXXXXXB
007914H	IPCP2	Input Capture Data Register Lower ch.2	R	Input Capture ch.2/ch.3	XXXXXXXXB
007915H		Input Capture Data Register Upper ch.2	R		XXXXXXXXB
007916H	IPCP3	Input Capture Data Register Lower ch.3	R		XXXXXXXXB
007917H		Input Capture Data Register Upper ch.3	R		XXXXXXXXB
007918H	OCCP0	Output Compare Register Lower ch.0	R/W	Output Compare ch.0/ch.1	XXXXXXXXB
007919H		Output Compare Register Upper ch.0	R/W		XXXXXXXXB
00791AH	OCCP1	Output Compare Register Lower ch.1	R/W		XXXXXXXXB
00791BH		Output Compare Register Upper ch.1	R/W		XXXXXXXXB
00791CH	OCCP2	Output Compare Register Lower ch.2	R/W	Output Compare ch.2/ch.3	XXXXXXXXB
00791DH		Output Compare Register Upper ch.2	R/W		XXXXXXXXB
00791EH	OCCP3	Output Compare Register Lower ch.3	R/W		XXXXXXXXB
00791FH		Output Compare Register Upper ch.3	R/W		XXXXXXXXB
007920H	DBAPL	DMA Buffer Address Pointer Lower 8-bit	R/W	μDMAC	XXXXXXXXB
007921H	DBAPM	DMA Buffer Address Pointer Middle 8-bit	R/W		XXXXXXXXB
007922H	DBAPH	DMA Buffer Address Pointer Upper 8-bit	R/W		XXXXXXXXB
007923H	DMACS	DMA Control Register	R/W		XXXXXXXXB
007924H	DIOAL	DMA I/O Register Address Pointer Lower 8-bit	R/W		XXXXXXXXB
007925H	DIOAH	DMA I/O Register Address Pointer Upper 8-bit	R/W		XXXXXXXXB
007926H	DDCTL	DMA Data Counter Lower 8-bit	R/W		XXXXXXXXB
007927H	DDCTH	DMA Data Counter Upper 8-bit	R/W		XXXXXXXXB
007928H to 007FFFH	Prohibited				

- Explanation on read/write
  R/W : Readable / Writable
  R : Read only
  W : Write only

- Explanation on initial values
  0 : Initial value is “0”.
  1 : Initial value is “1”.
  X : Initial value is undefined.
  - : Initial value is undefined (None) .
  * : Initial value of this bit is “1” or “0”.

Note : No I/O instruction can be used for registers located between 007900H and 007FFFH.

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS support	μDMAC	Interrupt vector			Interrupt control register		Priority
			Number*1		Address	ICR	Address	
Reset	×	×	#08	08H	FFFFDCH	—	—	High
INT 9 instruction	×	×	#09	09H	FFFFD8H	—	—	
Exceptional treatment	×	×	#10	0AH	FFFFD4H	—	—	
USB Function1	×	0, 1	#11	0BH	FFFFD0H	ICR00	0000B0H	
USB Function2	×	2 to 6*2	#12	0CH	FFFFCCH			
USB Function3	×	×	#13	0DH	FFFFC8H	ICR01	0000B1H	
USB Function4	×	×	#14	0EH	FFFFC4H			
USB HOST1	×	×	#15	0FH	FFFFC0H	ICR02	0000B2H	
USB HOST2	×	×	#16	10H	FFFFBCH			
I²C ch.0	×	×	#17	11H	FFFFB8H	ICR03	0000B3H	
DTP/External interrupt ch.0/ch.1	○	×	#18	12H	FFFFB4H			
I²C ch.1	×	×	#19	13H	FFFFB0H	ICR04	0000B4H	
DTP/External interrupt ch.2/ch.3	○	×	#20	14H	FFFFACH			
I²C ch.2	×	×	#21	15H	FFFFA8H	ICR05	0000B5H	
DTP/External interrupt ch.4/ch.5	○	×	#22	16H	FFFFA4H			
PWC/Reload timer ch.0	△	14	#23	17H	FFFFA0H	ICR06	0000B6H	
DTP/External interrupt ch.6/ch.7	△	×	#24	18H	FFFF9CH			
Input capture ch.0/ch.1	△	7	#25	19H	FFFF98H	ICR07	0000B7H	
Reload timer ch.1	△	×	#26	1AH	FFFF94H			
Input capture ch.2/ch.3	△	8	#27	1BH	FFFF90H	ICR08	0000B8H	
Reload timer ch.2	△	×	#28	1CH	FFFF8CH			
Output compare ch.0/ch.1	○	×	#29	1DH	FFFF88H	ICR09	0000B9H	
PPG ch.0/ch.1	×	×	#30	1EH	FFFF84H			
Output compare ch.2/ch.3	○	×	#31	1FH	FFFF80H	ICR10	0000BAH	
PPG ch.2/ch.3	×	×	#32	20H	FFFF7CH			
UART (Send completed) ch.2/ch.3	○	11	#33	21H	FFFF78H	ICR11	0000BBH	
PPG ch.4/ch.5	×	×	#34	22H	FFFF74H			
UART (Reception completed) ch.2/ch.3	◎	10	#35	23H	FFFF70H	ICR12	0000BCH	
A/D converter/Free-run timer	△	15	#36	24H	FFFF6CH			
UART (Send completed) ch.0/ch.1	○	13	#37	25H	FFFF68H	ICR13	0000BDH	
Extended serial I/O	×	9	#38	26H	FFFF64H			
UART (Reception completed) ch.0/ch.1	◎	12	#39	27H	FFFF60H	ICR14	0000BEH	
Time-base timer/Watch timer	×	×	#40	28H	FFFF5CH			
Flash memory status	×	×	#41	29H	FFFF58H	ICR15	0000BFH	
Delay interrupt output module	×	×	#42	2AH	FFFF54H			Low

(Continued)

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◎ : Available, EI²OS stop function provided (The interrupt request flag is cleared by the interrupt clear signal. With a stop request).

○ : Available (The interrupt request flag is cleared by the interrupt clear signal.)

△ : Available when any interrupt source sharing ICR is not used.

× : Unavailable

*1 : If the same level interrupt is output simultaneously, the lower interrupt factor of interrupt vector number has priority.

*2 : ch.2 and 3 can also be used during USB HOST operation.

Notes :
- If the same interrupt control register (ICR) has two interrupt factors and the use of the EI²OS is permitted, the EI²OS is activated when either of the factors is detected. As any interrupt other than the activation factor is masked while the EI²OS is running, it is recommended that you should mask either of the interrupt requests when using the EI²OS.
- The interrupt flag is cleared by the EI²OS interrupt clear signal for the resource that has two interrupt factors in the same interrupt control register (ICR).
- If a resource has two interrupt sources for the same interrupt number, both of the interrupt request flags are cleared by the μDMAC interrupt clear signal. Therefore, when you use either of two interrupt factors for the DMAC function, another interrupt function is disabled. Set the interrupt request permission bit to “0” in the appropriate resource, and take measures by software polling.

• Content of USB interruption factor

USB interrupt factor	Details
USB function 1	End Point0-IN End Point0-OUT
USB function 2	End Point1-5 *
USB function 3	SUSP SOF BRST WKUP CONF
USB function 4	SPK
USB HOST1	DIRQ CNNIRQ URIRQ RWKIRQ
USB HOST2	SOFIRQ CMPIRQ

* : Endpoints 1 and 2 can also be used during USB HOST operation.

■ USB

1. USB Function

The USB function is an interface supporting the USB (Universal Serial Bus) communications protocol.

• Feature of USB function
  • Correspond to USB Full Speed
  • Full speed (12 Mbps) is supported.
  • The device status is auto-answer.
  • Bit stripping, bit stuffing, and automatic generation and check of CRC5 and CRC16
  • Toggle check by data synchronization bit
  • Automatic response to all standard commands except Get/SetDescriptor and SynchFrame commands (these 3 commands can be processed the same way as the class vendor commands).
  • The class vendor commands can be received as data and responded via firmware.
  • Supports up to 6 EndPoints (EndPoint0 is fixed to control transfer)
  • 2 transfer data buffers integrated for each end point (one IN buffer and one OUT buffer for EndPoint 0)
  • Supports automatic transfer mode for transfer data via DMA (except buffers for EndPoint 0)

2. USB HOST

USB HOST provides the minimal host operations required and is a function that enables data to be transferred to and from a device without PC intervention.

• Feature of USB HOST
  • Automatic detection of Low Speed/Full Speed transfer
  • Low Speed/Full Speed transfer support
  • Automatic detection of connection and cutting device
  • Reset sending function support to USB-bus
  • Support of IN/OUT/SETUP/SOF token
  • In-token handshake packet automatic transmission (excluding STALL)
  • Out-token handshake packet automatic detection
  • Supports a maximum packet length of 256 bytes.
  • Error (CRC error/toggle error/time-out) various supports
  • Wake-Up function support

• Restrictions of USB HOST

		USB HOST
HUB support		○*
Transfer	Bulk transfer	○
	Control transfer	○
	Interrupt transfer	○
	Isochronous transfer	×
Transfer speed	Low Speed	○
	Full Speed	○
PRE packet support		×
SOF packet support		○
Error	CRC error	○
	Toggle error	○
	Time-out	○
	Maximum packet < receive data	○
Detection of connection and cutting of device		○
Transfer speed detection		○

○ : Supported
× : Not supported

* : It corresponds to Full Speed only, and the HUB supports up to one step.

■ SECTOR CONFIGURATION OF FLASH MEMORY

• Sector configuration of 3Mbit flash memory

3 Mbits flash memory is located in $F9_H$ to FF_H bank on the CPU memory map.

Flash Memory	CPU address	Writer address *
Prohibited	F80000H F8FFFFH	00000H 0FFFFH
SA0 (64 Kbytes)	F90000H F9FFFFH	10000H 1FFFFH
SA1 (64 Kbytes)	FA0000H FAFFFFH	20000H 2FFFFH
SA2 (64 Kbytes)	FB0000H FBFFFFH	30000H 3FFFFH
Prohibited	FC0000H FCFFFFH	40000H 4FFFFH
SA3 (64 Kbytes)	FD0000H FDFFFFH	50000H 5FFFFH
SA4 (64 Kbytes)	FE0000H FEFFFFH	60000H 6FFFFH
SA5 (32 Kbytes)	FF0000H FF7FFFH	70000H 77FFFH
SA6 (8 Kbytes)	FF8000H FF9FFFH	78000H 79FFFH
SA7 (8 Kbytes)	FFA000H FFBFFFH	7A000H 7BFFFH
SA8 (16 Kbytes)	FFC000H FFFFFFH	7C000H 7FFFFH

* : The writer address is relative to the CPU address when data is programmed into flash memory by a parallel programmer. Programming and erasing by the general-purpose parallel programmer are executed based on writer addresses.

- Sector configuration of 4Mbit flash memory

4 Mbits flash memory is located in $F8_H$ to FF_H bank on the CPU memory map.

Flash Memory	CPU address	Writer address *
SA0 (64 Kbytes)	F80000H F8FFFFH	00000H 0FFFFH
SA1 (64 Kbytes)	F90000H F9FFFFH	10000H 1FFFFH
SA2 (64 Kbytes)	FA0000H FAFFFFH	20000H 2FFFFH
SA3 (32 Kbytes)	FB0000H FB7FFFH	30000H 37FFFH
SA4 (8 Kbytes)	FB8000H FB9FFFH	38000H 39FFFH
SA5 (8 Kbytes)	FBA000H FBBFFFH	3A000H 3BFFFH
SA6 (16 Kbytes)	FBC000H FBFFFFH	3C000H 3FFFFH
SA7 (64 Kbytes)	FC0000 FCFFFF	40000H 4FFFFH
SA8 (64 Kbytes)	FD0000 FDFFFF	50000H 5FFFFH
SA9 (64 Kbytes)	FE0000H FEFFFFH	60000H 6FFFFH
SA10 (32 Kbytes)	FF0000H FF7FFFH	70000H 77FFFH
SA11 (8 Kbytes)	FF8000H FF9FFFH	78000H 79FFFH
SA12 (8 Kbytes)	FFA000H FFBFFFH	7A000H 7BFFFH
SA13 (16 Kbytes)	FFC000H FFFFFFH	7C000H 7FFFFH

* : The writer address is relative to the CPU address when data is programmed into flash memory by a parallel programmer. Programming and erasing by the general-purpose parallel programmer are executed based on writer addresses.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	$V_{CC} \geq AV_{CC}$*2
	AVRH	V_{SS} – 0.3	V_{SS} + 4.0	V	$AV_{CC} \geq AVR \geq 0$ V*3
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*4
		V_{SS} – 0.3	V_{SS} + 6.0	V	N-ch open-drain (Withstand voltage of 5 V I/O)*5
		– 0.5	V_{SS} + 4.5	V	USB I/O
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*4
		– 0.5	V_{SS} + 4.5	V	USB I/O
Maximum clamp current	I_{CLAMP}	– 2.0	+2.0	mA	*6
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*6
“L” level maximum output current	I_{OL1}	—	10	mA	Other than USB I/O*7
	I_{OL2}	—	43	mA	USB I/O*7
“L” level average output current	I_{OLAV1}	—	4	mA	*8
	I_{OLAV2}	—	15/4.5	mA	USB-IO (Full speed/ Low speed) *8
“L” level maximum total output current	ΣI_{OL}	—	100	mA	
“L” level average total output current	ΣI_{OLAV}	—	50	mA	*9
“H” level maximum output current	I_{OH1}	—	– 10	mA	Other than USB I/O*7
	I_{OH2}	—	– 43	mA	USB I/O*7
“H” level average output current	I_{OHAV1}	—	– 4	mA	*8
	I_{OHAV2}	—	–15/–4.5	mA	USB-IO (Full speed/ Low speed) *8
“H” level maximum total output current	ΣI_{OH}	—	– 100	mA	
“H” level average total output current	ΣI_{OHAV}	—	– 50	mA	*9
Power consumption	Pd	—	340	mW	
Operating temperature	T_A	– 40	+ 85	°C	
Storage temperature	Tstg	– 55	+ 150	°C	
		– 55	+ 125	°C	USB I/O

*1 : The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2 : Be careful not to let AV_{CC} exceed V_{CC}, for example, when the power is turned on.

*3 : Be careful not to let AVRH exceed AVcc.

*4 : V_I and V_O must not exceed Vcc + 0.3 V. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*5 : Applicable to pins : P60 to P67, P96, PA0 to PA7, PB0 to PB4, UTEST

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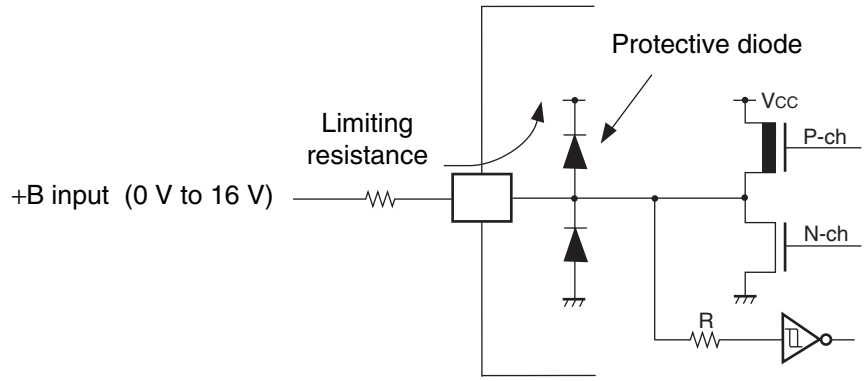
*6 : • Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, P90 to P95, PB5, PB6

- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than P60 to P67, P96, PA0 to PA7, PB0 to PB4, DVP, DVM, HVP, HVM, UTEST, $\overline{\text{HCON}}$
- Sample recommended circuits:

• Input/output equivalent circuits



*7 : A peak value of an applicable one pin is specified as a maximum output current.

*8 : The average output current specifies the mean value of the current flowing in the relevant single pin during a period of 100 ms.

*9 : The average total output current specifies the mean value of the currents flowing in all of the relevant pins during a period of 100 ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	3.0	3.6	V	At normal operation (when using USB)
		2.7	3.6	V	At normal operation (when not using USB)
		1.8	3.6	V	Hold state of stop operation
Input “H” voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	CMOS input pin
	V_{IHS1}	0.8 V_{CC}	V_{CC} + 0.3	V	CMOS hysteresis input pin
	V_{IHS2}	0.8 V_{CC}	V_{SS} + 5.3	V	N-ch open-drain (Withstand voltage of 5 V I/O)*
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD pin input
	V_{IHUSB}	2.0	V_{CC} + 0.3	V	USB pin input
Input “L” voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	CMOS input pin
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	CMOS hysteresis input pin
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD pin input
	V_{ILUSB}	V_{SS}	0.8	V	USB pin input
Differential input sensitivity	V_{DI}	0.2	—	V	USB pin input
Differential common mode input voltage range	V_{CM}	0.8	2.5	V	USB pin input
Operating temperature	T_A	– 40	+ 85	°C	When not using USB
		0	+ 70	°C	When using USB, at external bus operation

* : Applicable to pins : P60 to P67, P96, PA0 to PA7, PB0 to PB4, UTEST

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output "H" voltage	V_{OH}	Output pins other than P60 to P67, P96, PA0 to PA7, PB0 to PB4, HVP, HVM, DVP, DVM	I_{OH} = – 4.0 mA	V_{CC} – 0.5	—	Vcc	V	
		HVP, HVM, DVP, DVM	R_L = 15 kΩ ± 5%	2.8	—	3.6	V	
Output "L" voltage	V_{OL}	Output pins other than HVP, HVM, DVP, DVM	I_{OL} = 4.0 mA	Vss	—	Vss + 0.4	V	
		HVP, HVM, DVP, DVM	R_L = 1.5 kΩ ± 5%	0	—	0.3	V	
Input leak current	I_{IL}	Output pins other than P60 to P67, P96, PA0 to PA7, PB0 to PB4, HVP, HVM, DVP, DVM	V_{CC} = 3.3 V, Vss < V_I < V_{CC}	– 10	—	+ 10	µA	
		HVP, HVM, DVP, DVM	—	– 5	—	+ 5	µA	
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17	V_{CC} = 3.3 V, T_A = + 25 °C	25	50	100	kΩ	
Open drain output current	I_{LIOD}	P60 to P67, P96, PA0 to PA7, PB0 to PB4	—	—	0.1	10	µA	
Power supply current	I_{CC}	V_{CC}	V_{CC} = 3.3 V, Internal frequency 24 MHz, At normal operating	—	75	85	mA	MB90F334A MB90F335A
			At USB operating (USTP = 0)	—	65	75	mA	MB90333A
			V_{CC} = 3.3 V, Internal frequency 24 MHz, At normal operating	—	70	80	mA	MB90F334A MB90F335A
			At non-operating USB (USTP = 1)	—	60	70	mA	MB90333A
	I_{CCS}		V_{CC} = 3.3 V, Internal frequency 24 MHz, At sleep mode	—	27	40	mA	
	I_{CTS}		V_{CC} = 3.3 V, Internal frequency 24 MHz, At timer mode	—	3.5	10	mA	
			V_{CC} = 3.3 V, Internal frequency 3 MHz, At timer mode	—	1	2	mA	
	I_{CCL}		V_{CC} = 3.3 V, Internal frequency 8 kHz, At sub clock operation, (T_A = +25 °C)	—	25	150	µA	

(Continued)

(Continued)

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCLS}	V_{CC}	V_{CC} = 3.3 V, Internal frequency 8 kHz, At sub clock, At sleep operating, (T_A = + 25 °C)	—	10	50	µA	
	I_{CCT}		V_{CC} = 3.3 V, Internal frequency 8 kHz, Watch mode, (T_A = + 25 °C)	—	1.5	40	µA	
	I_{CCH}		T_A = + 25 °C, At stop	—	1	40	µA	
Input capacitance	C_{IN}	Other than AVcc, AVss, Vcc, Vss	—	—	5	15	pF	
Pull-up resistor	R_{up}	$\overline{RST}$	—	25	50	100	kΩ	
USB I/O output impedance	Z_{USB}	DVP, DVM HVP, HVM	—	3	—	14	Ω	

Note : P60 to P67, P96, PA0 to PA7, and PB0 to PB4 are N-ch open-drain pins usually used as CMOS.

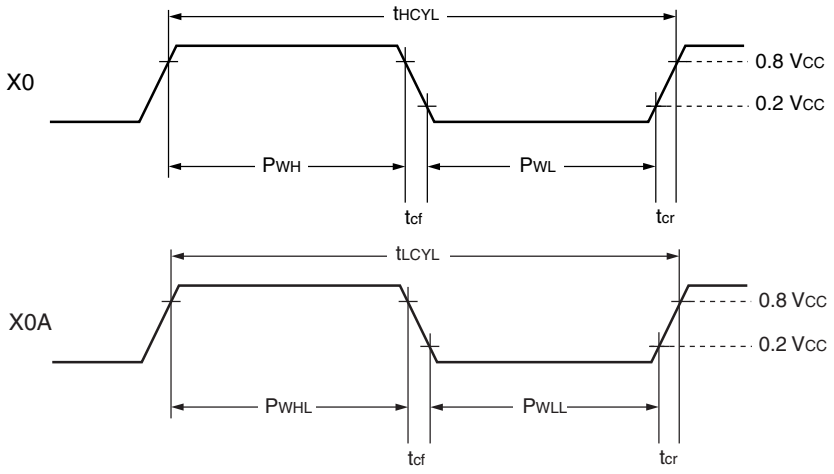
4. AC Characteristics

(1)Clock input timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

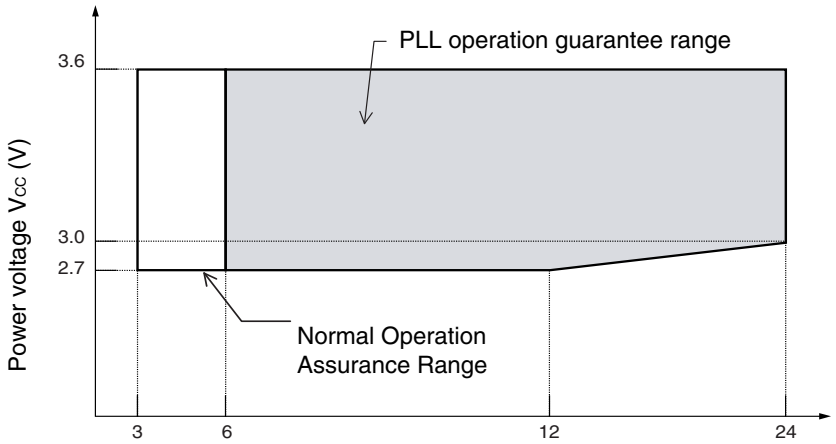
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CH}	X0, X1	—	6	—	MHz	When oscillator is used
			6	—	24	MHz	External clock input
	f_{CL}	X0A, X1A	—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1	—	166.7	—	ns	When oscillator is used
			166.7	—	41.7	ns	External clock input
	t_{LCYL}	X0A, X1A	—	30.5	—	s	
Input clock pulse width	P_{WH} P_{WL}	X0	10	—	—	ns	A reference duty ratio is 30% to 70%.
	P_{WHL} P_{WLL}	X0A	—	15.2	—	s	
Input clock rise time and fall time	tcr tcf	X0	—	—	5	ns	At external clock
Internal operating clock frequency	f_{CP}	—	3	—	24	MHz	When main clock is used
	f_{CPL}	—	—	8.192	—	kHz	When sub clock is used
Internal operating clock cycle time	t_{CP}	—	42	—	333	ns	When main clock is used
	t_{CPL}	—	—	122.1	—	s	When sub clock is used

• Clock Timing



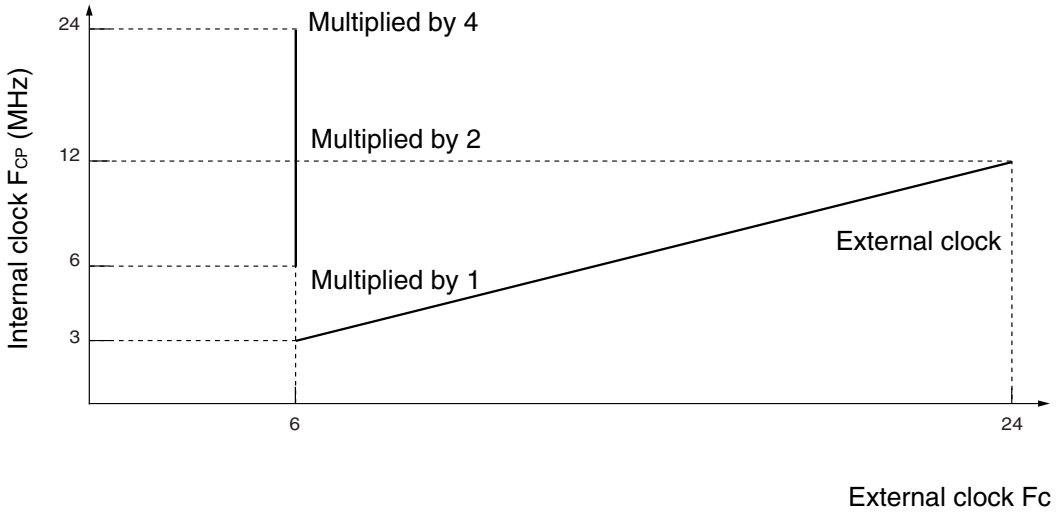
• PLL operation guarantee range

Relation between power supply voltage and internal operation clock frequency



Note : When the USB is used, operation is guaranteed at voltages between 3.0 V and 3.6 V.

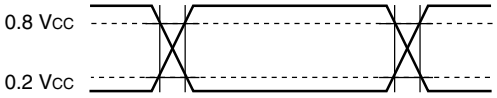
Relation between internal operation clock frequency and external clock frequency



The AC standards assume the following measurement reference voltages.

- Input signal waveform

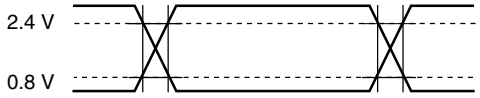
Hysteresis input pin



Hysteresis input/other than MD input pin

- Output signal waveform

Output pin

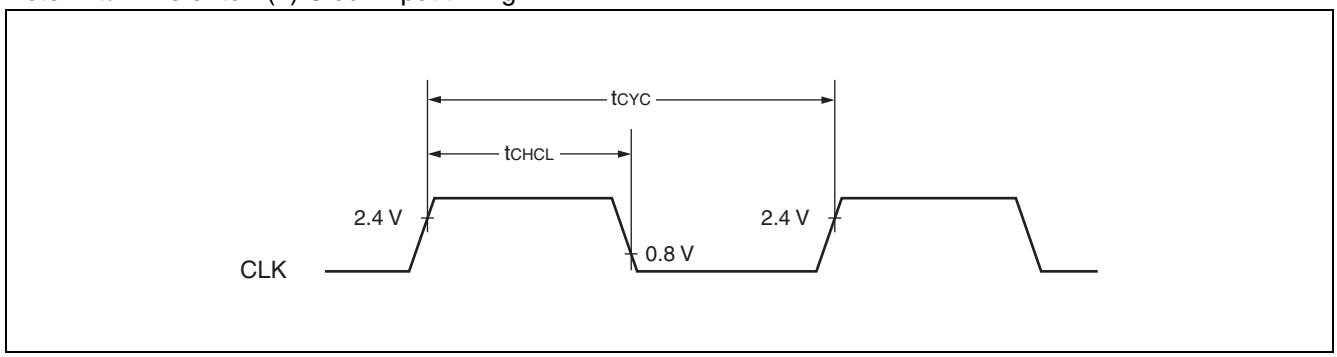


(2)Clock output timing

(V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	
CLK↑→CLK↓	t_{CHCL}	CLK	V_{CC} = 3.0 V to 3.6 V	$t_{CP}/2$ – 15	$t_{CP}/2$ + 15	ns	At f_{cp} = 24 MHz
				$t_{CP}/2$ – 20	$t_{CP}/2$ + 20	ns	At f_{cp} = 12 MHz
				$t_{CP}/2$ – 64	$t_{CP}/2$ + 64	ns	At f_{cp} = 6 MHz

Note : t_{CP} : Refer to “ (1) Clock input timing”.



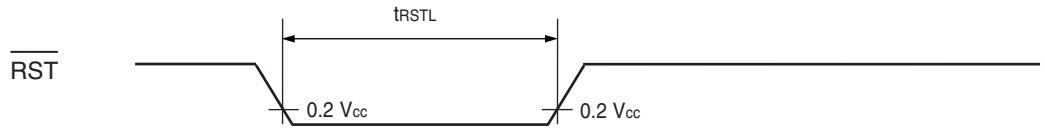
(3) Reset

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

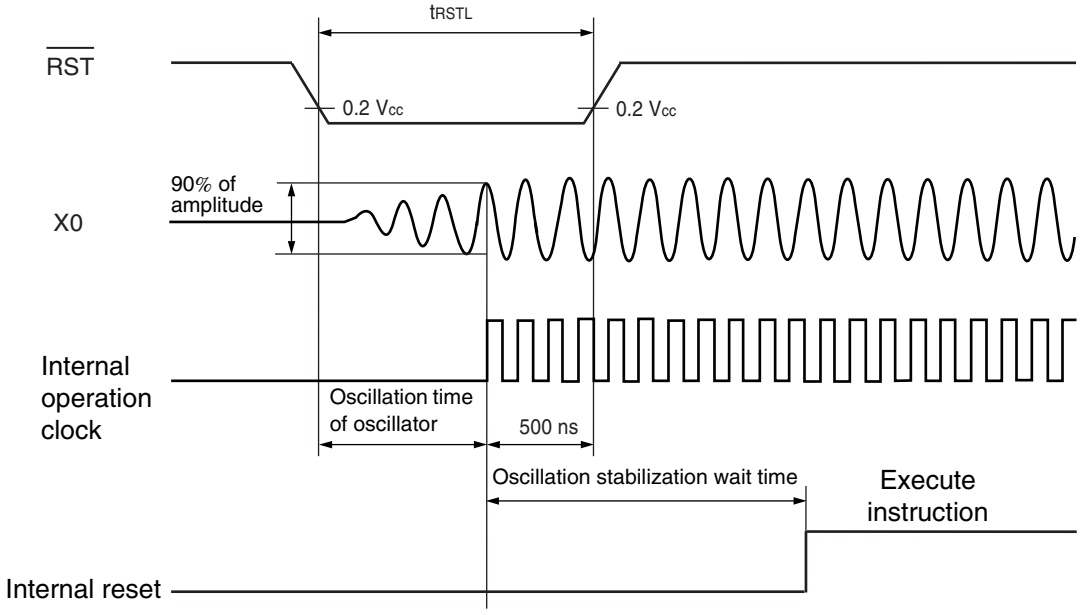
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	500	—	ns	At normal operating, At time base timer mode, At main sleep mode, At PLL sleep mode
				Oscillation time of oscillator* + 500 ns	—	µs	At stop mode, At sub clock mode, At sub sleep mode, At watch mode

* : Oscillation time of oscillator is the time that the amplitude reaches 90%. It takes several milliseconds to several dozens of milliseconds on a crystal oscillator, several hundreds of microseconds to several milliseconds on a ceramic oscillator, and 0 milliseconds on an external clock.

• During normal operation, time-base timer mode, main sleep mode and PLL sleep mode



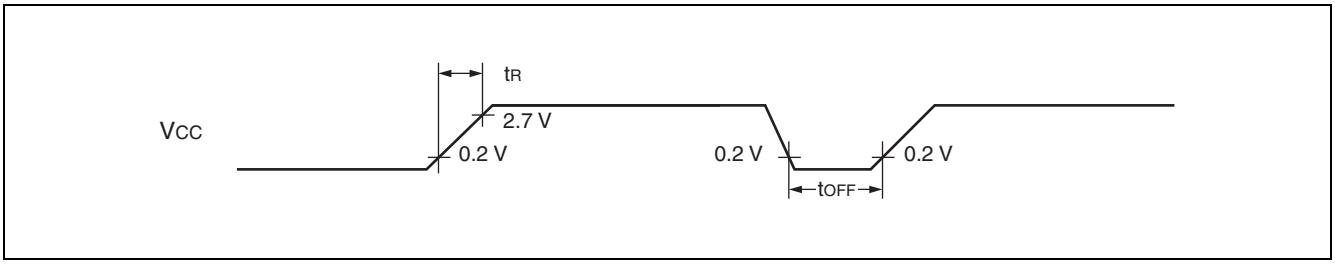
• During stop mode, sub clock mode, sub-sleep mode and watch mode



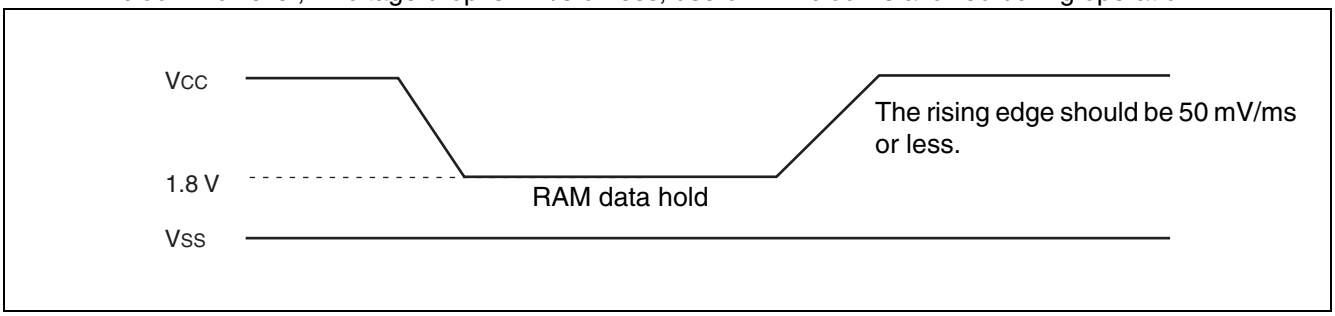
(4) Power-on reset

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	V_{CC}	—	0.05	30	ms	
Power supply shutdown time	t_{OFF}	V_{CC}		1	—	ms	Waiting time until power-on



Notes :
- V_{CC} must be lower than 0.2 V before the power supply is turned on.
- The above standard is a value for performing a power-on reset.
- In the device, there are internal registers which is initialized only by a power-on reset. When the initialization of these items is expected, turn on the power supply according to the standards.
- Sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during operation as illustrated below, voltage fluctuation should be minimized so that the voltage rises as smoothly as possible. When raising the power, do not use PLL clock. However, if voltage drop is 1 V/s or less, use of PLL clock is allowed during operation.



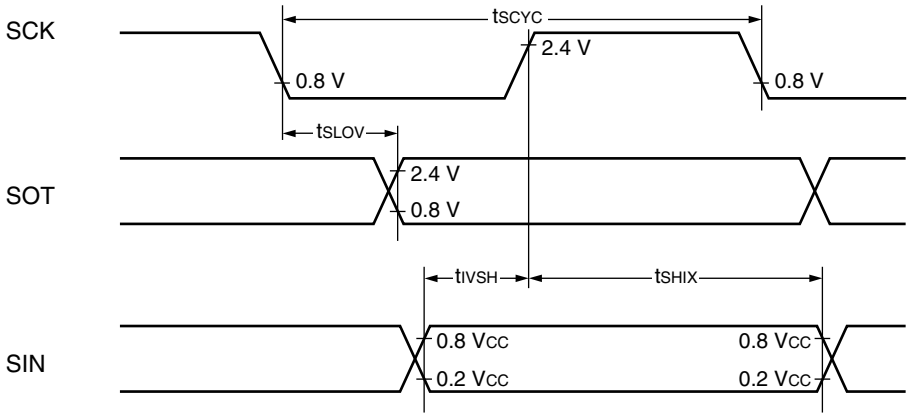
(5) UART0, UART1, UART2, UART3 I/O extended serial timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

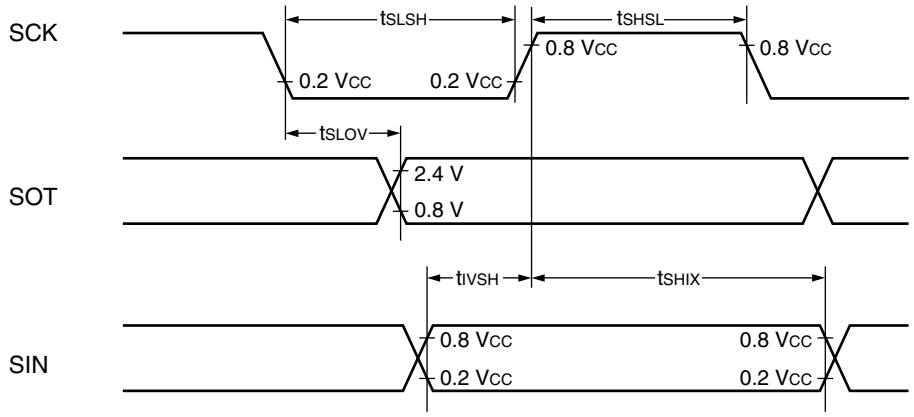
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock mode output pin is : C_L = 80 pF + 1TTL	8 t_{CP}	—	ns
SCK↓→SOT delay time	t_{SLOV}	SCKx, SOTx		– 80	+ 80	ns
Valid SIN→SCK↑	t_{IVSH}	SCKx, SINx		100	—	ns
SCK↑→valid SIN hold time	t_{SHIX}	SCKx, SINx		60	—	ns
Serial clock H pulse width	t_{SHSL}	SCKx, SINx	External shift clock mode output pin is : C_L = 80 pF + 1TTL	4 t_{CP}	—	ns
Serial clock L pulse width	t_{SLSH}	SCKx, SINx		4 t_{CP}	—	ns
SCK↓→SOT delay time	t_{SLOV}	SCKx, SOTx		—	150	ns
Valid SIN→SCK↑	t_{IVSH}	SCKx, SINx		60	—	ns
SCK↑→valid SIN hold time	t_{SHIX}	SCKx, SINx		60	—	ns

Notes : • Above rating is the case of CLK synchronous mode.
• C_L is a load capacitance value on pins for testing.
• t_{CP} : Refer to “ (1) Clock input timing”.

• Internal shift clock mode



• External shift clock mode



(6) I²C timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCL clock frequency	f_{SCL}	Power-supply voltage of external pull-up resistor at 5.0 V. R = 1.2 kΩ, C = 50 pF*2 Power-supply voltage of external pull-up resistor at 3.6 V. R = 1.0 kΩ, C = 50 pF*2	0	100	kHz
(Repeat) [start] condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	µs
SCL clock "L" width	t_{LOW}		4.7	—	µs
SCL clock "H" width	t_{HIGH}		4.0	—	µs
Repeat [start] condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	Power-supply voltage of external pull-up resistor at 5.0 V. f_{CP}*1 ≤ 20 MHz, R = 1.2 kΩ, C = 50 pF*2 Power-supply voltage of external pull-up resistor at 3.6 V. f_{CP}*1 ≤ 20 MHz, R = 1.0 kΩ, C = 50 pF*2	250*4	—	ns
		Power-supply voltage of external pull-up resistor at 5.0 V. f_{CP}*1 > 20 MHz, R = 1.2 kΩ, C = 50 pF*2 Power-supply voltage of external pull-up resistor at 3.6 V. f_{CP}*1 > 20 MHz, R = 1.0 kΩ, C = 50 pF*2	200*4	—	
[Stop] condition setup time SCL ↑ → SDA ↑	t_{SUSTO}	Power-supply voltage of external pull-up resistor at 5.0 V. R = 1.2 kΩ, C = 50 pF*2 Power-supply voltage of external pull-up resistor at 3.6 V. R = 1.0 kΩ, C = 50 pF*2	4.0	—	µs
Bus free time between [stop] condition and [start] condition	t_{BUS}		4.7	—	µs

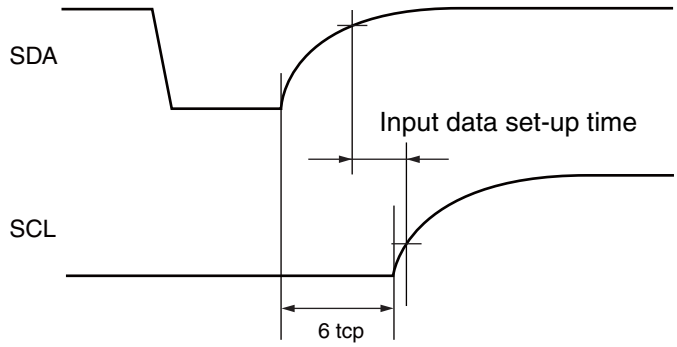
*1 : f_{CP} is internal operating clock frequency. Refer to " (1) Clock input timing".

*2 : R and C are pull-up resistance of SCL and SDA lines and load capacitance.

*3 : The maximum t_{HDDAT} only has to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

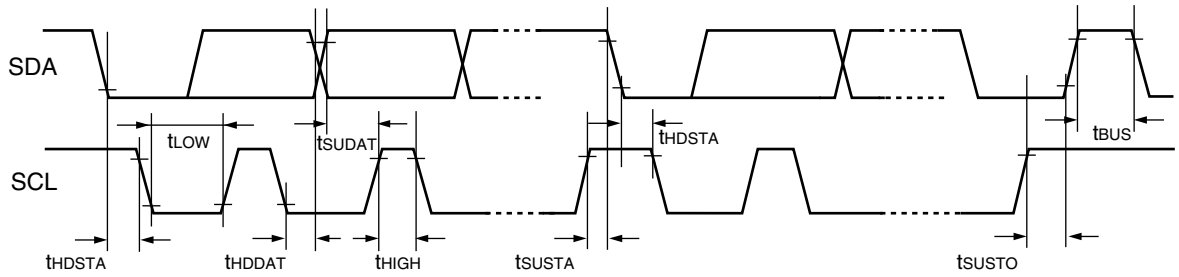
*4 : Refer to "• Note of SDA, SCL set-up time".

• Note of SDA, SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor. Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

•Timing definition

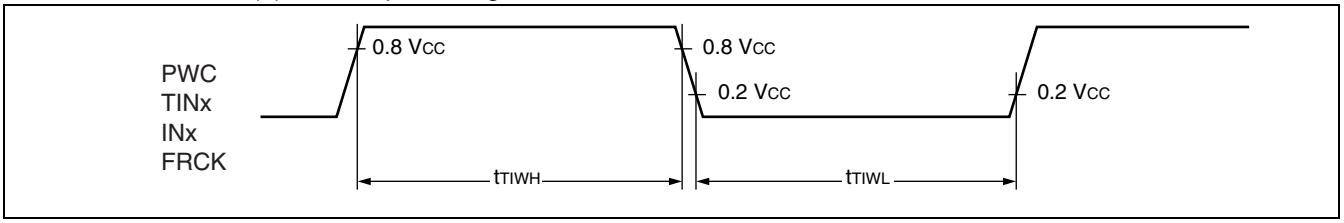


(7) Timer input timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	FRCK, INx, TINx, PWC	—	4 t_{CP}	—	ns

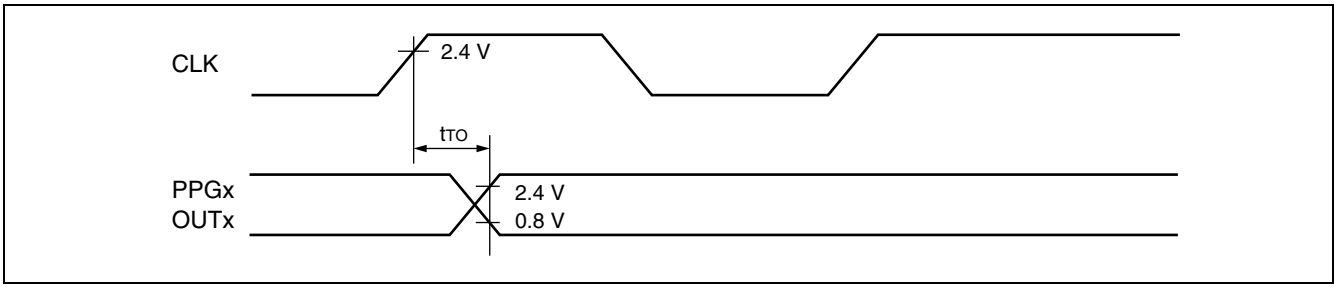
Note : t_{CP} : Refer to " (1) Clock input timing".



(8) Timer output timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
CLK↑→T_{OUT} change time PPG0 to PPG5 change time OUT0 to OUT3 change time	t_{TO}	TOTx, PPGx, OUTx	—	30	—	ns

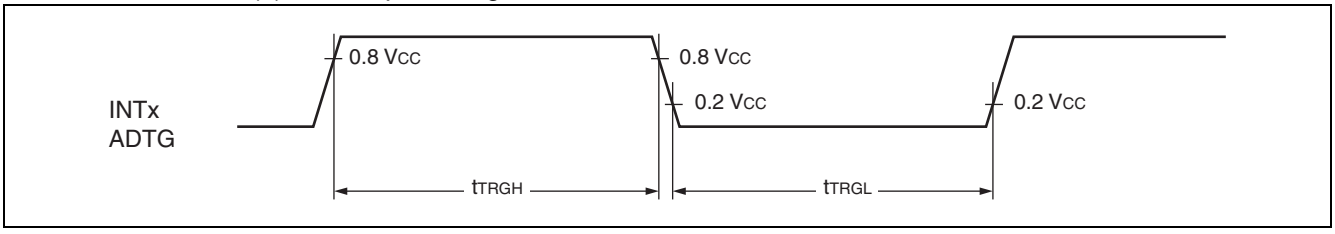


(9) Trigger input timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INTx, ADTG	—	5 t_{CP}	—	ns	At normal operating
				1	—	µs	In Stop mode

Note : t_{CP} : Refer to " (1) Clock input timing".

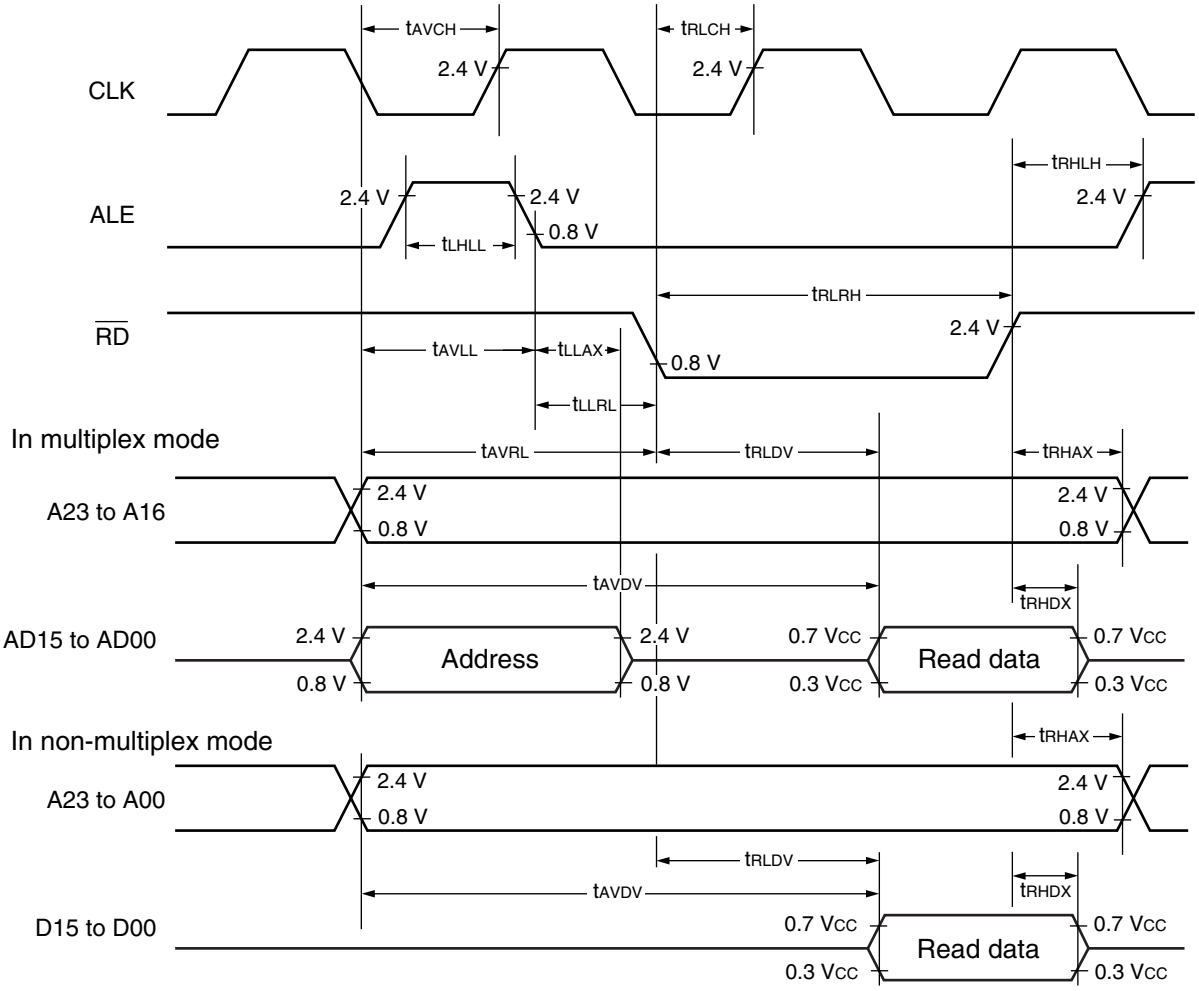


(10) Bus read timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 15$	—	ns	At f_{cp} = 24 MHz
				$t_{CP}/2 - 20$	—	ns	At f_{cp} = 12 MHz
				$t_{CP}/2 - 35$	—	ns	At f_{cp} = 6 MHz
Valid address→ALE↓time	t_{AVLL}	Address, ALE	—	$t_{CP}/2 - 17$	—	ns	
				$t_{CP}/2 - 40$	—	ns	At f_{cp} = 6 MHz
ALE↓→Address valid time	t_{LLAX}	ALE, Address	—	$t_{CP}/2 - 15$	—	ns	
Valid address→$\overline{RD}$↓time	t_{AVRL}	$\overline{RD}$, Address	—	$t_{CP} - 25$	—	ns	
Valid address→valid data input	t_{AVDV}	Address/ data	—	—	$5\ t_{CP}/2 - 55$	ns	
				—	$5\ t_{CP}/2 - 80$	ns	At f_{cp} = 6 MHz
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	—	$3\ t_{CP}/2 - 25$	—	ns	At f_{cp} = 24 MHz
				$3\ t_{CP}/2 - 20$	—	ns	At f_{cp} = 12 MHz
$\overline{RD}$↓→valid data input	t_{RLDV}	$\overline{RD}$, Data	—	—	$3\ t_{CP}/2 - 55$	ns	
				—	$3\ t_{CP}/2 - 80$	ns	At f_{cp} = 6 MHz
$\overline{RD}$↓→data hold time	t_{RHDX}	$\overline{RD}$, Data	—	0	—	ns	
$\overline{RD}$↑→ALE↑time	t_{RHLH}	$\overline{RD}$, ALE	—	$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$↑→address valid time	t_{RHAX}	Address, $\overline{RD}$	—	$t_{CP}/2 - 10$	—	ns	
Valid address→CLK↑time	t_{AVCH}	Address, CLK	—	$t_{CP}/2 - 17$	—	ns	
$\overline{RD}$↓→CLK↑time	t_{RLCH}	$\overline{RD}$, CLK	—	$t_{CP}/2 - 17$	—	ns	
ALE↓→$\overline{RD}$↓time	t_{LLRL}	$\overline{RD}$, ALE	—	$t_{CP}/2 - 15$	—	ns	

Note : t_{CP} : Refer to " (1) Clock input timing".

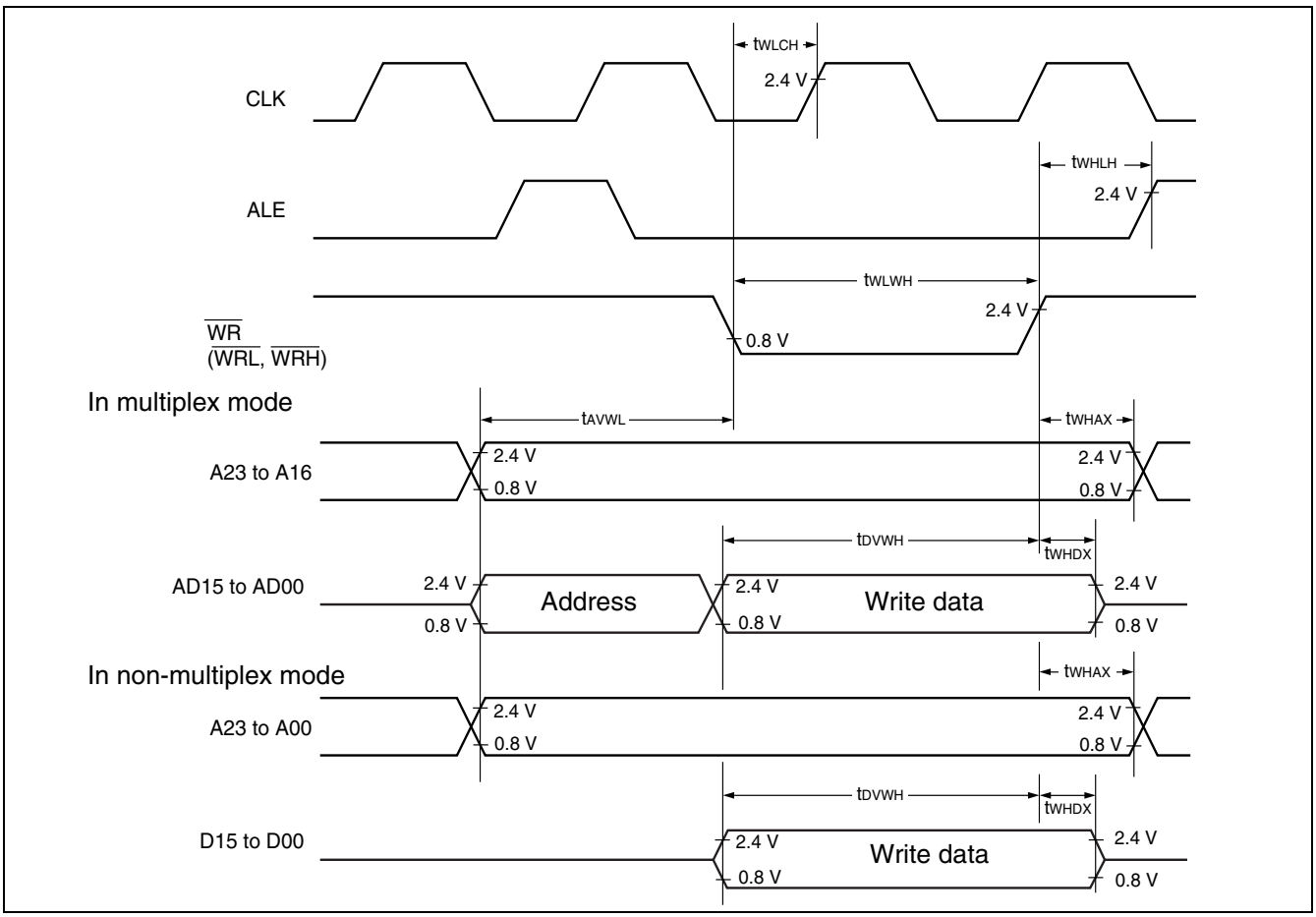

tAVCH
tRLCH
CLK
2.4 V
2.4 V
tRHLH
ALE
2.4 V
2.4 V
2.4 V
0.8 V
tLHLL
tRLRH
RD
2.4 V
tAVLL
tLLAX
0.8 V
tLLRL
In multiplex mode
tAVRL
tRLDV
tRHAX
A23 to A16
2.4 V
0.8 V
2.4 V
0.8 V
tAVDV
tRHDX
AD15 to AD00
2.4 V
Address
2.4 V
0.8 V
0.8 V
0.7 VCC
Read data
0.7 VCC
0.3 VCC
0.3 VCC
In non-multiplex mode
tRHAX
A23 to A00
2.4 V
0.8 V
2.4 V
0.8 V
tRLDV
tAVDV
tRHDX
D15 to D00
0.7 VCC
Read data
0.7 VCC
0.3 VCC
0.3 VCC

(11) Bus write timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address→$\overline{WR}$↓ time	t_{AVWL}	Address, $\overline{WR}$	—	t_{CP} – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WRL}$, $\overline{WRH}$	—	3 t_{CP}/2 – 25	—	ns	At f_{cp} = 24 MHz
			—	3 t_{CP}/2 – 20	—	ns	At f_{cp} = 12 MHz
Valid data output→$\overline{WR}$↑ time	t_{DVWH}	Data, $\overline{WR}$	—	3 t_{CP}/2 – 15	—	ns	
$\overline{WR}$↑→data hold time	t_{WHDX}	$\overline{WR}$, Data	—	10	—	ns	At f_{cp} = 24 MHz
			—	20	—	ns	At f_{cp} = 12 MHz
			—	30	—	ns	At f_{cp} = 6 MHz
$\overline{WR}$↑→address valid time	t_{WHAX}	$\overline{WR}$, Address	—	t_{CP}/2 – 10	—	ns	
$\overline{WR}$↑→ALE↑time	t_{WHLH}	$\overline{WR}$, ALE	—	t_{CP}/2 – 15	—	ns	
$\overline{WR}$↓→CLK↑time	t_{WLCH}	$\overline{WR}$, CLK	—	t_{CP}/2 – 17	—	ns	

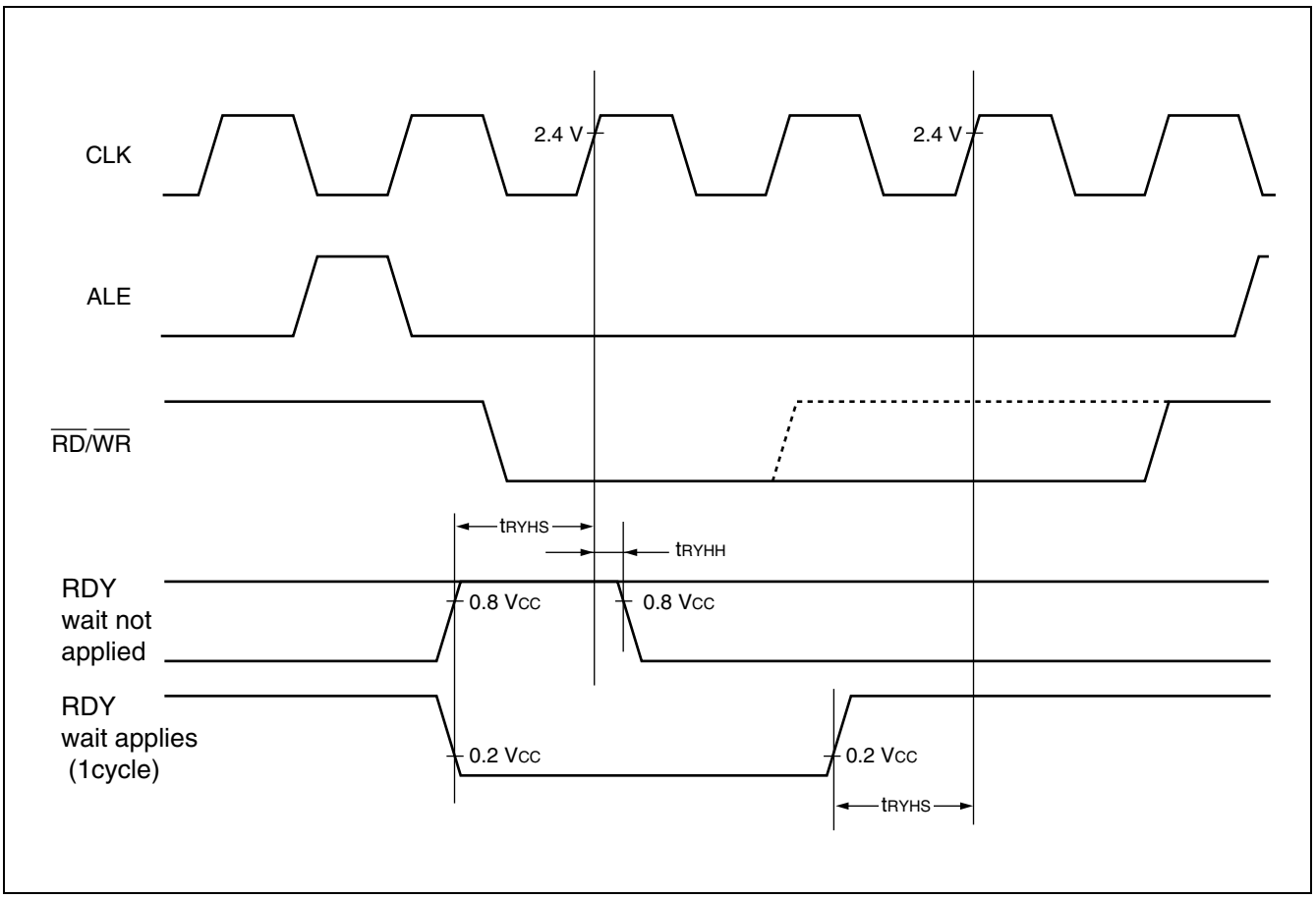
Note : t_{CP} : Refer to “ (1) Clock input timing”.



(12) Ready input timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
RDY set-up time	t_{RYHS}	RDY	—	35	—	ns	
			—	70	—	ns	f_{cp} = 6 MHz
RDY hold time	t_{RYHH}		—	0	—	ns	

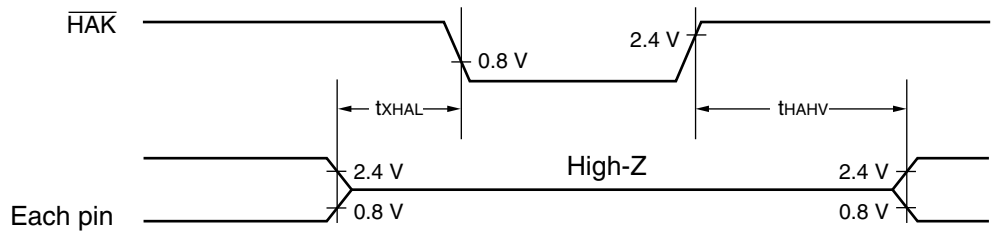


(13) Hold timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns
$\overline{HAK}$ ↓ → pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns

Notes : • It takes one cycle or more for $\overline{HAK}$ to change after the HRQ pin is captured.
• t_{CP} : Refer to " (1) Clock input timing".



5. Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinear error	—	—	—	—	± 2.5	LSB	
Differential linear error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN15	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVRH – AV_{SS})/1024
Full-scale transition voltage	V_{FST}	AN0 to AN15	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V	
Conversion time	—	—	—	176 t_{CP}*1	—	ns	
Sampling time	—	—	—	64 t_{CP}*1	—	ns	
Analog port input current	I_{AIN}	AN0 to AN15	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN15	0	—	AVRH	V	
Reference voltage	—	AVRH	2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	1.4	3.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*2
Reference voltage supplying current	I_R	AVRH	—	95	170	µA	
	I_{RH}	AVRH	—	—	5	µA	*2
Interchannel disparity	—	AN0 to AN15	—	—	4	LSB	

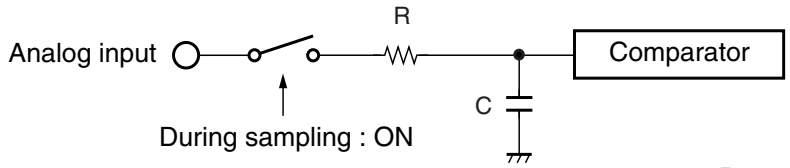
*1 : t_{CP} : Refer to “ 4. AC Characteristics (1) Clock input timing”.

*2 : The current when the CPU is in stop mode and the A/D converter is not operating (For V_{CC} = AV_{CC} = AVRH = 3.3 V).

Notes :

- **About the external impedance of the analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model



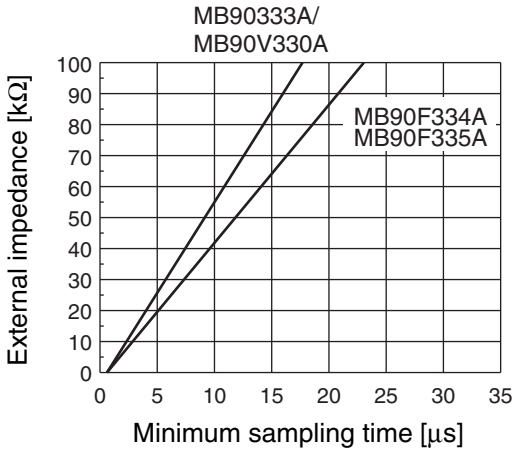
	R	C
MB90333A	1.9 kΩ (Max)	32.3 pF (Max)
MB90F334A	1.9 kΩ (Max)	25.0 pF (Max)
MB90F335A	1.9 kΩ (Max)	25.0 pF (Max)
MB90V330A	1.9 kΩ (Max)	32.3 pF (Max)

Note : The values are reference values.

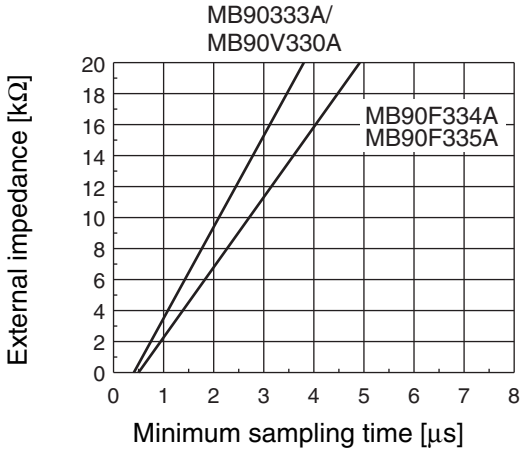
- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between the external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



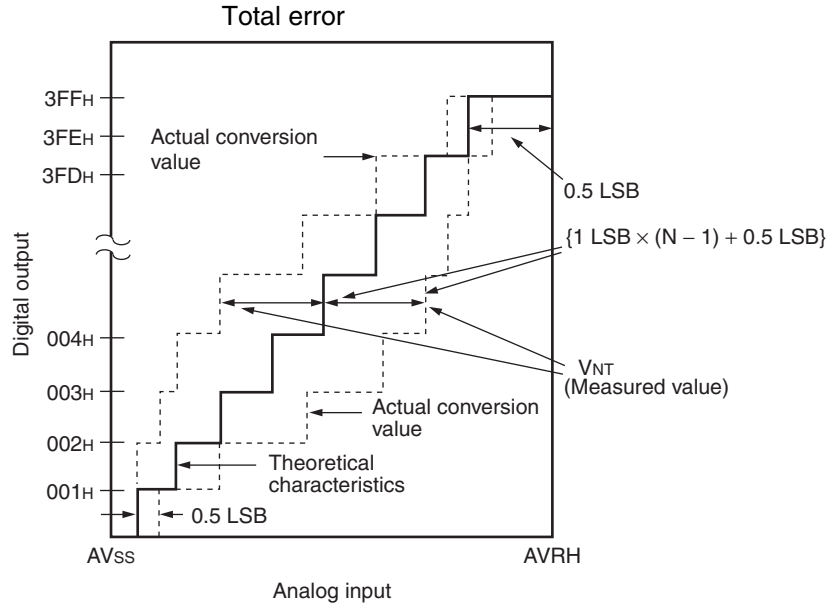
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- **About errors**

As |AVRH| becomes smaller, values of relative errors grow larger.

A/D Converter Glossary

Resolution :	Analog changes that are identifiable with the A/D converter.
Linearity error :	The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics.
Differential linearity error :	The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.
Total error :	The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Theoretical value)} = \frac{AVRH - AVss}{1024}\ [V]$$

V_{OT} (Theoretical value) = AVss + 0.5 LSB [V]

V_{FST} (Theoretical value) = AVRH – 1.5 LSB [V]

V_{NT} : Voltage at a transition of digital output from (N - 1) to N

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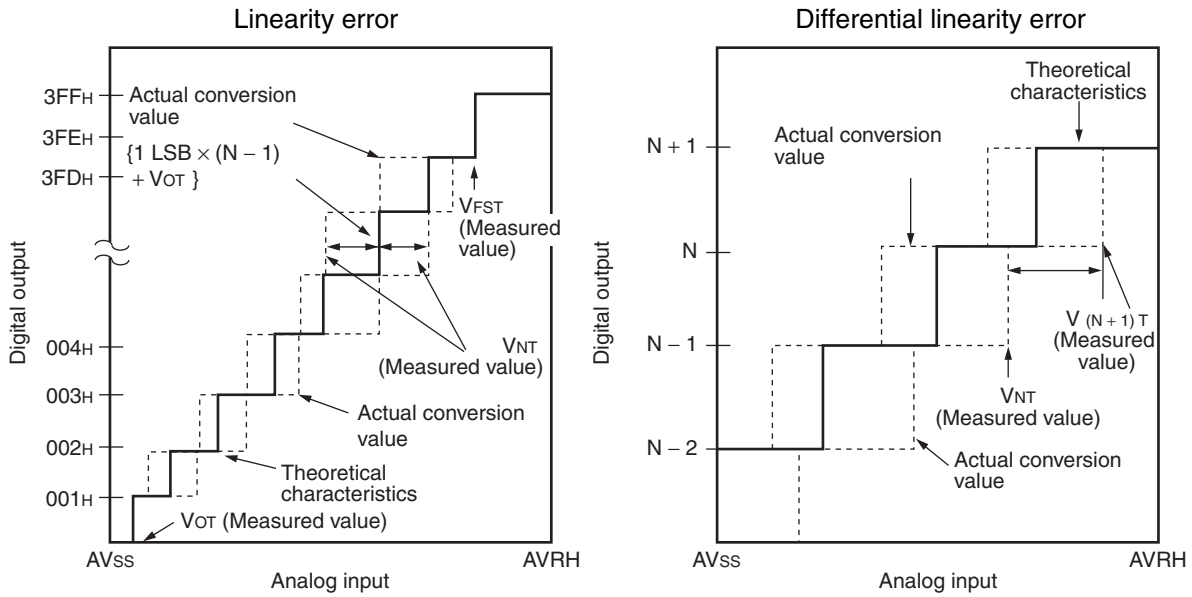


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at transition of digital output from "000_H" to "001_H"
V_{FST} : Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

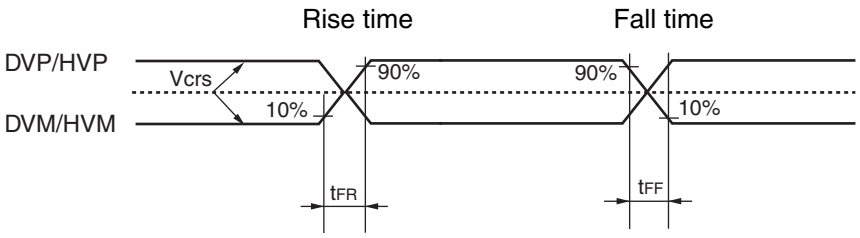
6. USB characteristics

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

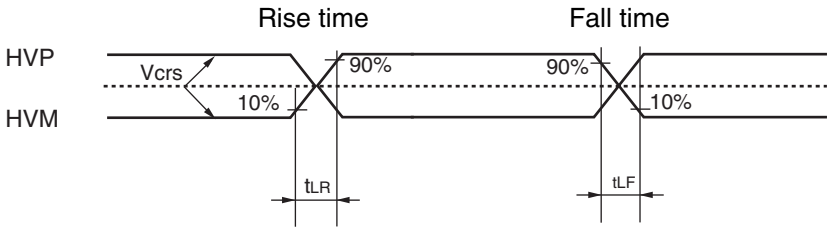
Parameter		Symbol	Value		Unit	Remarks
			Min	Max		
Input characteristics	Input High level voltage	V_{IH}	2.0	—	V	
	Input Low level voltage	V_{IL}	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	V	
	Differential common mode range	V_{CM}	0.8	2.5	V	
Output characteristics	Output High level voltage	V_{OH}	2.8	3.6	V	I_{OH} = – 200 µA
	Output Low level voltage	V_{OL}	0.0	0.3	V	I_{OL} = 2 mA
	Cross over voltage	V_{CRS}	1.3	2.0	V	
	Rise time	t_{FR}	4	20	ns	Full Speed
		t_{LR}	75	300	ns	Low Speed
	Fall time	t_{FF}	4	20	ns	Full Speed
		t_{LF}	75	300	ns	Low Speed
	Rising/falling time matching	t_{RFM}	90	111.11	%	(T_{FR}/T_{FF})
		t_{RLM}	80	125	%	(T_{LR}/T_{LF})
	Output impedance	Z_{DRV}	28	44	Ω	Including Rs = 27 Ω
Series resistance		R_S	25	30	Ω	Recommended value = 27 Ω at using USB*

* : Arrange the series resistance R_S values in order to set the impedance value within the output impedance ZSRV.

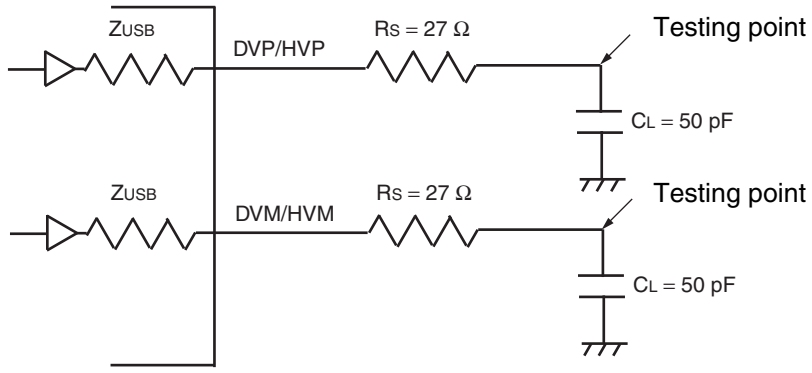
• Data signal timing (Full Speed)



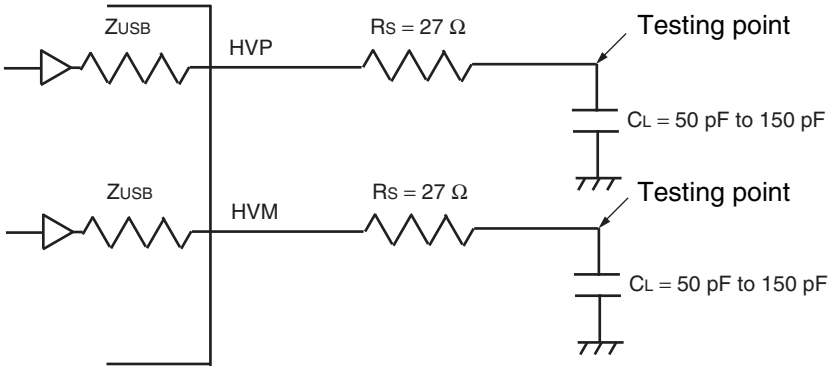
• Data signal timing (Low Speed)



• Load condition (Full Speed)



• Load condition (Low Speed)



7. Flash memory write/erase characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C V_{CC} = 3.0 V	—	1	15	s	Excludes 00H programming prior to erasure.
Chip erase time		—	9	—	s	*:MB90F334A (384 Kbytes) Excludes 00H programming prior to erasure.
		—	14	—		*:MB90F335A (512 Kbytes) Excludes 00H programming prior to erasure.
Word (16-bit width) programming time		—	16	3600	µs	Except for over head time of system level
Programming/erase cycle	—	10000	—	—	cycle	
Flash memory data retaining period	Average T_A = + 85 °C	20	—	—	year	*

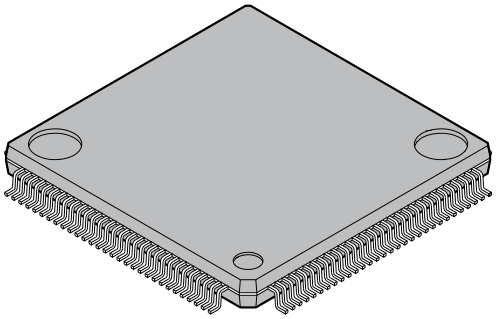
* : This value comes from the technology qualification. (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C)

■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F334APMC1 MB90F335APMC1 MB90333APMC1	120-pin plastic LQFP (FPT-120P-M24)	
MB90F334APMC MB90F335APMC MB90333APMC	120-pin plastic LQFP (FPT-120P-M21)	
MB90V330ACR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation

■ PACKAGE DIMENSIONS

120-pin plastic LQFP

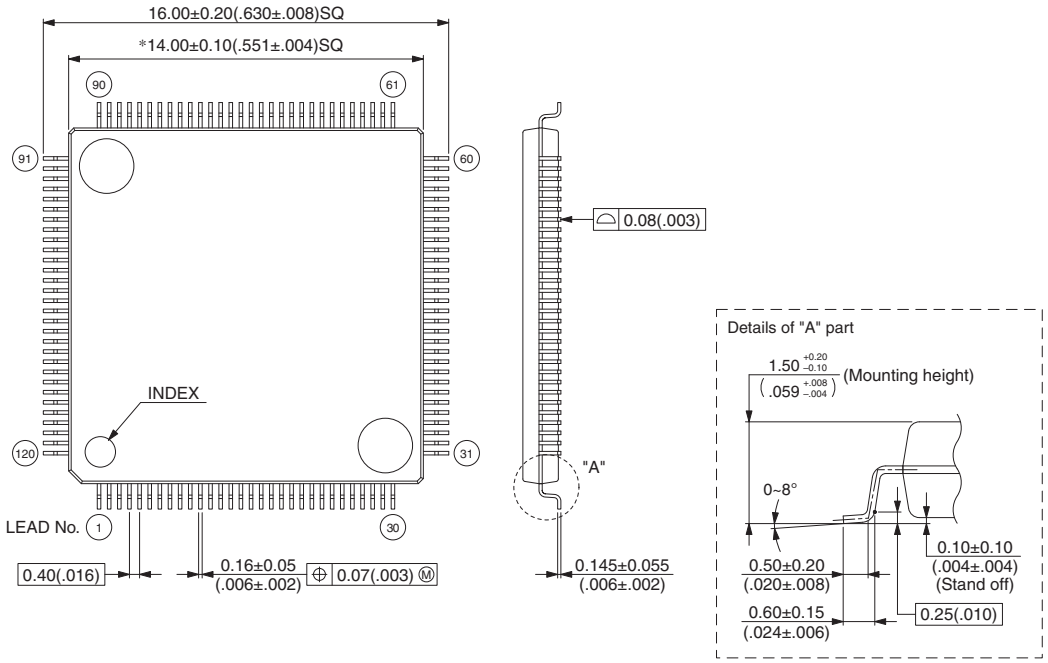


(FPT-120P-M24)

Lead pitch	0.40 mm
Package width × package length	14.0 mm × 14.0 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Code (Reference)	P-LFQFP120-14×14-0.40

120-pin plastic LQFP
(FPT-120P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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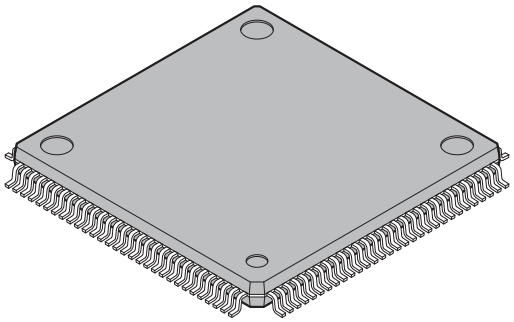
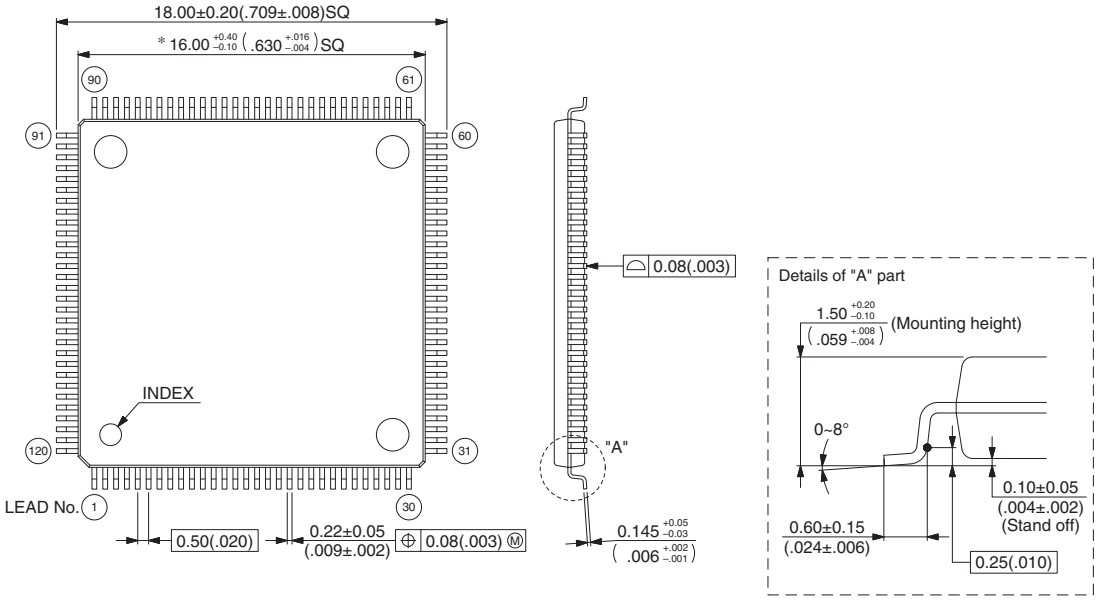
120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
39	■ ELECTRICAL CHARACTERISTICS 2. Recommended Operating Conditions	Corrected the remarks for operating temperature as follows; When using USB → When using USB, at external bus operation

The vertical lines marked in the left side of the page show the changes.

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FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fsl/en/

For further information please contact:

North and South America
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://us.fujitsu.com/micro/

Europe
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/semiconductor/

Korea
FUJITSU SEMICONDUCTOR KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fujitsu.com/sg/services/micro/semiconductor/

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fmc/en/

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