Low-Power Dual Channel Digital Isolators

Check for Samples: ISO7420E, ISO7420FE, ISO7421E, ISO7421FE

FEATURES

- **Signaling Rate > 50 Mbps**
- **For Devices with Suffix F, Output is Low in Fail-Safe Mode**
- **Low Power Consumption: Typical I_{CC} per Channel (3.3V Supplies):**
  - **ISO7420: 1.4 mA at 1 Mbps, 2.5 mA at 25 Mbps**
  - **ISO7421: 1.8 mA at 1 Mbps, 2.8 mA at 25 Mbps**
- **Low Propagation Delay: 7 ns (Typical)**
- **Low Pulse Skew: 200 ps (Typical)**
- **Wide T_A Range Specified: –40°C to 125°C**
- **50 KV/μs Transient Immunity, Typical**
- **Isolation Barrier Life: > 25 Years**
- **Operates from 3V to 5.5V Supply Levels**
- **Narrow Body SOIC-8 Package**

APPLICATIONS

- **Opto-Coupler Replacement in:**
  - **Industrial FieldBus**
    - **ProfiBus**
    - **ModBus**
    - **DeviceNet™ Data Buses**
  - **Servo Control Interface**
  - **Motor Control**
  - **Power Supplies**
  - **Battery Packs**

SAFETY AND REGULATORY APPROVALS

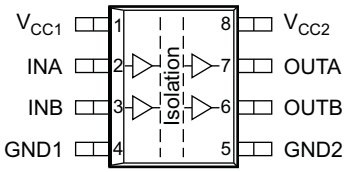
- **2.5 KV_{RMS} for 1 minute per UL 1577**
- **CSA Component Acceptance Notice 5A**
- **IEC 60747-5-2 (VDE 0884 Rev. 2)**
- **IEC 60950-1 and IEC 61010-1 End Equipment Standards**
- **All Approvals Pending**

DESCRIPTION

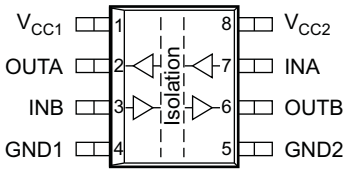
ISO7420E, ISO7420FE, ISO7421E and ISO7421FE provide galvanic isolation up to 2.5 KV_{RMS} for 1 minute per UL. These devices have two isolated channels. Each channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. The suffix F indicates low-output option in fail-safe condition (see Table 1).

These devices have TTL input thresholds and operate from 3V to 5.5V supplies. All inputs are 5V tolerant when supplied from a 3.3V supply.

ISO7420
D Package
(Top View)



ISO7421
D Package
(Top View)



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN DESCRIPTIONS

PIN			I/O	DESCRIPTION
NAME	ISO7420x	ISO7421x		
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
GND1	4	4	–	Ground connection for V_{CC1}
GND2	5	5	–	Ground connection for V_{CC2}
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V_{CC1}	1	1	–	Power supply, V_{CC1}
V_{CC2}	8	8	–	Power supply, V_{CC2}

Table 1. FUNCTION TABLE(1)

INPUT SIDE V_{CC}	OUTPUT SIDE V_{CC}	INPUT INA, INB	OUTPUT OUTA, OUTB	
			ISO7420E / ISO7421E	ISO7420FE / ISO7421FE
PU	PU	H	H	H
		L	L	L
		Open	H(2)	L(3)
PD	PU	X	H(2)	L(3)
PU	PD	X	Z	Z

(1) PU = Powered up (V_{CC} ≥ 3 V); PD = Powered down (V_{CC} ≤ 2.4 V); X = Irrelevant; H = High level; L = Low level; Z = High Impedance
(2) In fail-safe condition, output defaults to high level
(3) In fail-safe condition, output defaults to low level

AVAILABLE OPTIONS

PRODUCT	RATED ISOLATION	PACKAGE	INPUT THRESHOLD	RATED T_A	CHANNEL DIRECTION	MARKED AS	ORDERING NUMBER
ISO7420E(1)	2.5 KV_{RMS}	D-8	~1.5 V TTL (CMOS compatible)	–40°C to 125°C	Same	SO7420	ISO7420ED (rail)
							ISO7420EDR (reel)
ISO7420FE						I7420F	ISO7420FED (rail)
							ISO7420FEDR (reel)
ISO7421E(1)					Opposite	SO7421	ISO7421ED (rail)
							ISO7421EDR (reel)
ISO7421FE(1)						I7421F	ISO7421FED (rail)
							ISO7421FEDR (reel)

(1) Product Preview

ABSOLUTE MAXIMUM RATINGS(1)

					VALUE
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5 V to 6 V
V_I	Voltage at IN, OUT				–0.5 V to 6 V
I_O	Output current				±15 mA
ESD	Electrostatic discharge	Human-body model	JEDEC Standard 22, Test Method A114-C.01	All pins	±3 kV
		Field-induced charged-device model	JEDEC Standard 22, Test Method C101		±1.5 kV
		Machine model	ANSI/ESDS5.2-1996		±200 V
$T_{J(Max)}$	Maximum junction temperature				150°C
T_{stg}	Storage temperature				-65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3.0		5.5	V
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V
t_{ui}	Input pulse duration	20			ns
1 / t_{ui}	Signaling rate	0		50(1)	Mbps
T_J(2)	Junction temperature	–40		136	°C
T_A	Ambient Temperature	-40	25	125	°C

(1) Under typical conditions, the device is capable of signaling rate > 150 Mbps.
(2) To maintain the recommended operating conditions for T_J, see the *Package Thermal Characteristics* table.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} = 5V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.		V_{CCx} (1) – 0.8	4.6		V
		I_{OH} = –20 μA; see Figure 1.		V_{CCx} (1) – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 μA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	μA
I_{IL}	Low-level input current			–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	50		kV/μs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
	ISO7420x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.4	0.8	mA
I_{CC2}					3.4	5	
I_{CC1}		10 Mbps	C_L = 15pF		0.6	1	
I_{CC2}					4.5	6	
I_{CC1}		25 Mbps			1	1.5	
I_{CC2}					6.2	8	
I_{CC1}		50 Mbps			1.7	2.5	
I_{CC2}					9	12	
	ISO7421x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		2.3	3.6	mA
I_{CC2}					2.3	3.6	
I_{CC1}		10 Mbps	C_L = 15pF		2.9	4.2	
I_{CC2}					2.9	4.2	
I_{CC1}		25 Mbps			3.9	5.3	
I_{CC2}					3.9	5.3	
I_{CC1}		50 Mbps			5.5	7	
I_{CC2}					5.5	7	

(1) V_{CCx} is the supply voltage for the output channel that is being measured

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} = 5V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1.		7	11	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.2	3	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time			0.3	1	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				3.7	ns
t_r	Output signal rise time	See Figure 1.		1.8		ns
t_f	Output signal fall time			1.7		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2.		6		μs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} = 5V ± 10%, V_{CC2} = 3.3V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.	ISO7421x (5V side)	V_{CC1} – 0.8	4.6		V
			ISO7420x/7421x (3.3V side)	V_{CC2} - 0.4	3		
		I_{OH} = –20 μA; see Figure 1,	ISO7421x (5V side)	V_{CC1} – 0.1	5		
			ISO7420x/7421x (3.3V side)	V_{CC2} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 μA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	μA
I_{IL}	Low-level input current			–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	50		kV/μs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
	ISO7420x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.4	0.8	mA
I_{CC2}					2.6	3.7	
I_{CC1}		10 Mbps	C_L = 15pF		0.6	1	
I_{CC2}					3.3	4.3	
I_{CC1}		25 Mbps			1	1.5	
I_{CC2}					4.4	5.6	
I_{CC1}		50 Mbps			1.7	2.5	
I_{CC2}					6.2	7.5	
	ISO7421x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		2.3	3.6	mA
I_{CC2}					1.8	2.8	
I_{CC1}		10 Mbps	C_L = 15pF		2.9	4.2	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps			3.9	5.3	
I_{CC2}					2.8	3.9	
I_{CC1}		50 Mbps			5.5	7	
I_{CC2}					3.8	5	

SWITCHING CHARACTERISTICS

V_{CC1} = 5V ± 10%, V_{CC2} = 3.3V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1.		8	13.5	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.3	3	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time				1.5	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				5.4	ns
t_r	Output signal rise time	See Figure 1.		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2.		6		μs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} = 3.3V ± 10%, V_{CC2} = 5V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.	ISO7421x (3.3V side)	V_{CC1} – 0.4	3		V
			ISO7420x/7421x (5V side)	V_{CC2} – 0.8	4.6		
		I_{OH} = –20 μA; see Figure 1	ISO7421x (3.3V side)	V_{CC1} – 0.1	3.3		
			ISO7420x/7421x (5V side)	V_{CC2} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 μA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	μA
I_{IL}	Low-level input current			–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	50		kV/μs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
	ISO7420x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.2	0.4	mA
I_{CC2}					3.4	5	
I_{CC1}		10 Mbps	C_L = 15pF		0.4	0.6	
I_{CC2}					4.5	6	
I_{CC1}		25 Mbps			0.6	0.9	
I_{CC2}					6.2	8	
I_{CC1}		50 Mbps			1	1.3	
I_{CC2}					9	12	
	ISO7421x						
I_{CC1}	Supply current for V_{CC2} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		1.8	2.8	mA
I_{CC2}					2.3	3.6	
I_{CC1}		10 Mbps	C_L = 15pF		2.2	3.2	
I_{CC2}					2.9	4.2	
I_{CC1}		25 Mbps			2.8	3.9	
I_{CC2}					3.9	5.3	
I_{CC1}		50 Mbps			3.8	5	
I_{CC2}					5.5	7	

SWITCHING CHARACTERISTICS

V_{CC1} = 3.3V ± 10%, V_{CC2} = 5V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1.		7.5	12	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.7	3	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time			0.5	1.5	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.6	ns
t_r	Output signal rise time	See Figure 1.		1.7		ns
t_f	Output signal fall time			1.6		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2.		6		μs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} = 3.3 V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.		V_{CCx} (1) – 0.4	3		V
		I_{OH} = –20 μA; see Figure 1.		V_{CCx} (1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 μA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	μA
I_{IL}	Low-level input current			–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	50		kV/μs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
	ISO7420x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.2	0.4	mA
I_{CC2}					2.6	3.7	
I_{CC1}		10 Mbps	C_L = 15pF		0.4	0.6	
I_{CC2}					3.3	4.3	
I_{CC1}		25 Mbps			0.6	0.9	
I_{CC2}					4.4	5.6	
I_{CC1}		50 Mbps			1	1.3	
I_{CC2}					6.2	7.5	
	ISO7421x						
I_{CC1}	Supply current for V_{CC2} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		1.8	2.8	mA
I_{CC2}					1.8	2.8	
I_{CC1}		10 Mbps	C_L = 15pF		2.2	3.2	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps			2.8	3.9	
I_{CC2}					2.8	3.9	
I_{CC1}		50 Mbps			3.8	5	
I_{CC2}					3.8	5	

(1) V_{CCx} is the supply voltage for the output channel that is being measured

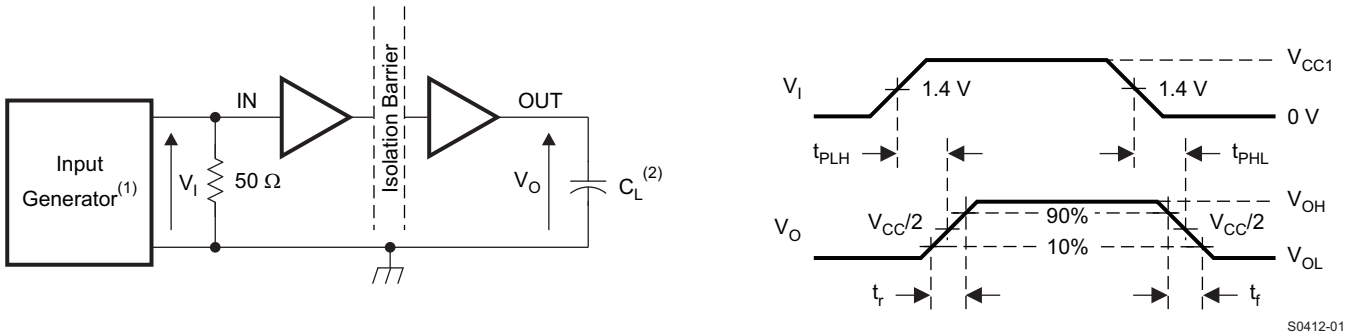
SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} = 3.3 V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1.		8.5	14	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	2	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time			0.4	2	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				6.2	ns
t_r	Output signal rise time	See Figure 1.		2		ns
t_f	Output signal fall time			1.8		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2.		6		μs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

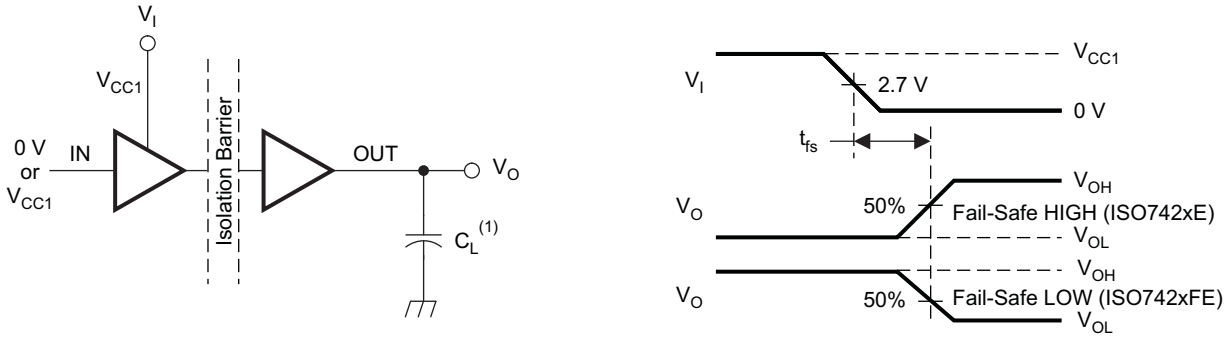
PARAMETER MEASUREMENT INFORMATION



(1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in an actual application.

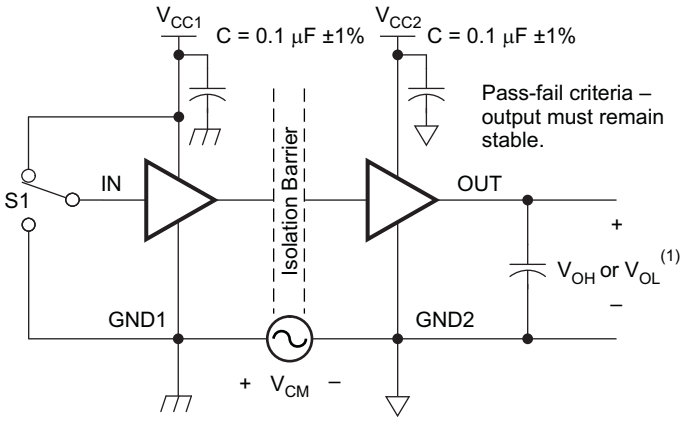
(2) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

IEC INSULATION AND SAFETY-RELATED SPECIFICATIONS FOR THE D-8 PACKAGE

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4.8			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4.3			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	>400			V
	Minimum internal gap (internal clearance)	Distance through the insulation	0.014			mm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A < 100°C		>10^{12}		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		>10^{11}		Ω
C_{IO}	Barrier capacitance, input to output(1)	V_{IO} = 0.4 sin (2πft), f = 1 MHz		1		pF
C_I	Input capacitance(2)	V_I = V_{CC}/2 + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		1		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

INSULATION CHARACTERISTICS(3)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		560	V_{PEAK}
V_{PR}	Input-to-output test voltage per IEC 60747-5-2	Method a, After environmental tests subgroup 1, V_{PR} = V_{IORM} x 1.6, t = 10 s, Partial Discharge < 5 pC	896	V_{PEAK}
		Method b1, V_{PR} = V_{IORM} x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	1050	
		After Input/Output safety test subgroup 2/3, V_{PR} = V_{IORM} x 1.2, t = 10 s, Partial discharge < 5 pC	672	
V_{IOTM}	Transient overvoltage per IEC 60747-5-2	V_{TEST} = V_{IOTM} t = 60 sec (qualification) t= 1 sec (100% production)	4000	V_{PEAK}
V_{ISO}	Isolation voltage per UL	V_{TEST} = V_{ISO}, t = 60 sec (qualification)	2500	V_{RMS}
		V_{TEST} = 1.2 x V_{ISO}, t = 1 sec (100% production)	3000	
R_S	Insulation resistance	V_{IO} = 500 V at T_S	>10^9	Ω
	Pollution degree		2	

(3) Climatic Classification 40/125/21

Table 2. IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 Vrms	I–IV
	Rated mains voltage ≤ 300 Vrms	I–III
	Rated mains voltage ≤ 400 Vrms	I–II

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program(1)
File number: pending (40016131)	File number: pending (220991)	File number: pending (E181974)

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

LIFE EXPECTANCY vs WORKING VOLTAGE

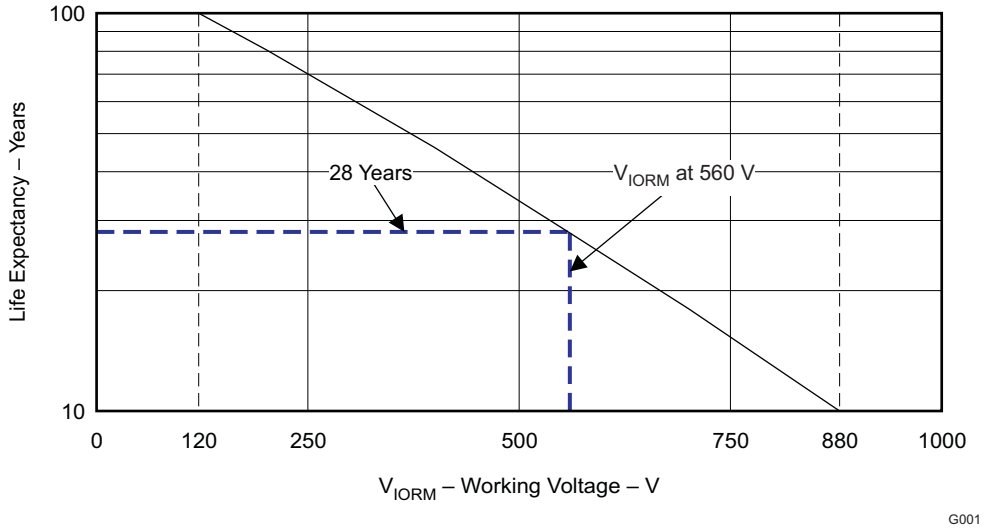


Figure 4. Life Expectancy vs Working Voltage

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 212°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			107	mA
		θ_{JA} = 212°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			164	
T_S	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Characteristics* table is that of a device installed in the JESD51-3, Low-Effective-Thermal-Conductivity Test Board for Leaded Surface-Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

PACKAGE THERMAL CHARACTERISTICS

(over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air thermal resistance	Low-K thermal resistance(1)		212		°C/W
		High-K thermal resistance(1)		122		
θ_{JB}	Junction-to-board thermal resistance			37		°C/W
θ_{JC}	Junction-to-case thermal resistance			69.1		°C/W
P_D	Device power dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 100-Mbps 50% duty-cycle square wave			138	mW

(1) Tested in accordance with the low-K or high-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages

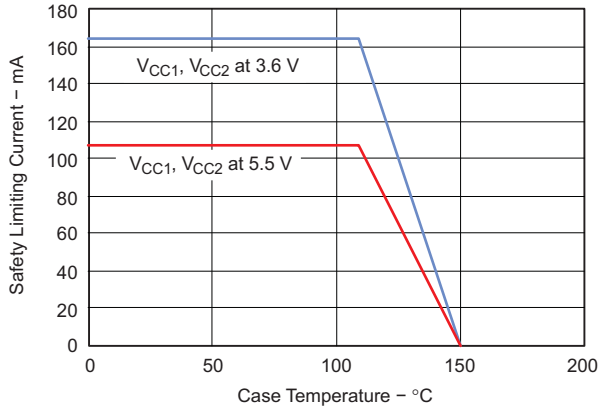


Figure 5. θ_{JC} Thermal Derating Curve per IEC 60747-5-2

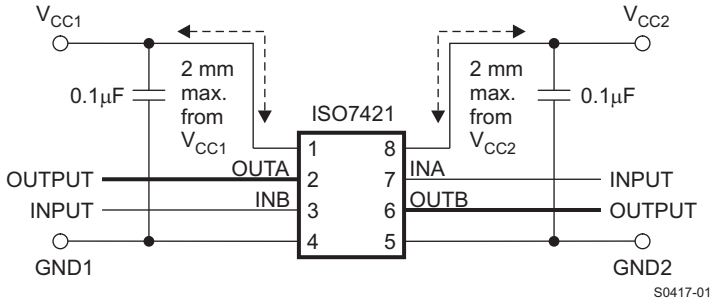


Figure 6. Typical ISO742x Application Circuit

Note: For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide.*

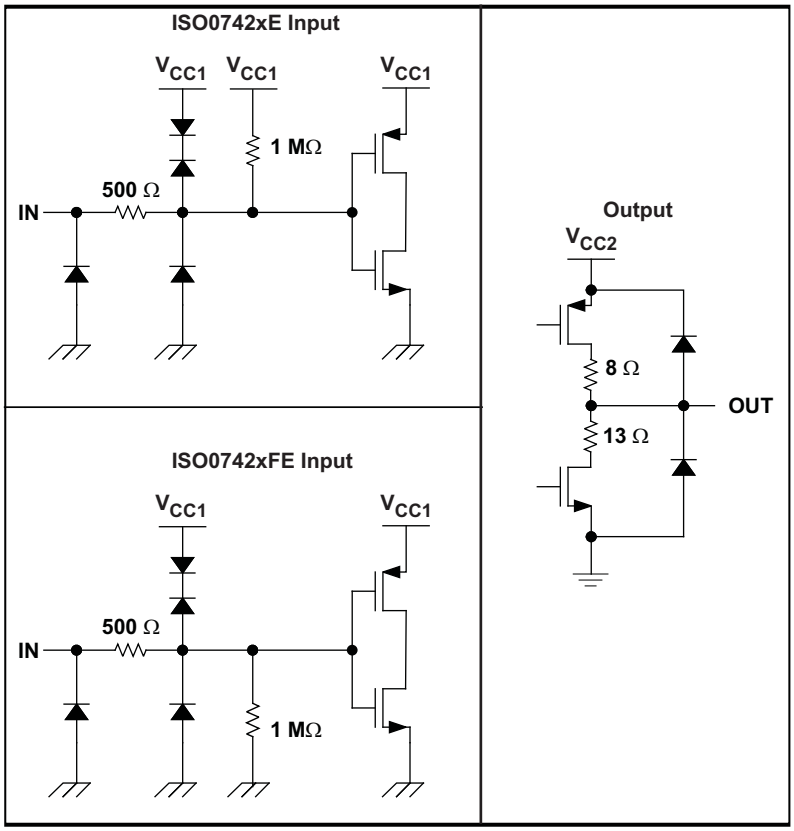


Figure 7. Device I/O Schematics

TYPICAL CHARACTERISTICS

ISO7420 SUPPLY CURRENT PER CHANNEL vs DATA RATE (NO LOAD)

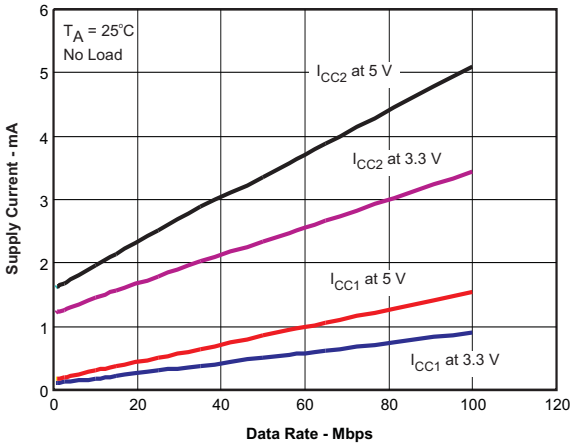


Figure 8. ISO7420x

ISO7420 SUPPLY CURRENT ALL CHANNELS vs DATA RATE (NO LOAD)

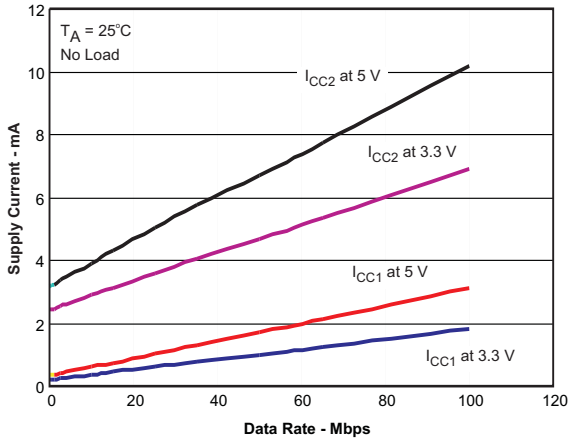


Figure 9. ISO7420x

ISO7420 SUPPLY CURRENT PER CHANNEL vs DATA RATE (15 pF LOAD)

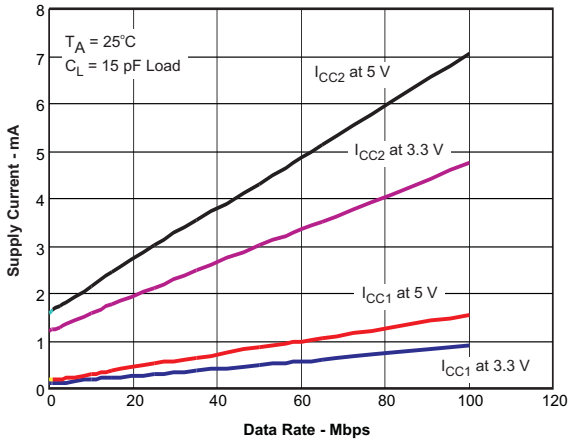


Figure 10.

ISO7420 SUPPLY CURRENT ALL CHANNELS vs DATA RATE (15 pF LOAD)

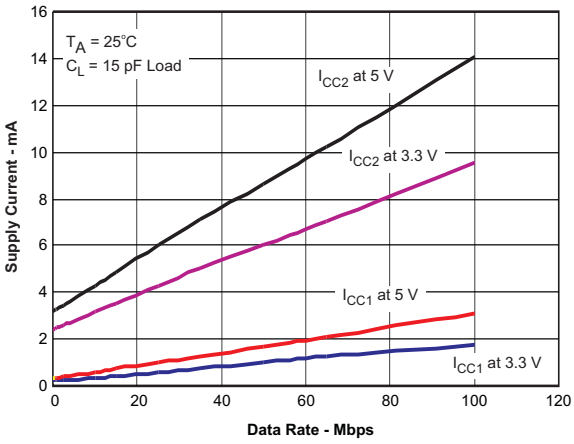


Figure 11.

TYPICAL CHARACTERISTICS (continued)

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

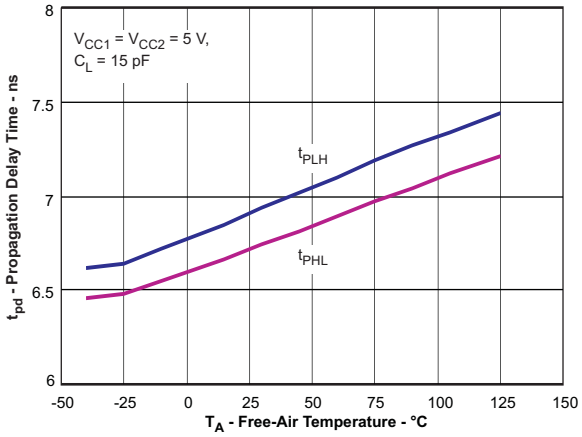


Figure 12.

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

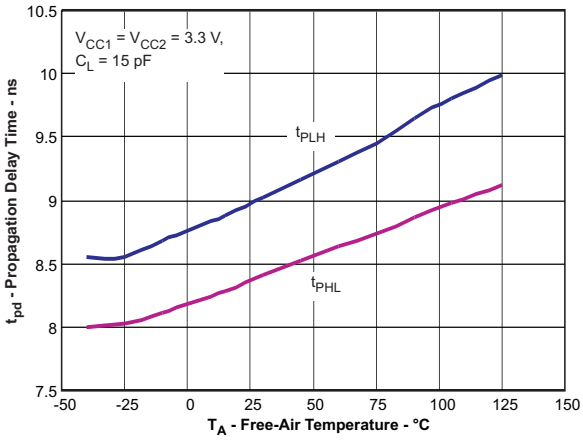


Figure 13.

INPUT V_{CC} FAIL-SAFE VOLTAGE THRESHOLD vs FREE-AIR TEMPERATURE

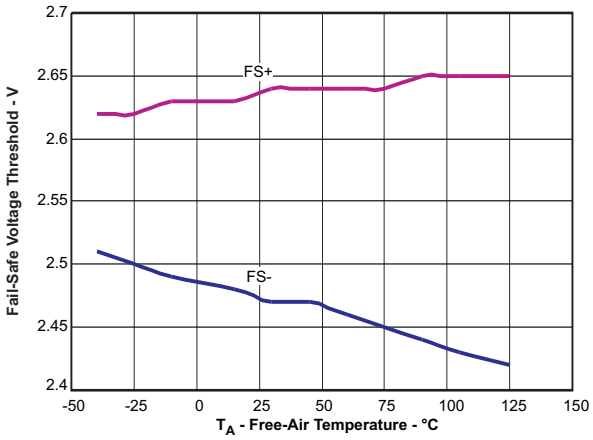


Figure 14.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEl OUTPUT CURRENT

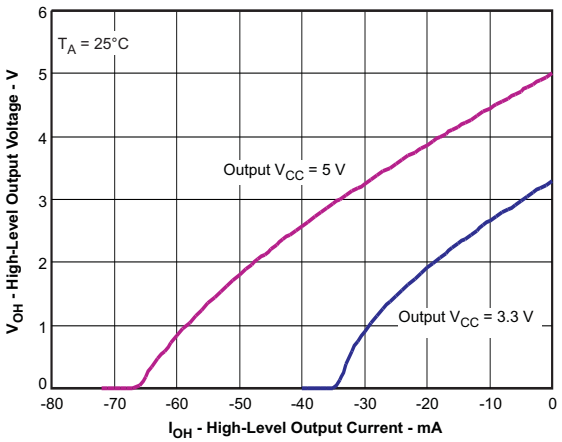


Figure 15.

TYPICAL CHARACTERISTICS (continued)

LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEI OUTPUT CURRENT

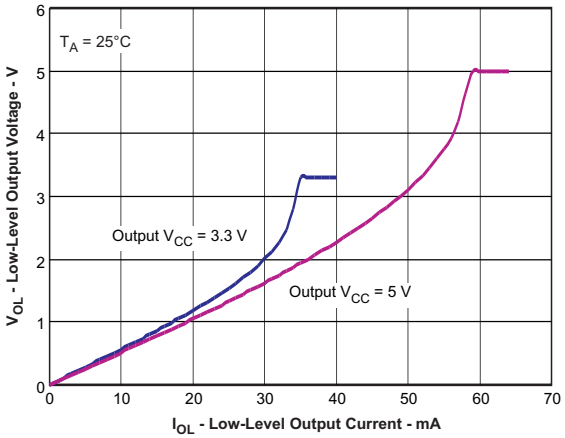


Figure 16.

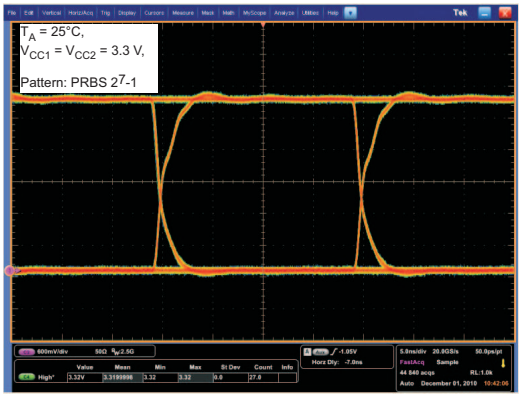


Figure 17. Typical Eye Diagram at 50 MBPS, 3.3 V Operation

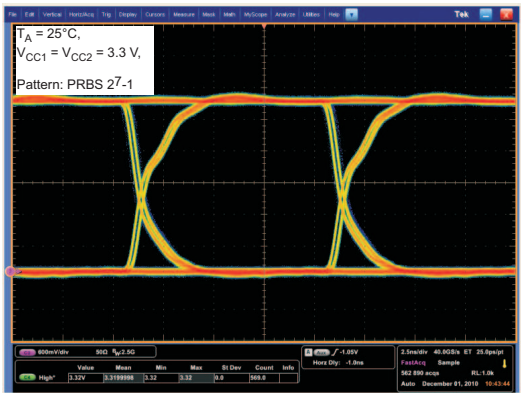


Figure 18. Typical Eye Diagram at 100 MBPS, 3.3 V Operation

REVISION HISTORY

Changes from Original (December 2010) to Revision A **Page**

- Changed the Max values for Supply current for V_{CC1} and V_{CC2}, C_L = 15pF 7

Changes from Revision A (December 2010) to Revision B **Page**

- Changed Feature bullet From: ISO7421: TBDmA at 1Mbps, TBDmA at 25Mbps To: ISO7421: 1.8mA at 1Mbps, 2.8mA at 25Mbps 1
- Updated the ISO7421x Supply Current values for V_{CC1} and V_{CC2} = 5V 4
- Updated the ISO7421x Supply Current values for V_{CC1} = 5V and V_{CC2} = 3.3V 5
- Updated the ISO7421x Supply Current values for V_{CC1} = 3.3V and V_{CC2} = 5V 6
- Updated the ISO7421x Supply Current values for V_{CC1} and V_{CC2} = 3.3V 7

PACKAGING INFORMATION

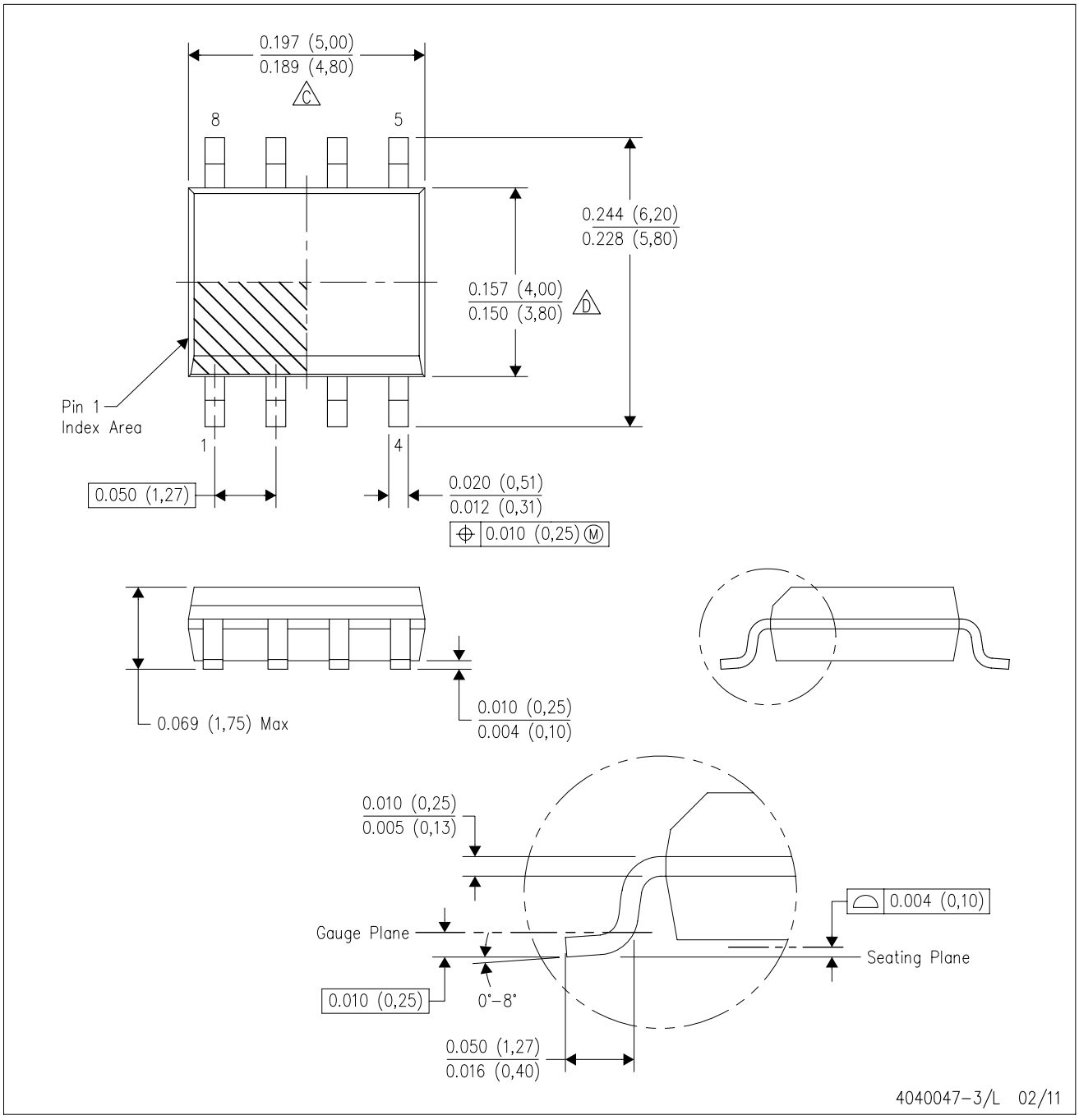
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ISO7420FED	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

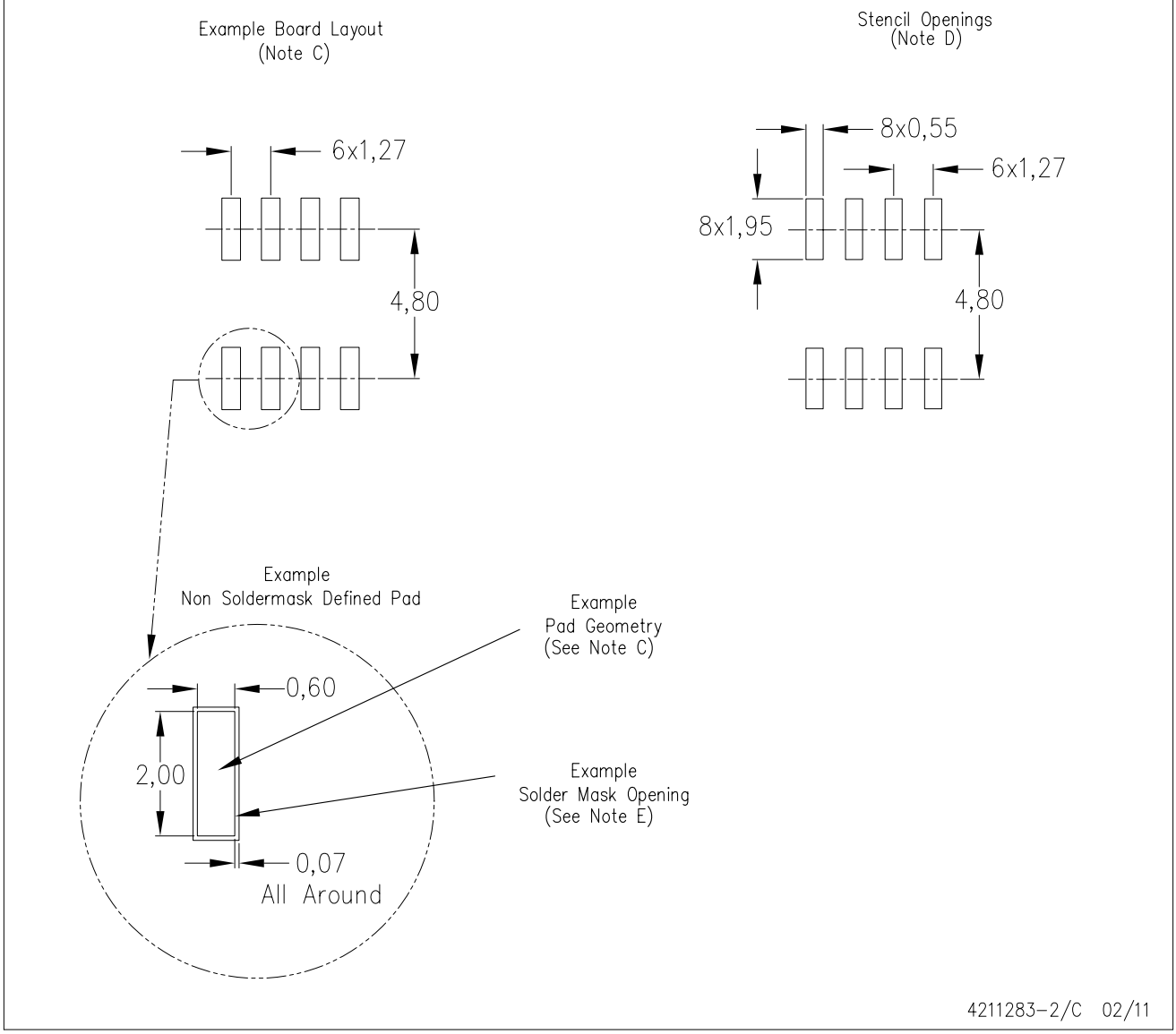
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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