CY14B101Q1
CY14B101Q2
CY14B101Q3

1 Mbit (128K x 8) Serial SPI nvSRAM

Features

- 1 Mbit Nonvolatile SRAM
  - Internally organized as 128K x 8
  - STORE to QuantumTrap Nonvolatile Elements initiated automatically on Power Down (AutoStore) or by user using HSB Pin (Hardware Store) or SPI instruction (Software Store)
  - RECALL to SRAM initiated on Power Up (Power Up Recall) or by SPI Instruction (Software RECALL)
  - Automatic STORE on Power Down with a small Capacitor
- High Reliability
  - Infinite Read, Write, and RECALL Cycles
  - 1 Million STORE cycles to QuantumTrap
  - Data Retention: 20 Years
- High Speed Serial Peripheral Interface (SPI)
  - 40 MHz Clock Rate
  - Supports SPI Modes 0 (0,0) and 3 (1,1)
- Write Protection
  - Hardware Protection using Write Protect ($\overline{WP}$) Pin
  - Software Protection using Write Disable Instruction
  - Software Block Protection for 1/4,1/2, or entire Array
- Low Power Consumption
  - Single 3V +20%, –10% Operation
  - Average V_{CC} current of 10 mA at 40 MHz Operation
- Industry Standard Configurations
  - Industrial Temperature
  - CY14B101Q1 has identical pin configuration to industry standard 8-pin NV Memory
  - 8-pin DFN and 16-pin SOIC Packages
  - RoHS Compliant

Functional Overview

The Cypress CY14B101Q1/CY14B101Q2/CY14B101Q3 combines a 1 Mbit nonvolatile static RAM with a nonvolatile element in each memory cell. The memory is organized as 128K words of 8 bits each. The embedded nonvolatile elements incorporate the QuantumTrap technology, creating the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while the QuantumTrap cell provides highly reliable nonvolatile storage of data. Data transfers from SRAM to the nonvolatile elements (STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM from the nonvolatile memory (RECALL operation). Both STORE and RECALL operations can also be triggered by the user.

Configuration

Feature	CY14B101Q1	CY14B101Q2	CY14B101Q3
AutoStore	No	Yes	Yes
Software STORE	Yes	Yes	Yes
Hardware STORE	No	No	Yes

Logic Block Diagram

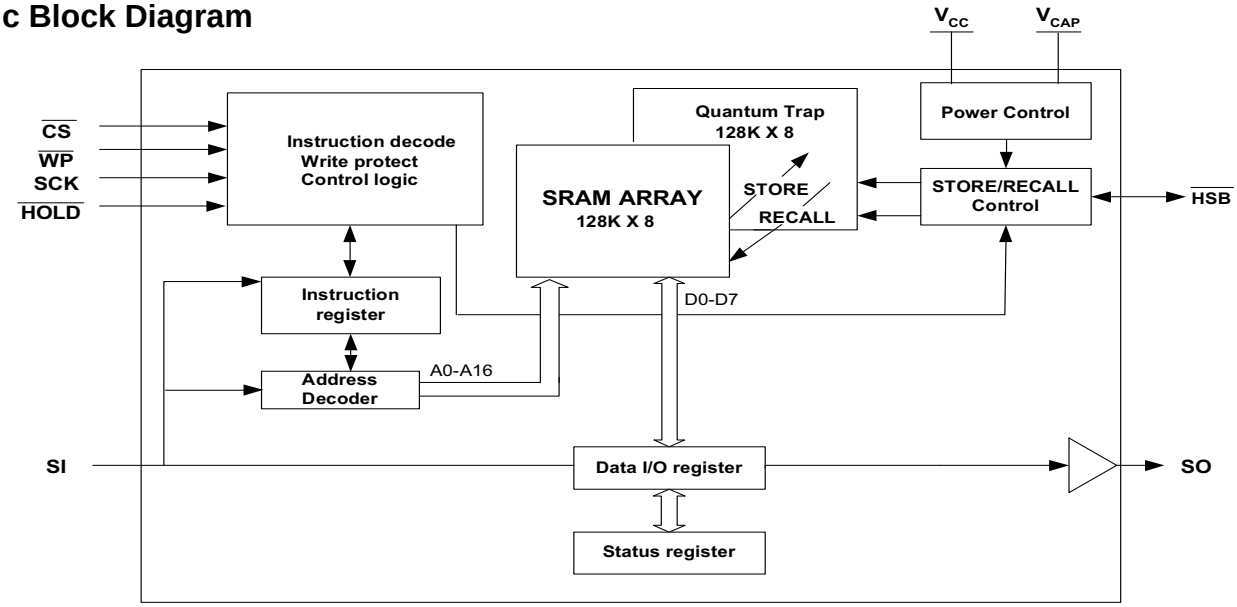

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Figure 2. Pin Diagram - 16-Pin SOIC

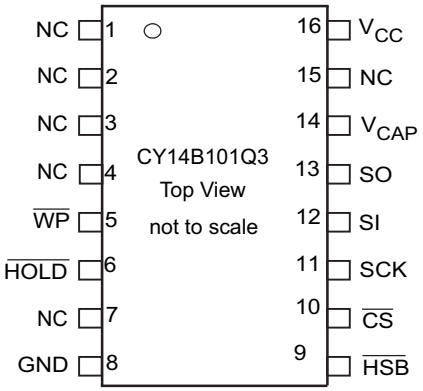


Table 1. Pin Definitions

Pin Name	I/O Type	Description
$\overline{CS}$	Input	**Chip Select**. Activates the device when pulled LOW. Driving this pin high puts the device in low power standby mode.
SCK	Input	**Serial Clock**. Runs at speeds up to maximum 40 MHz. All inputs are latched at the rising edge of this clock. Outputs are driven at the falling edge of the clock.
SI	Input	**Serial Input**. Pin for input of all SPI instructions and data.
SO	Output	**Serial Output**. Pin for output of data through SPI.
$\overline{WP}$	Input	**Write Protect**. Implements hardware write protection in SPI.
$\overline{HOLD}$	Input	**$\overline{HOLD}$ Pin**. Suspends Serial Operation.
$\overline{HSB}$	Input/Output	**Hardware STORE Busy**: A weak internal pull up keeps this pin pulled high. If not used, this pin is left as No Connect. Output: Indicates busy status of nvSRAM when LOW. Input: Hardware STORE implemented by pulling this pin LOW externally.
V_{CAP}	Power Supply	**AutoStore Capacitor**. Supplies power to the nvSRAM during power loss to STORE data from the SRAM to nonvolatile elements. If AutoStore is not needed, this pin must be left as No Connect. It must never be connected to GND.
NC	No Connect	**No Connect**: This pin is not connected to the die.
GND	Power Supply	Ground
V_{CC}	Power Supply	Power Supply (2.7V to 3.6V)

Notes
1. $\overline{HSB}$ pin is not available in 8 DFN packages.
2. CY14B101Q1 part does not have V_{CAP} pin and does not support AutoStore.
3. CY14B101Q2 part does not have $\overline{WP}$ pin

Device Operation

CY14B101Q1/CY14B101Q2/CY14B101Q3 is 1 Mbit nvSRAM memory with a nonvolatile element in each memory cell. All the reads and writes to nvSRAM happen to the SRAM which gives nvSRAM the unique capability to handle infinite writes to the memory. The data in SRAM is secured by a STORE sequence which transfers the data in parallel to the nonvolatile Quantum Trap cells. A small capacitor (V_{CAP}) is used to AutoStore the SRAM data in nonvolatile cells when power goes down providing power down data security. The Quantum Trap nonvolatile elements built in the reliable SONOS technology make nvSRAM the ideal choice for secure data storage.

The 1 Mbit memory array is organized as 128K words x 8 bits. The memory can be accessed through a standard SPI interface that enables very high clock speeds upto 40 MHz with zero cycle delay read and write cycles. This device supports SPI modes 0 and 3 (CPOL, CPHA = 0, 0 and 1, 1) and operates as SPI slave. The device is enabled using the Chip Select pin ($\overline{CS}$) and accessed through Serial Input (SI), Serial Output (SO), and Serial Clock (SCK) pins.

This device provides the feature for hardware and software write protection through $\overline{WP}$ pin and WRDI instruction respectively along with mechanisms for block write protection (1/4, 1/2, or full array) using BP0 and BP1 pins in the status register. Further, the HOLD pin can be used to suspend any serial communication without resetting the serial sequence.

CY14B101Q1/CY14B101Q2/CY14B101Q3 uses the standard SPI opcodes for memory access. In addition to the general SPI instructions for read and write, it provides four special instructions which enable access to four nvSRAM specific functions: STORE, RECALL, AutoStore Disable (ASDISB), and AutoStore Enable (ASENB).

The major benefit of nvSRAM SPI over serial EEPROMs is that all reads and writes to nvSRAM are performed at the speed of SPI bus with zero delay. Therefore, no wait time is required after any of the memory accesses. The STORE and RECALL operations need finite time to complete and all memory accesses are inhibited during this time. While a STORE or RECALL operation is in progress, the busy status of the device is indicated by the Hardware STORE Busy ($\overline{HSB}$) pin and also reflected on the $\overline{RDY}$ bit of the Status Register.

The Device is available in three different pin configurations that enable the user to choose a part which fits in best in their application**.** The feature summary is given in Table 2.

Table 2. Feature Summary

Feature	CY14B101Q1	CY14B101Q2	CY14B101Q3
$\overline{WP}$	Yes	No	Yes
V_{CAP}	No	Yes	Yes
$\overline{HSB}$	No	No	Yes
AutoStore	No	Yes	Yes
Power Up RECALL	Yes	Yes	Yes
Hardware STORE	No	No	Yes
Software STORE	Yes	Yes	Yes

SRAM Write

All writes to nvSRAM are carried out on the SRAM and do not use up any endurance cycles of the nonvolatile memory. This enables user to perform infinite write operations. A Write cycle is performed through the SPI WRITE instruction. The WRITE instruction is issued through the SI pin of the nvSRAM and consists of the WRITE opcode, three bytes of address, and one byte of data. Write to nvSRAM is done at SPI bus speed with zero cycle delay.

The device allows burst mode writes to be performed through SPI. This enables write operations on consecutive addresses without issuing a new WRITE instruction. When the last address in memory is reached, the address rolls over to 0x0000 and the device continues to write.

The SPI write cycle sequence is defined explicitly in the Memory Access section of SPI Protocol Description.

SRAM Read

A read cycle is performed at the SPI bus speed and the data is read out with zero cycle delay after the READ instruction is performed. The READ instruction is issued through the SI pin of the nvSRAM and consists of the READ opcode and 3 bytes of address. The data is read out on the SO pin.

This device allows burst mode reads to be performed through SPI. This enables reads on consecutive addresses without issuing a new READ instruction. When the last address in memory is reached in burst mode read, the address rolls over to 0x0000 and the device continues to read.

The SPI read cycle sequence is defined explicitly in the Memory Access section of SPI Protocol Description.

STORE Operation

STORE operation transfers the data from the SRAM to the nonvolatile Quantum Trap cells. The device stores data to the nonvolatile cells using one of three STORE operations: AutoStore, activated on device power down; Software STORE, activated by a STORE instruction in the SPI; Hardware STORE, activated by the HSB. During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

The $\overline{HSB}$ signal or the $\overline{RDY}$ bit in the Status register can be monitored by the system to detect if a STORE cycle is in progress. The busy status of nvSRAM is indicated by HSB being pulled LOW or RDY bit being set to '1'. To avoid unnecessary nonvolatile STOREs, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place.

AutoStore Operation

The AutoStore operation is a unique feature of nvSRAM which automatically stores the SRAM data to QuantumTrap during power down. This Store mechanism is implemented using a capacitor (V_{CAP}) and enables the device to safely STORE the data in the nonvolatile memory when power goes down.

During normal operation, the device draws current from V_{CC} to charge the capacitor connected to the V_{CAP} pin. When the voltage on the V_{CC} pin drops below V_{SWITCH} during power down, the device inhibits all memory accesses to nvSRAM and automatically performs a conditional STORE operation using the charge from the V_{CAP} capacitor. The AutoStore operation is not initiated if no write cycle has been performed since last RECALL.

Note If a capacitor is not connected to V_{CAP} pin, Autostore must be disabled by issuing the AutoStore Disable instruction specified in AutoStore Disable (ASDISB) on page 13. If AutoStore is enabled without a capacitor on V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the Store. This may corrupt the data stored in nvSRAM and Status register. In such case, WRSR instruction needs to be issued to update the nonvolatile bits BP0, BP1, WPEN to resume normal functionality.

During power down, the memory accesses are inhibited after the voltage on V_{CC} pin drops below V_{SWITCH}. To avoid inadvertent writes, it must be ensured that $\overline{CS}$ is not left floating prior to this event. Therefore, during power down the device must be deselected and $\overline{CS}$ must be allowed to follow V_{CC}.

Figure 3 shows the proper connection of the storage capacitor (V_{CAP}) for AutoStore operation. Refer to DC Electrical Characteristics on page 14 for the size of the V_{CAP}.

Note CY14B101Q1 does not support AutoStore operation. The user must perform Software STORE operation by using the SPI STORE instruction to secure the data.

Software Store Operation

Software STORE enables the user to trigger a STORE operation through a special SPI instruction. This operation is initiated irrespective of whether a write has been performed since last nv operation.

A STORE cycle takes t_{STORE} to complete, during which all the memory accesses to nvSRAM are inhibited. The RDY bit of the Status register or the $\overline{HSB}$ pin may be polled to find the Ready or Busy status of the nvSRAM. After the t_{STORE} cycle time is completed, the SRAM is activated again for read and write operations.

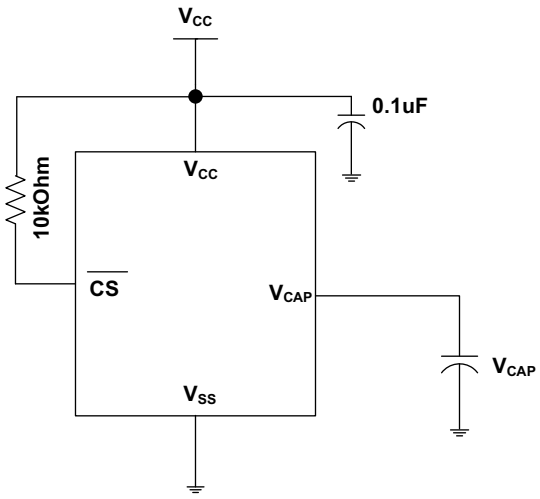
Hardware STORE and $\overline{HSB}$ pin Operation

The $\overline{HSB}$ pin in CY14B101Q3 is used to control and acknowledge STORE operations. If no STORE or RECALL is in progress, this pin can be used to request a Hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, nvSRAM conditionally initiates a STORE operation after t_{DELAY} duration. An actual STORE cycle starts only if a write to the SRAM has been performed since the last STORE or RECALL cycle. Reads and Writes to the memory are inhibited for t_{STORE} duration or as long as $\overline{HSB}$ pin is LOW.

The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, when a STORE cycle (initiated by any means) or Power up RECALL is in progress. Upon completion of the STORE operation, the nvSRAM remains disabled until the $\overline{HSB}$ pin returns HIGH. Leave the $\overline{HSB}$ pin unconnected if not used.

Note CY14B101Q1/CY14B101Q2 do not have HSB pin. $\overline{RDY}$ bit of the SPI status register may be probed to determine the Ready or Busy status of nvSRAM

Figure 3. AutoStore Mode



RECALL Operation

A RECALL operation transfers the data stored in the nonvolatile Quantum Trap elements to the SRAM. A RECALL may be initiated in two ways: Hardware RECALL, initiated on power up; and Software RECALL, initiated by a SPI RECALL instruction.

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared. Next, the nonvolatile information is transferred into the SRAM cells. All memory accesses are inhibited while a RECALL cycle is in progress. The RECALL operation does not alter the data in the nonvolatile elements.

Hardware Recall (Power Up)

During power up, when V_{CC} crosses V_{SWITCH}, an automatic RECALL sequence is initiated which transfers the content of nonvolatile memory on to the SRAM. The data would previously have been stored on the nonvolatile memory through a STORE sequence.

A Power Up Recall cycle takes t_{FA} time to complete and the memory access is disabled during this time. HSB pin can be used to detect the Ready status of the device. user

Software RECALL

Software RECALL enables the user to initiate a RECALL operation to restore the content of nonvolatile memory on to the SRAM. A Software RECALL is issued by using the SPI instruction for RECALL.

A Software RECALL takes t_{RECALL} to complete during which all memory accesses to nvSRAM are inhibited. The controller must provide sufficient delay for the RECALL operation to complete before issuing any memory access instructions.

Disabling and Enabling AutoStore

If the application does not require the AutoStore feature, it can be disabled by using the ASDISB instruction. If this is done, the nvSRAM does not perform a STORE operation at power down.

AutoStore can be re-enabled by using the ASENB instruction. However, these operations are not nonvolatile and if the user needs this setting to survive power cycle, a STORE operation must be performed following Autostore Disable or Enable operation.

Note CY14B101Q2/CY14B101Q3 has AutoStore Enabled from the factory. In CY14B101Q1, V_{CAP} pin is not present and AutoStore option is not available. The Autostore Enable and Disable instructions to CY14B101Q1 are ignored.

Note If AutoStore is disabled and V_{CAP} is not required, leave it open. V_{CAP} pin must never be connected to GND. Power Up Recall operation cannot be disabled in any case.

Serial Peripheral Interface

SPI Overview

The SPI is a four-pin interface with Chip Select ($\overline{CS}$), Serial Input (SI), Serial Output (SO) and Serial Clock (SCK) pins. CY14B101Q1/CY14B101Q2/CY14B101Q3 provides serial access to nvSRAM through SPI interface. The SPI bus on this device can run at speeds up to 40 MHz

The SPI is a synchronous serial interface which uses clock and data pins for memory access and supports multiple devices on the data bus. A device on SPI bus is activated using a chip select pin.

The relationship between chip select, clock, and data is dictated by the SPI mode. This device supports SPI modes 0 and 3. In both these modes, data is clocked into nvSRAM on rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active.

The SPI protocol is controlled by opcodes. These opcodes specify the commands from the bus master to the slave device. After $\overline{CS}$ is activated the first byte transferred from the bus master is the opcode. Following the opcode, any addresses and data are then transferred. The $\overline{CS}$ must go inactive after an operation is complete and before a new opcode can be issued. The commonly used terms used in SPI protocol are given below:

SPI Master

The SPI Master device controls the operations on a SPI bus. An SPI bus may have only one master with one or more slave devices. All the slaves share the same SPI bus lines and master may select any of the slave devices using the Chip Select pin. All the operations must be initiated by the master activating a slave device by pulling the $\overline{CS}$ pin of the slave LOW. The master also generates the Serial Clock (SCK) and all the data transmission on SI and SO lines are synchronized with this clock.

SPI Slave

SPI slave device is activated by the master through the Chip Select line. A slave device gets the Serial Clock (SCK) as an input from the SPI master and all the communication is synchronized with this clock. SPI slave never initiates a communication on the SPI bus and acts on the instruction from the master.

CY14B101Q1/CY14B101Q2/CY14B101Q3 operates as a SPI slave and may share the SPI bus with other SPI slave devices.

Chip Select ($\overline{CS}$)

For selecting any slave device, the master needs to pull down the corresponding $\overline{CS}$ pin. Any instruction can be issued to a slave device only while the $\overline{CS}$ pin is LOW. When the device is not selected, data through the SI pin is ignored and the serial output pin (SO) remains in a high impedance state.

Note A new instruction must begin with the falling edge of Chip Select ($\overline{CS}$). Therefore, only one opcode can be issued for each active Chip Select cycle.

Serial Clock (SCK)

Serial clock is generated by the SPI master and the communication is synchronized with this clock after $\overline{CS}$ goes LOW.

CY14B101Q1/CY14B101Q2/CY14B101Q3 enables SPI modes 0 and 3 for data communication. In both these modes, the inputs are latched by the slave device on the rising edge of SCK and outputs are issued on the falling edge. Therefore, the first rising edge of SCK signifies the arrival of first bit (MSB) of SPI instruction on the SI pin. Further, all data inputs and outputs are synchronized with SCK.

Data Transmission - SI and SO

SPI data bus consists of two lines, SI and SO, for serial data communication. The SI is also referred to as MOSI (Master Out Slave In) and SO is referred to as MISO (Master In Slave Out). The master issues instructions to the slave through the SI pin, while the slave responds through the SO pin. Multiple slave devices may share the SI and SO lines as described earlier.

Most Significant Bit (MSB)

The SPI protocol requires that the first bit to be transmitted is the Most Significant Bit (MSB). This is valid for both address and data transmission.

The 1 Mbit serial nvSRAM requires a 3-byte address for any read or write operation. However, since the actual address is only 17 bits, it implies that the first seven bits which are fed in are ignored by the device. Although these seven bits are ‘don’t care’, Cypress recommends that these bits are treated as 0s to enable seamless transition to higher memory densities.

Serial Opcode

After the slave device is selected with $\overline{CS}$ going LOW, the first byte received is treated as the opcode for the intended operation. CY14B101Q1/CY14B101Q2/CY14B101Q3 uses the standard opcodes for memory accesses. In addition to the memory accesses, it provides additional opcodes for the nvSRAM specific functions: STORE, RECALL, AutoStore Enable, and AutoStore Disable. Refer to Table 3 on page 8 for details.

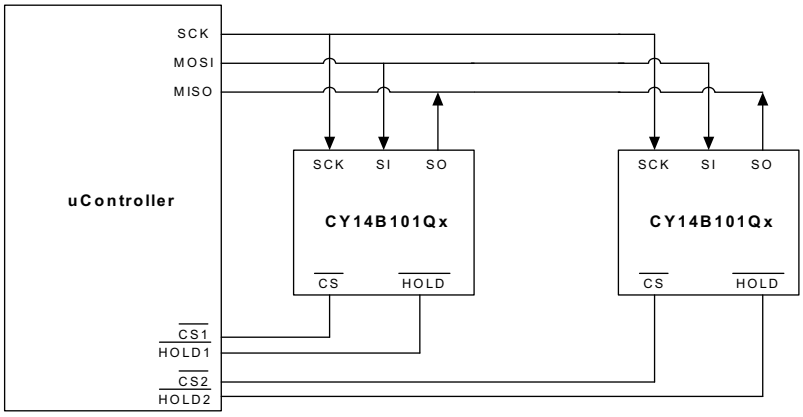
Invalid Opcode

If an invalid opcode is received, the opcode is ignored and the device ignores any additional serial data on the SI pin till the next falling edge of $\overline{CS}$ and the SO pin remains tristated.

Status Register

CY14B101Q1/CY14B101Q2/CY14B101Q3 has an 8-bit status register. The bits in the status register are used to configure the SPI bus. These bits are described in Table 5 on page 9.

Figure 4. System Configuration Using SPI nvSRAM



SPI Modes

CY14B101Q1/CY14B101Q2/CY14B101Q3 may be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

- SPI Mode 0 (CPOL=0, CPHA=0)
- SPI Mode 3 (CPOL=1, CPHA=1)

For both these modes, input data is latched-in on the rising edge of Serial Clock (SCK) starting from the first rising edge after CS goes active. If the clock starts from a HIGH state (in mode 3), the first rising edge, after the clock toggles, is considered. The output data is available on the falling edge of Serial Clock (SCK).

The two SPI modes are shown in Figure 5 and Figure 6. The status of clock when the bus master is in Standby mode and not transferring data is:

- SCK remains at 0 for Mode 0
- SCK remains at 1 for Mode 3

CPOL and CPHA bits must be set in the SPI controller for either Mode 0 or Mode 3. The device detects the SPI mode from the status of SCK pin when the device is selected by bringing the CS pin LOW. If SCK pin is LOW when device is selected, SPI Mode 0 is assumed and if SCK pin is HIGH, it works in SPI Mode 3.

Figure 5. SPI Mode 0

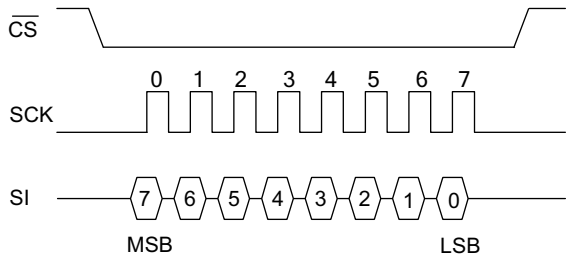
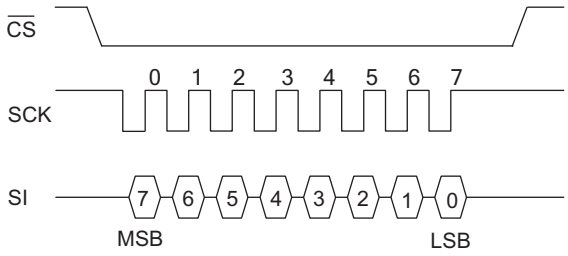


Figure 6. SPI Mode 3



SPI Operating Features

Power Up

Power up is defined as the condition when the power supply is turned on and V_{CC} crosses Vswitch voltage. During this time, the Chip Select (CS) must be allowed to follow the V_{CC} voltage. Therefore, CS must be connected to V_{CC} through a suitable pull up resistor. As a built-in safety feature, Chip Select (CS) is both edge sensitive and level sensitive. After power up, the device is not selected until a falling edge is detected on Chip Select (CS). This ensures that Chip Select (CS) must have been HIGH, before going Low to start the first operation.

As described earlier, nvSRAM performs a Power Up Recall operation after power up and therefore, all memory accesses are disabled for t_{RECALL} duration after power up. The HSB pin can be probed to check the ready or busy status of nvSRAM after power up.

Power On Reset

A Power On Reset (POR) circuit is included to prevent inadvertent writes. At power up, the device does not respond to any instruction until the V_{CC} reaches the Power On Reset threshold voltage (V_{SWITCH}). After V_{CC} transitions the POR threshold, the device is internally reset and performs an Power Up Recall operation. The device is in the following state after POR:

- Deselected (after Power up, a falling edge is required on Chip Select (CS) before any instructions are started).
- Standby power mode
- Not in the hold condition
- Status register state:
  - Write Enable (WEN) bit is reset to 0.
  - WPEN, BP1, BP0 unchanged from previous power down

The WPEN, BP1, and BP0 bits of the Status Register are nonvolatile bits and remain unchanged from the previous power down.

Before selecting and issuing instructions to the memory, a valid and stable V_{CC} voltage must be applied. This voltage must remain valid until the end of the transmission of the instruction.

Power Down

At power down (continuous decay of V_{CC}), when V_{CC} drops from the normal operating voltage and below the V_{SWITCH} threshold voltage, the device stops responding to any instruction sent to it. If a write cycle is in progress during power down, it is allowed t_{DELAY} time to complete after Vcc transitions below V_{SWITCH}, after which all memory accesses are inhibited and a conditional AutoStore operation is performed (AutoStore is not performed if no writes have happened since last RECALL cycle). This feature prevents inadvertent writes to nvSRAM from happening during power down.

However, to completely avoid the possibility of inadvertent writes during power down, ensure that the device is deselected and is in Standby Power Mode, and the Chip Select (CS) follows the voltage applied on V_{CC}.

Active Power and Standby Power Modes

When Chip Select (CS) is LOW, the device is selected, and is in the Active Power mode. The device consumes I_{CC} current, as specified in DC Electrical Characteristics on page 14. When Chip Select (CS) is HIGH, the device is deselected and the device goes into the Standby Power mode if a STORE or RECALL cycle is not in progress. If a STORE or RECALL cycle is in progress, device goes into the Standby Power Mode after the STORE or RECALL cycle is completed. In the Standby Power mode, the current drawn by the device drops to I_{SB}.

SPI Functional Description

The CY14B101Q1/CY14B101Q2/CY14B101Q3 uses an 8-bit instruction register. Instructions and their opcodes are listed in Table 3. All instructions, addresses, and data are transferred with the MSB first and start with a HIGH to LOW CS transition. There are, in all, 12 SPI instructions which provide access to most of the functions in nvSRAM. Further, the WP and HOLD pins provide additional functionality driven through hardware.

Table 3. Instruction Set

Instruction Category	Instruction Name	Opcode	Operation
Status Register Control Instructions	WREN	0000 0110	Set Write Enable Latch
	WRDI	0000 0100	Reset Write Enable Latch
	RDSR	0000 0101	Read Status Register
	WRSR	0000 0001	Write Status Register
SRAM Read/Write Instructions	READ	0000 0011	Read Data From Memory Array
	WRITE	0000 0010	Write Data To Memory Array
Special NV Instructions	STORE	0011 1100	Software STORE
	RECALL	0110 0000	Software RECALL
	ASENB	0101 1001	AutoStore Enable
	ASDISB	0001 1001	AutoStore Disable
Reserved	- Reserved -	0001 1110	Reserved for Internal use

The SPI instructions are divided based on their functionality in the following types:

- Status Register Access: WRSR and RDSR instructions
- Write Protection Functions: WREN and WRDI instructions along with WP pin and WEN, BP0, and BP1 bits
- SRAM memory Access: READ and WRITE instructions
- nvSRAM special instructions: STORE, RECALL, ASENB, and ASDISB

Status Register

The status register bits are listed in Table 3. The status register consists of Ready bit ($\overline{RDY}$) and data protection bits BP1, BP0, WEN, and WPEN. The $\overline{RDY}$ bit can be polled to check the Ready or Busy status while a nvSRAM STORE cycle is in progress. The status register can be modified by WRSR instruction and read by RDSR instruction. However, only WPEN, BP1, and BP0 bits of the Status Register can be modified by using WRSR instruction. WRSR instruction has no effect on WEN and $\overline{RDY}$ bits. The default value shipped from the factory for BP1, BP2 and WPEN bits is '0'.

Table 4. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN (0)	X	X	X	BP1 (0)	BP0 (0)	WEN	$\overline{RDY}$

Table 5. Status Register Bit Definition

Bit	Definition	Description
Bit 0 ($\overline{RDY}$)	Ready	Read Only bit indicates the ready status of device to perform a memory access. This bit is set to "1" by the device while a STORE or Software RECALL cycle is in progress.
Bit 1 (WEN)	Write Enable	WEN indicates if the device is write-enabled. Setting WEN = '1' enables writes and setting WEN = '0' disables all write operations
Bit 2 (BP0)	Block Protect bit '0'	Used for block protection. For details see Table 6 on page 10.
Bit 3 (BP1)	Block Protect bit '1'	Used for block protection. For details see Table 6 on page 10.
Bit 7 (WPEN)	Write Protect Enable bit	Used for enabling the function of Write Protect Pin ($\overline{WP}$). For details see Table 7 on page 11.

Read Status Register (RDSR) Instruction

The Read Status Register instruction provides access to the status register. This instruction is used to probe the Write Enable Status of the device or the Ready status of the device. $\overline{RDY}$ bit is set by the device to 1 whenever a STORE cycle is in progress. The Block Protection and WPEN bits indicate the extent of protection employed.

This instruction is issued after the falling edge of $\overline{CS}$ using the opcode for RDSR.

Write Status Register (WRSR) Instruction

The WRSR instruction enables the user to write to the Status register. However, this instruction cannot be used to modify bit 0 and bit 1 (WEN and $\overline{RDY}$). The BP0 and BP1 bits can be used to select one of four levels of block protection. Further, WPEN bit can be set to '1' to enable the use of Write Protect ($\overline{WP}$) pin.

WRSR instruction is a write instruction and needs writes to be enabled (WEN bit set to '1') using the WREN instruction before it is issued. The instruction is issued after the falling edge of $\overline{CS}$ using the opcode for WRSR followed by 8 bits of data to be stored in the Status Register. Since, only bits 2, 3, and 7 can be modified by WRSR instruction, it is recommended to leave the other bits as '0' while writing to the Status Register

Note In CY14B101Q1/CY14B101Q2/CY14B101Q3, the values written to Status Register are saved to nonvolatile memory only after a STORE operation. If AutoStore is disabled (or while using CY14B101Q1), any modifications to the Status Register must be secured by using a Software STORE operation

Note CY14B101Q2 does not have $\overline{WP}$ pin. Any modification to bit 7 of the Status register has no effect on the functionality of CY14B101Q2.

Figure 7. Read Status Register (RDSR) Instruction Timing

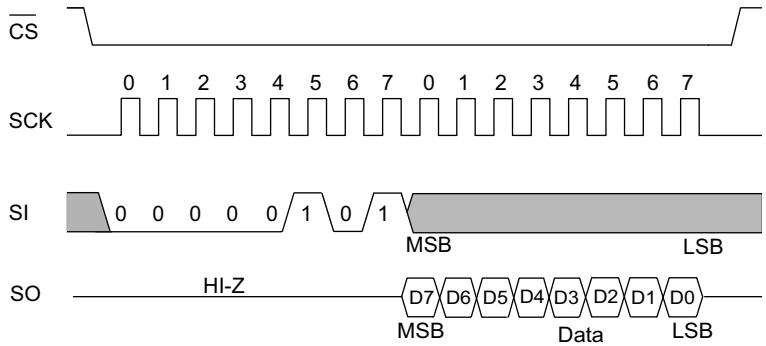
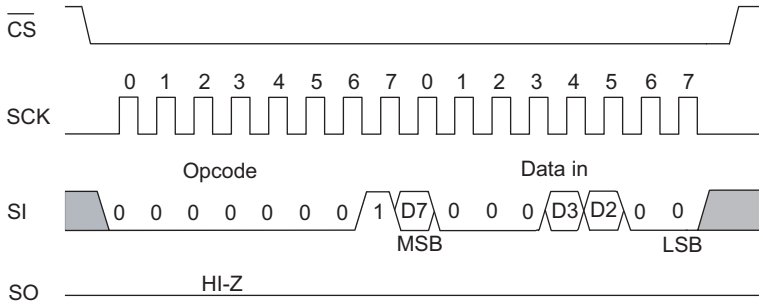


Figure 8. Write Status Register (WRSR) Instruction Timing



Write Protection and Block Protection

CY14B101Q1/CY14B101Q2/CY14B101Q3 provides features for both software and hardware write protection using WRDI instruction and WP. Additionally, this device also provides block protection mechanism through BP0 and BP1 pins of the Status Register.

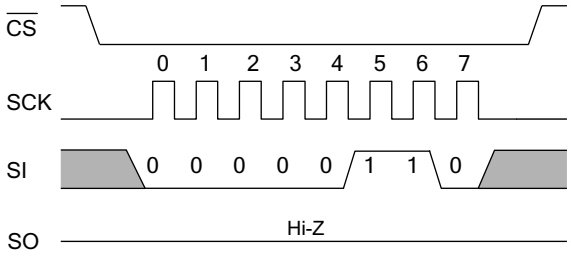
The write enable and disable status of the device is indicated by WEN bit of the status register. The write instructions (WRSR and WRITE) and nvSRAM special instruction (STORE, RECALL, ASENB, and ASDISB) need the write to be enabled (WEN bit = 1) before they can be issued.

Write Enable (WREN) Instruction

On power up, the device is always in the write disable state. The following WRITE, WRSR, or nvSRAM special instruction must therefore be preceded by a Write Enable instruction. If the device is not write enabled (WEN = '0'), it ignores the write instructions and returns to the standby state when CS is brought HIGH. A new CS falling edge is required to re-initiate serial communication. The instruction is issued following the falling edge of CS. When this instruction is used, the WEN bit of status register is set to '1'. WEN bit defaults to '0' on power up.

Note After completion of a write instruction (WRSR or WRITE) or nvSRAM special instruction (STORE, RECALL, ASENB, and ASDISB) instruction, WEN bit is cleared to '0'. This is done to provide protection from any inadvertent writes. Therefore, WREN instruction needs to be used before a new write instruction is issued.

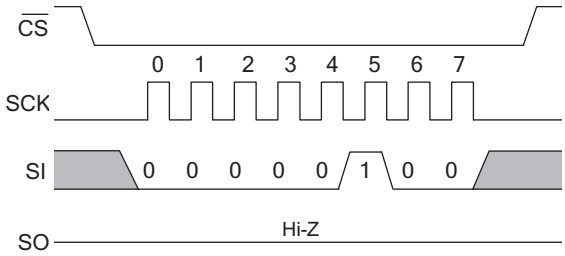
Figure 9. WREN Instruction



Write Disable (WRDI) Instruction

Write Disable instruction disables the write by clearing the WEN bit to '0' in order to protect the device against inadvertent writes. This instruction is issued following falling edge of CS followed by opcode for WRDI instruction. The WEN bit is cleared on the rising edge of CS following a WRDI instruction.

Figure 10. WRDI Instruction



Block Protection

Block protection is provided using the BP0 and BP1 pins of the Status register. These bits can be set using WRSR instruction and probed using the RDSR instruction. The nvSRAM is divided into four array segments. One-quarter, one-half, or all of the memory segments can be protected. Any data within the protected segment is read only. Table 6 shows the function of Block Protect bits.

Table 6. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected
	BP1	BP0	
0	0	0	None
1 (1/4)	0	1	0x18000-0x1FFFF
2 (1/2)	1	0	0x10000-0x1FFFF
3 (All)	1	1	0x00000-0x1FFFF

Write Protect ($\overline{WP}$) Pin

The write protect pin ($\overline{WP}$) is used to provide hardware write protection. $\overline{WP}$ pin enables all normal read and write operations when held HIGH. When the $\overline{WP}$ pin is brought LOW and WPEN bit is “1”, all write operations to the status register are inhibited. The hardware write protection function is blocked when the WPEN bit is “0”. This enables the user to install the device in a system with the $\overline{WP}$ pin tied to ground, and still write to the status register.

$\overline{WP}$ pin can be used along with WPEN and Block Protect bits (BP1 and BP0) of the status register to inhibit writes to memory. When $\overline{WP}$ pin is LOW and WPEN is set to “1”, any modifications to status register are disabled. Therefore, the memory is protected by setting the BP0 and BP1 bits and the $\overline{WP}$ pin inhibits any modification of the status register bits, providing hardware write protection.

Note $\overline{WP}$ going LOW when $\overline{CS}$ is still LOW has no effect on any of the ongoing write operations to the status register.

Note CY14B101Q2 does not have $\overline{WP}$ pin and therefore does not provide hardware write protection.

Table 7 summarizes all the protection features of this device

Table 7. Write Protection Operation

WPEN	$\overline{WP}$	WEN	Protected Blocks	Unprotected Blocks	Status Register
X	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	1	Protected	Writable	Protected
1	HIGH	1	Protected	Writable	Writable

Memory Access

All memory accesses are done using the READ and WRITE instructions. These instructions cannot be used while a STORE or RECALL cycle is in progress. A STORE cycle in progress is indicated by the RDY bit of the status register and the $\overline{HSB}$ pin.

Read Sequence (READ)

The read operations on this device are performed by giving the instruction on Serial Input pin (SI) and reading the output on Serial Output (SO) pin. The following sequence needs to be followed for a read operation: After the $\overline{CS}$ line is pulled LOW to select a device, the read opcode is transmitted through the SI line followed by three bytes of address. The Most Significant address byte contains A16 in bit 0 and other bits as ‘don’t cares’. Address bits A15 to A0 are sent in the following two address bytes. After the last address bit is transmitted on the SI pin, the data (D7-D0) at the specific address is shifted out on the SO line on the falling edge of SCK. Any other data on SI line after the last address bit is ignored.

CY14B101Q1/CY14B101Q2/CY14B101Q3 allows reads to be performed in bursts through SPI which can be used to read consecutive addresses without issuing a new READ instruction. If only one byte is to be read, the $\overline{CS}$ line must be driven HIGH after one byte of data comes out. However, the read sequence may be continued by holding the $\overline{CS}$ line LOW and the address is automatically incremented and data continues to shift out on SO pin. When the last data memory address (0x1FFFF) is reached, the address rolls over to 0x0000 and the device continues to read.

Write Sequence (WRITE)

The write operations on this device are performed through the Serial Input (SI) pin. To perform a write operation, if the device is write disabled, then the device must first be write enabled through the WREN instruction. When the writes are enabled ($\overline{WE}$N = ‘1’), WRITE instruction is issued after the falling edge of $\overline{CS}$. A WRITE instruction constitutes transmitting the WRITE opcode on SI line followed by 3 bytes address sequence and the data (D7-D0) which is to be written. The Most Significant address byte contains A16 in bit 0 with other bits being ‘don’t cares’. Address bits A15 to A0 are sent in the following two address bytes.

CY14B101Q1/CY14B101Q2/CY14B101Q3 enables writes to be performed in bursts through SPI which can be used to write consecutive addresses without issuing a new WRITE instruction. If only one byte is to be written, the $\overline{CS}$ line must be driven HIGH after the D0 (LSB of data) is transmitted. However, if more bytes are to be written, $\overline{CS}$ line must be held LOW and address is incremented automatically. The following bytes on the SI line are treated as data bytes and written in the successive addresses. When the last data memory address (0x1FFFF) is reached, the address rolls over to 0x0000 and the device continues to write. The WEN bit is reset to “0” on completion of a WRITE sequence.

Note When a burst write reaches a protected block address, it continues the address increment into the protected space but does not write any data to the protected memory. If the address roll over takes the burst write to unprotected space, it resumes writes. The same operation is true if a burst write is initiated within a write protected block.

Figure 11. Read Instruction Timing

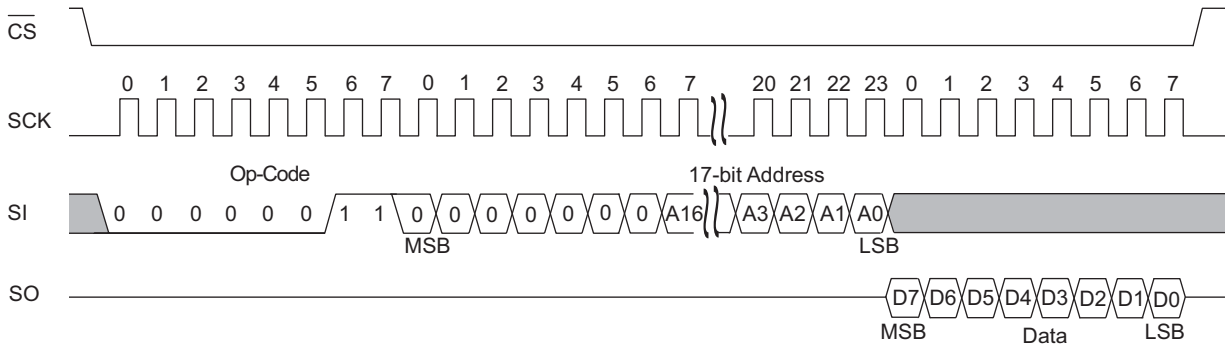


Figure 12. Burst Mode Read Instruction Timing

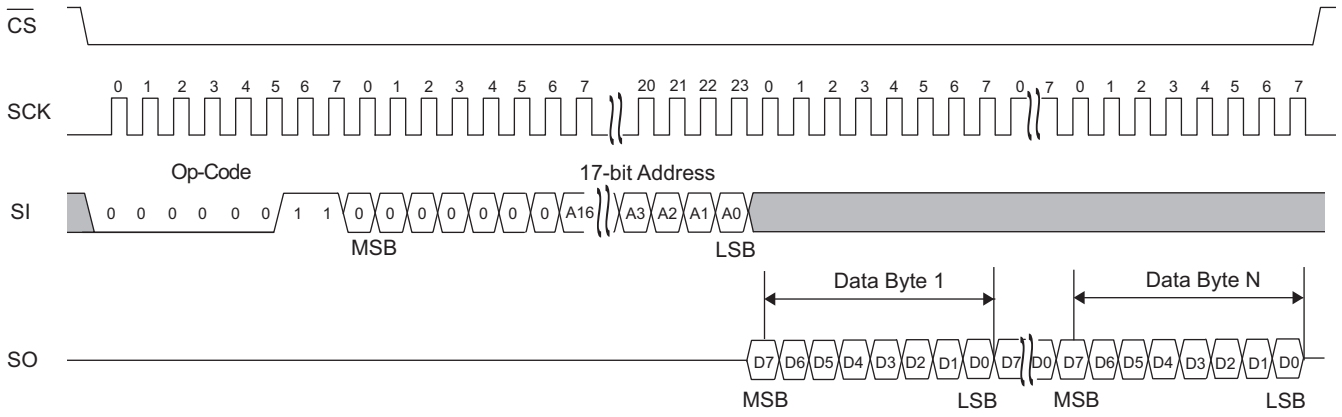


Figure 13. Write Instruction Timing

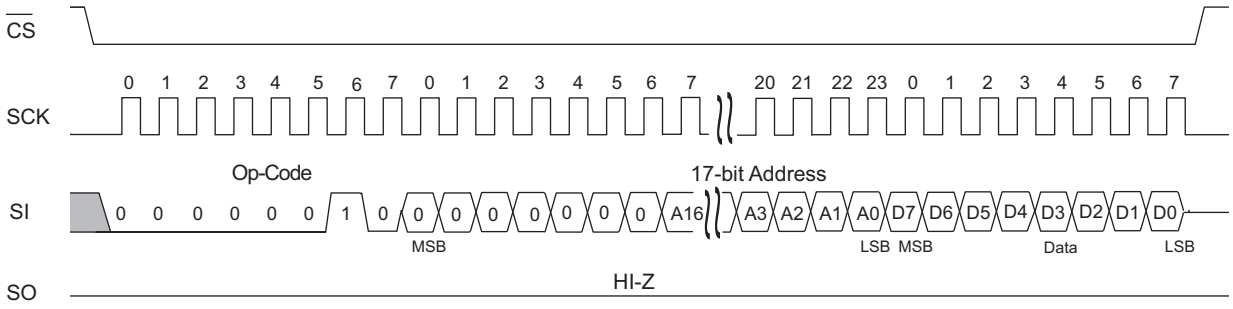
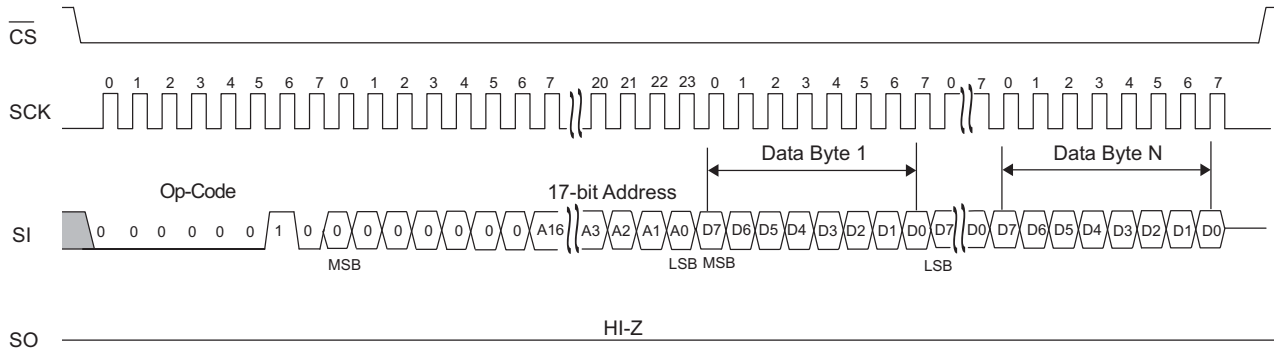


Figure 14. Burst Mode Write Instruction Timing



nvSRAM Special Instructions

CY14B101Q1/CY14B101Q2/CY14B101Q3 provides four special instructions which enables access to four nvSRAM specific functions: STORE, RECALL, ASDISB, and ASENB. Table 8 lists these instructions.

Software STORE

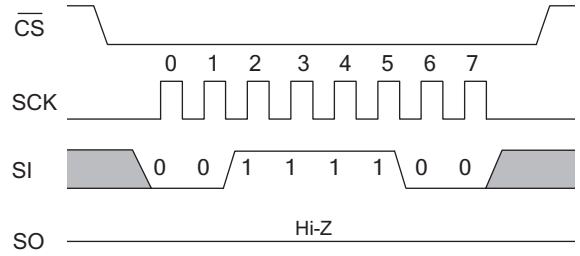
When a STORE instruction is executed, nvSRAM performs a Software STORE operation. The STORE operation is issued irrespective of whether a write has taken place since last STORE or RECALL operation.

Table 8. nvSRAM Special Instructions

Function Name	Opcode	Operation
STORE	0011 1100	Software STORE
RECALL	0110 0000	Software RECALL
ASENB	0101 1001	AutoStore Enable
ASDISB	0001 1001	AutoStore Disable

To issue this instruction, the device must be write enabled (WEN bit = '1'). The instruction is performed by transmitting the STORE opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the STORE instruction.

Figure 15. Software STORE Operation

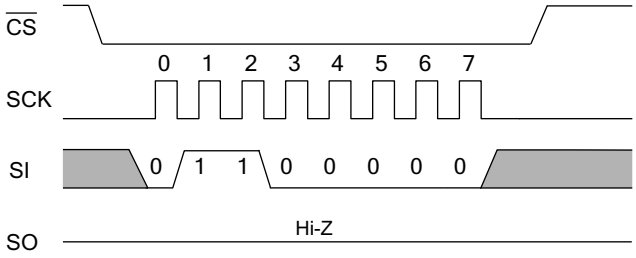


Software RECALL

When a RECALL instruction is executed, nvSRAM performs a Software RECALL operation. To issue this instruction, the device must be write enabled (WEN = '1').

The instruction is performed by transmitting the RECALL opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the RECALL instruction.

Figure 16. Software RECALL Operation

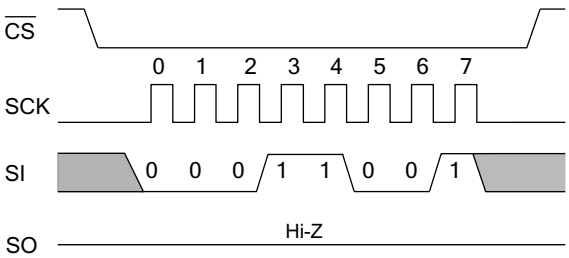


AutoStore Disable (ASDISB)

AutoStore is enabled by default in CY14B101Q2/CY14B101Q3. The ASDISB instruction disables the AutoStore. This setting is not nonvolatile and needs to be followed by a STORE sequence to survive the power cycle.

To issue this instruction, the device must be write enabled (WEN = '1'). The instruction is performed by transmitting the ASDISB opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the ASDISB instruction.

Figure 17. AutoStore Disable Operation



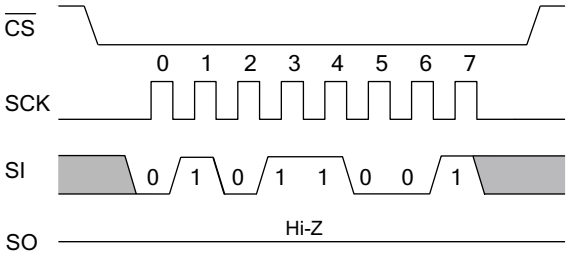
AutoStore Enable (ASENB)

The AutoStore Enable instruction enables the AutoStore on CY14B101Q1. This setting is not nonvolatile and needs to be followed by a STORE sequence to survive the power cycle.

To issue this instruction, the device must be write enabled (WEN = '1'). The instruction is performed by transmitting the ASENB opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the ASENB instruction.

Note If ASDISB and ASENB instructions are executed in CY14B101Q1, the device is busy for the duration of software sequence processing time (t_{SS}). However, ASDISB and ASENB instructions have no effect on CY14B101Q1 as AutoStore is internally disabled.

Figure 18. AutoStore Enable Operation

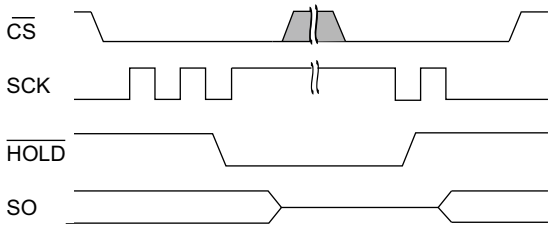


HOLD Pin Operation

The HOLD pin is used to pause the serial communication. When the device is selected and a serial sequence is underway, HOLD is used to pause the serial communication with the master device without resetting the ongoing serial sequence. To pause, the HOLD pin must be brought LOW when the SCK pin is LOW. To resume serial communication, the HOLD pin must be brought HIGH when the SCK pin is LOW (SCK may toggle during HOLD). While the device serial communication is paused, inputs to the SI pin are ignored and the SO pin is in the high impedance state.

This pin can be used by the master with the CS pin to pause the serial communication by bringing the pin HOLD LOW and deselecting an SPI slave to establish communication with another slave device, without the serial communication being reset. The communication may be resumed at a later point by selecting the device and setting the HOLD pin HIGH.

Figure 19. HOLD Operation



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature .....–65°C to +150°C

Maximum Accumulated Storage Time

At 150°C Ambient Temperature..... .....1000h

At 85°C Ambient Temperature..... ... 20 Years

Ambient Temperature with Power Applied.....–55°C to +150°C

Supply Voltage on V_{CC} Relative to GND.....–0.5V to +4.1V

DC Voltage Applied to Outputs in High-Z State .....–0.5V to V_{CC} + 0.5V

Input Voltage .....–0.5V to V_{CC} + 0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential.....–2.0V to V_{CC} + 2.0V

Package Power Dissipation Capability (T_A = 25°C).....1.0W

Surface Mount Lead Soldering Temperature (3 Seconds) .....+260°C

DC Output Current (1 output at a time, 1s duration).....15 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch up Current ..... > 200 mA

Table 9. Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	2.7V to 3.6V

DC Electrical Characteristics

Over the Operating Range (V_{CC} = 2.7V to 3.6V)

Parameter	Description	Test Conditions	Min	Typ[4]	Max	Unit
V_{CC}	Power Supply Voltage		2.7	3.0	3.6	V
I_{CC1}	Average V_{cc} Current	At f_{SCK} = 40 MHz. Values obtained without output loads (I_{OUT} = 0 mA)			10	mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Don't Care, V_{CC} = Max. Average current for duration t_{STORE}			10	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs Don't Care. Average current for duration t_{STORE}			5	mA
I_{SB}	V_{CC} Standby Current	$\overline{CS} \geq (V_{CC} - 0.2V)$. $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.			5	mA
I_{IX}[5]	Input Leakage Current (except HSB)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$	–1		+1	µA
	Input Leakage Current (for HSB)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$	–100		+1	µA
I_{OZ}	Off State Output Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{OUT} \leq V_{CC}$	–1		+1	µA
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		V_{SS} – 0.5		0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –2 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OUT} = 4 mA			0.4	V
V_{CAP}	Storage Capacitor	Between V_{CAP} pin and V_{SS}, 5V Rated	61	68	180	µF

Notes

4. Typical values are at 25°C, V_{CC}= V_{CC} (Typ). Not 100% tested.
5. The HSB pin has I_{OUT} = -2 uA for V_{OH} of 2.4V when both active high and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data Retention	20	Years
NV_C	Nonvolatile STORE Operations	1,000	K

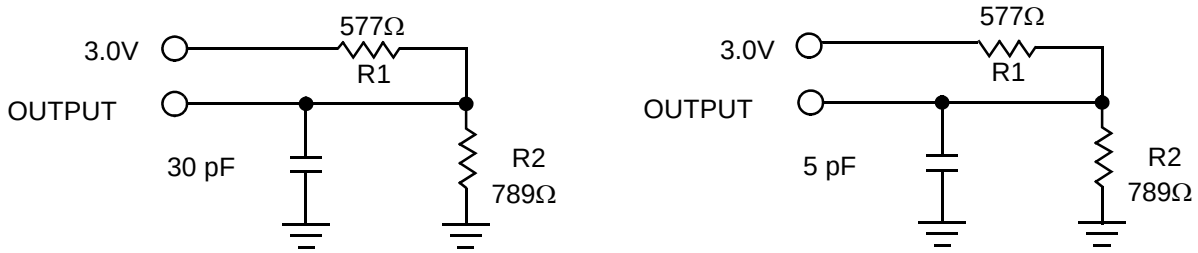
Capacitance

Parameter[6]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1MHz, V_{CC} = V_{CC} (Typ)	6	pF
C_{OUT}	Output Pin Capacitance		8	pF

Thermal Resistance

Parameter [6]	Description	Test Conditions	16-SOIC	8-DFN	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	55.17	17.7	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		2.64	18.8	°C/W

Figure 20. AC Test Loads and Waveforms



AC Test Conditions

Input Pulse Levels ..... 0V to 3V
Input Rise and Fall Times (10% - 90%) ..... ≤3 ns
Input and Output Timing Reference Levels 1.5V

Note
6. These parameters are guaranteed by design and are not tested.

AC Switching Characteristics

Cypress Parameter	Alt. Parameter	Description	40MHz		Unit
			Min	Max	
f_{SCK}	f_{SCK}	Clock Frequency, SCK		40	MHz
t_{CL}	t_{WL}	Clock Pulse Width Low	11		ns
t_{CH}	t_{WH}	Clock Pulse Width High	11		ns
t_{CS}	t_{CE}	CS High Time	20		ns
t_{CSS}	t_{CES}	CS Setup Time	10		ns
t_{CSH}	t_{CEH}	CS Hold Time	10		ns
t_{SD}	t_{SU}	Data In Setup Time	5		ns
t_{HD}	t_{H}	Data In Hold Time	5		ns
t_{HH}	t_{HD}	HOLD Hold Time	5		ns
t_{SH}	t_{CD}	HOLD Setup Time	5		ns
t_{CO}	t_{V}	Output Valid		9	ns
t_{HHZ}	t_{HZ}	HOLD to Output High Z		15	ns
t_{HLZ}	t_{LZ}	HOLD to Output Low Z		15	ns
t_{OH}	t_{HO}	Output Hold Time	0		ns
t_{HZCS}	t_{DIS}	Output Disable Time		25	ns

Figure 21. Synchronous Data Timing (Mode 0)

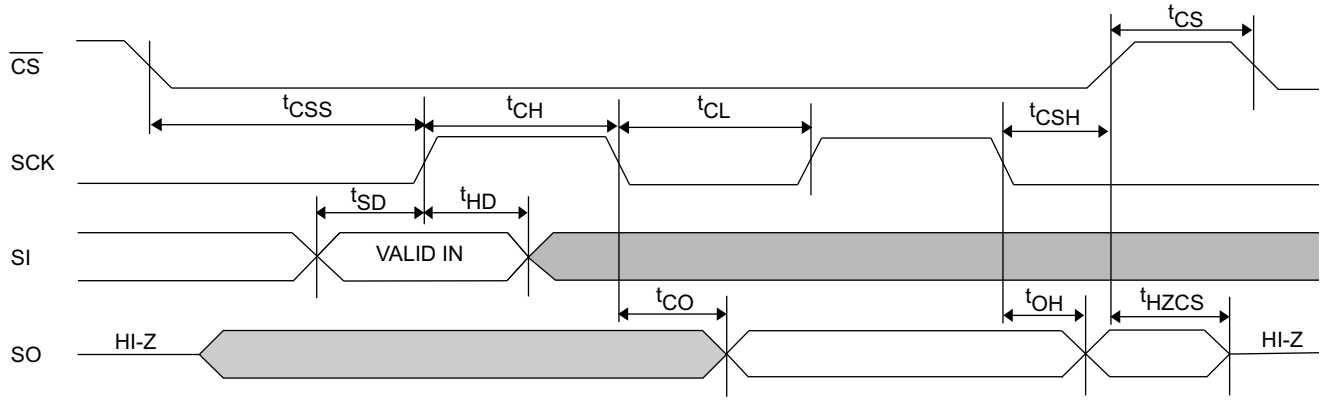
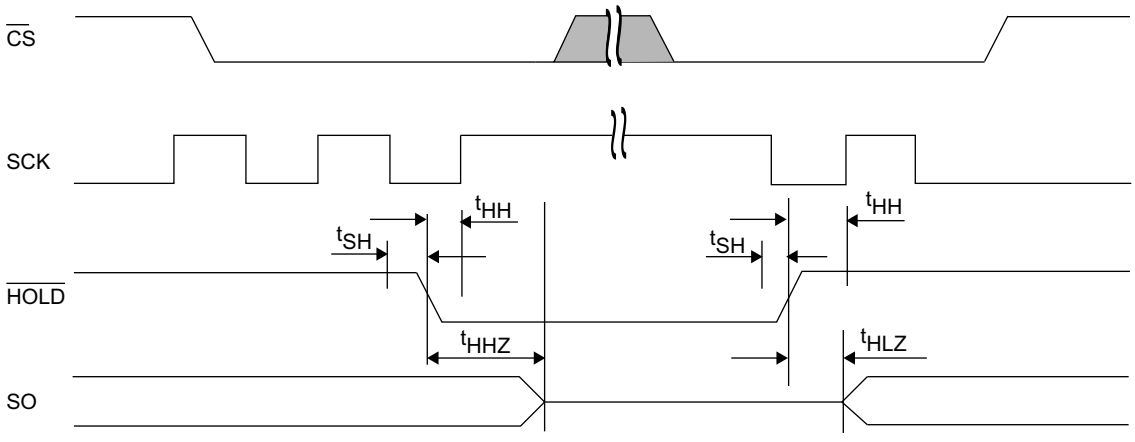


Figure 22. $\overline{\text{HOLD}}$ Timing

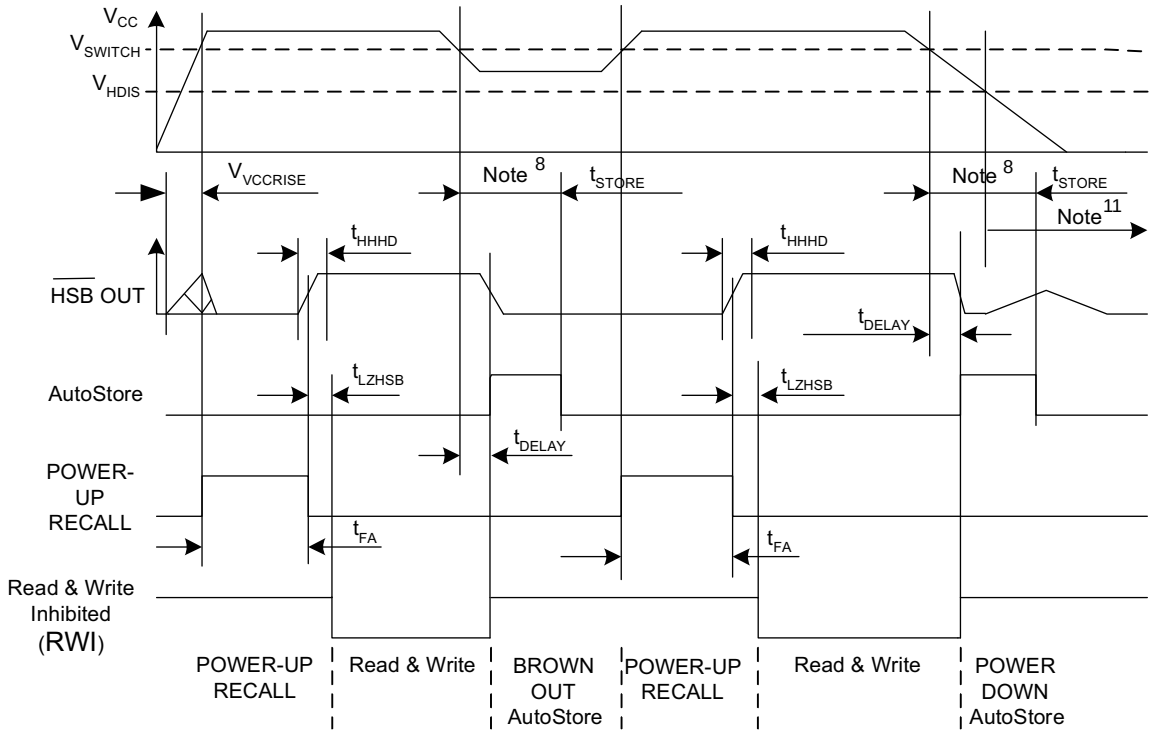


AutoStore or Power Up RECALL

Parameters	Description	CY14B101Q1/CY14B101Q2/ CY14B101Q3		Unit
		Min	Max	
t_{FA} [7]	Power Up RECALL Duration		20	ms
t_{STORE} [8]	STORE Cycle Duration		8	ms
t_{DELAY} [9]	Time Allowed to Complete SRAM Cycle		25	ns
V_{SWITCH}	Low Voltage Trigger Level		2.65	V
$t_{VCCRISE}$[6]	VCC Rise Time	150		µs
V_{HDIS}[6]	$\overline{HSB}$ Output Disable Voltage		1.9	V
t_{LZHSB}[6]	$\overline{HSB}$ To Output Active Time		5	µs
t_{HHHD}[6]	$\overline{HSB}$ High Active Time		500	ns

Switching Waveforms

Figure 23. AutoStore or Power Up RECALL[10]



Notes
7. t_{FA} starts from the time V_{CC} rises above V_{SWITCH}.
8. If an SRAM write has not taken place since the last nonvolatile cycle, AutoStore or Hardware Store is not initiated
9. On a Hardware STORE, Software Store / RECALL, AutoStore Enable / Disable and AutoStore initiation, SRAM operation continues to be enabled for time t_{DELAY}.
10. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
11. $\overline{HSB}$ pin is driven high to V_{CC} only by internal 100kOhm resistor, $\overline{HSB}$ driver is disabled.

Software Controlled STORE and RECALL Cycles

Parameter	Description	CY14B101Q1/CY14B101Q2/ CY14B101Q3		Unit
		Min	Max	
t_{RECALL}	RECALL Duration		200	µs
t_{SS} [12, 13]	Soft Sequence Processing Time		100	µs

Switching Waveforms

Figure 24. Software STORE Cycle[13]

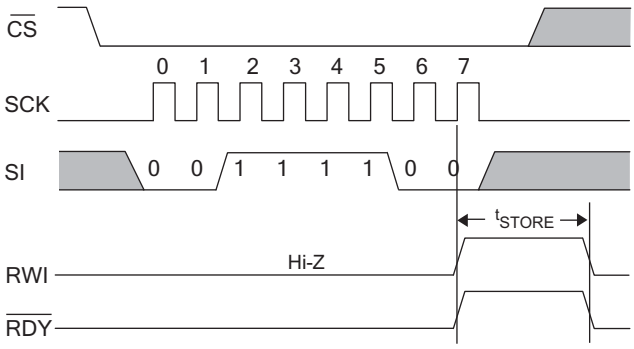
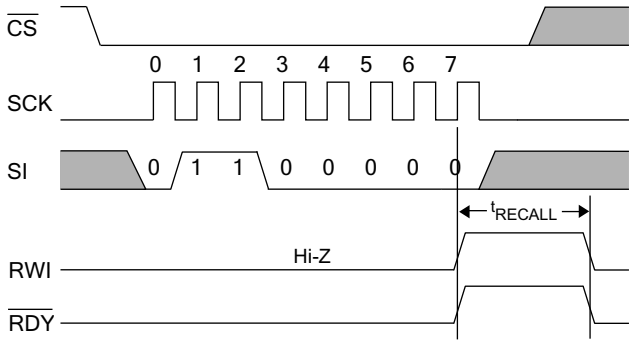


Figure 25. Software RECALL Cycle[13]



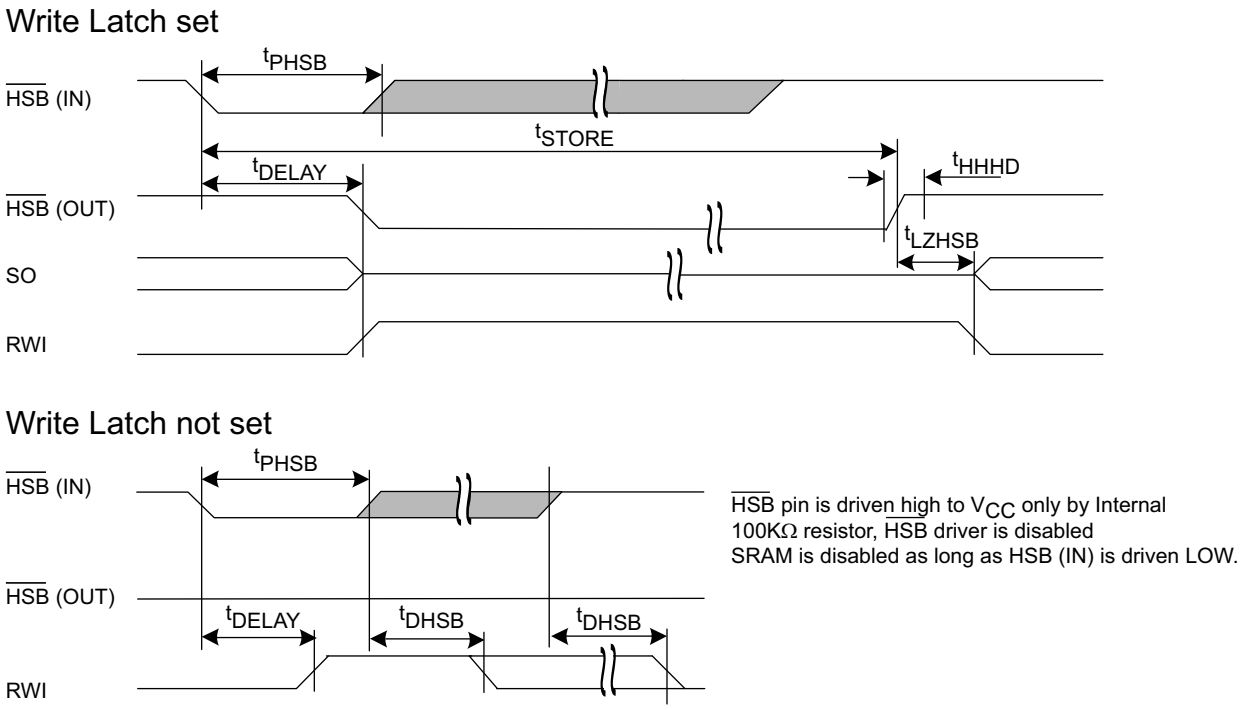
Notes
12. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
13. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.

Hardware STORE Cycle

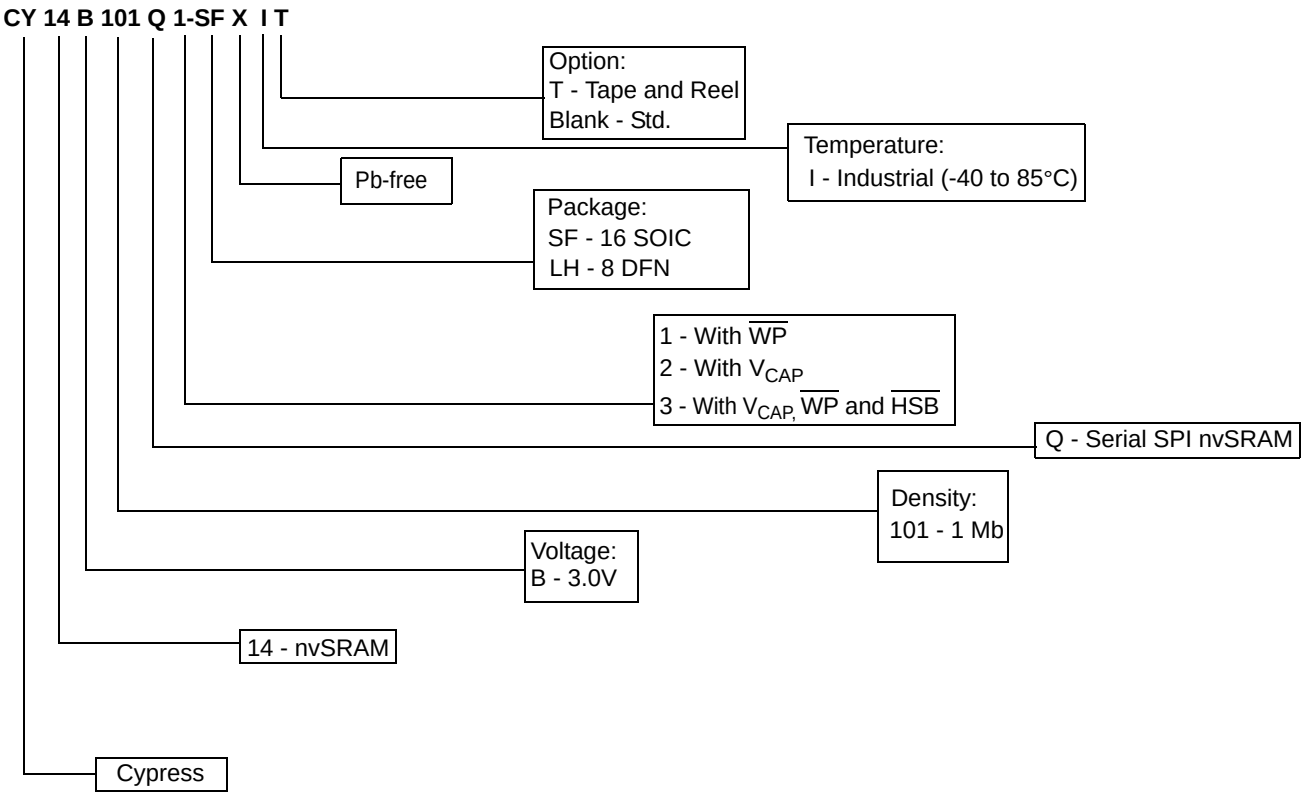
Parameter	Description	CY14B101Q3		Unit
		Min	Max	
t_{DHSB}	$\overline{HSB}$ To Output Active Time when write latch not set		25	ns
t_{PHSB}	Hardware STORE Pulse Width	15		ns

Switching Waveforms

Figure 26. Hardware STORE Cycle[8]



Part Numbering Nomenclature



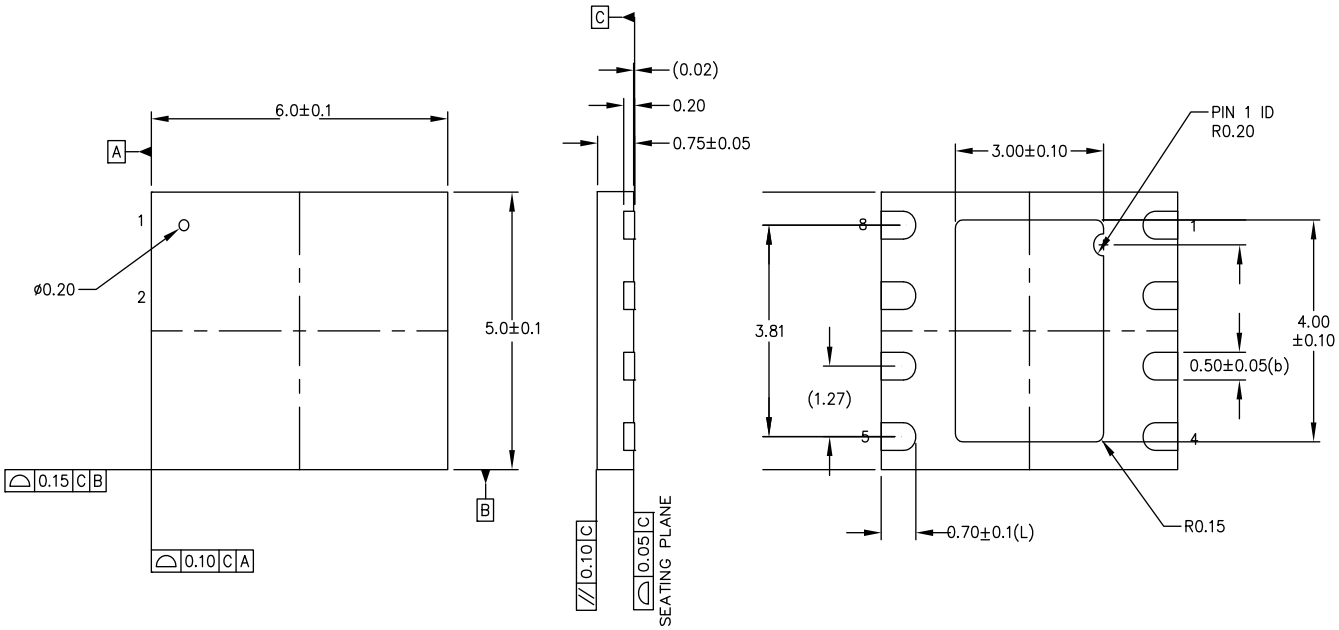
Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
CY14B101Q1-LHXIT	001-50671	8 DFN (With $\overline{WP}$)	Industrial
CY14B101Q1-LHXI	001-50671	8 DFN (With $\overline{WP}$)	
CY14B101Q2-LHXIT	001-50671	8 DFN (With V_{CAP})	
CY14B101Q2-LHXI	001-50671	8 DFN (With V_{CAP})	
CY14B101Q3-SFXIT	51-85022	16 SOIC (With V_{CAP}, $\overline{WP}$ and $\overline{HSB}$)	
CY14B101Q3-SFXI	51-85022	16 SOIC (With V_{CAP}, $\overline{WP}$ and $\overline{HSB}$)	

All the above parts are Pb-free.

Package Diagrams

Figure 27. 8-Pin (196 mil) DFN Package (001-50671)



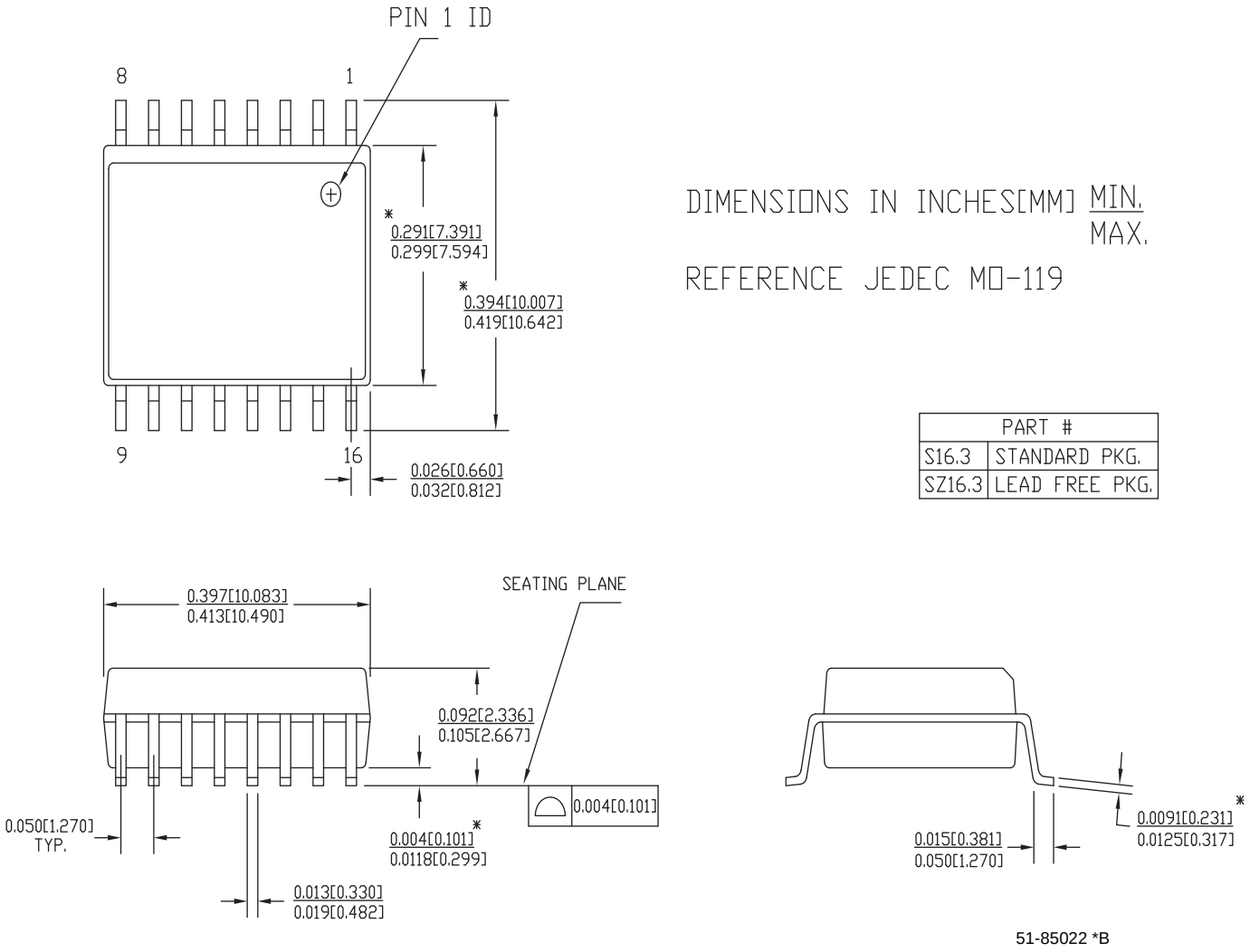
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. PACKAGE WEIGHT: TBD
3. BASED ON REF JEDEC # MO-240 EXCEPT DIMENSIONS (L) and (b)

001-50671 *A

Package Diagrams (continued)

Figure 28. 16-Pin (300 mil) SOIC (51-85022)



Document History Page

Document Title: CY14B101Q1/CY14B101Q2/CY14B101Q3 1 MBit (128K x 8) Serial SPI nvSRAM Document Number: 001-50091				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2607408	GSIN/ GVCH/AESA	12/19/08	New Datasheet
*A	2654487	GVCH/PYRS	02/04/2009	Moved from Advance information to Preliminary Changed part number from CY14B101QxA to CY14B101Qx Updated pin description of V_{CAP} pin Updated Device operation and SPI peripheral interface description Added Factory setting values for BP1, BP2 and WPEN bits Updated Real Time Clock operation description Changed I_{CC2} from 5mA to 10mA
*B	2733293	GVCH/AESA	07/08/2009	Corrected typo error in the Document History Page (Description of change) Corrected Typo error of footnote 2 and 3 Updated AutoStore operation description Updated test condition of I_{CC1} and I_{SB} parameter Updated V_{HDIS} parameter description
*C	2757348	08/28/2009	08/28/2009	Moved data sheet status from Preliminary to Final Removed commercial temperature related specs Added thermal resistance values for 16-SOIC and DFN package Added note to Write Sequence (WRITE) description
*D	2839453	GVCH/PYRS	01/06/10	Changed STORE cycles to QuantumTrap from 200K to 1 Million Updated Figure 3 Added Contents

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