



# Complete VGA Interface with EMI Suppression

MAX9511

## General Description

The MAX9511 is a complete solution to interface a video graphics controller to a VGA port and/or docking station with optimal video performance and minimal electromagnetic interference (EMI) emission. The MAX9511 has output drivers with variable EMI suppression for graphics video and sync (RGBHV) signals. The MAX9511 includes external load-detection circuitry.

The MAX9511 suppresses EMI emissions by limiting the slew rate (SR) rather than limiting bandwidth with fixed L-C filters. The SR controls the large-signal bandwidth without affecting the small-signal bandwidth, resulting in sharper video images, while reducing EMI. The SR of the MAX9511 provides tighter control than traditional passive L-C components, and allows the SR to track the resolution by varying an external resistor ( $R_{RX}$ ) rather than being fixed to a sub-optimal value.

The load-detection circuitry of the MAX9511 automatically detects and transmits a change in load status to the input stages when an external load (monitor, docking station, or projector) is connected. The MAX9511 is compatible with the load-detection circuitry on the digital-to-analog (DAC) outputs of most video graphics controllers. The output drivers provide 6dB of gain to compensate for the 75 $\Omega$  back-termination resistors, which reduce transmission line reflections.

The RGBHV channels can be placed into shutdown to reduce power when no external load is connected.

The MAX9511 operates from 3V and 5V supplies. The DDC circuitry performs bidirectional level translation from 3V to 5V logic levels. The MAX9511 is offered in a 24-pin QSOP package and is specified over the commercial 0°C to +70°C temperature range.

## Applications

- Notebook PCs (Laptops)
- Docking Stations
- Graphics Cards for Notebooks and Personal Computers
- Personal Computer Motherboards with On-Board Video Graphics Controllers
- Workstations

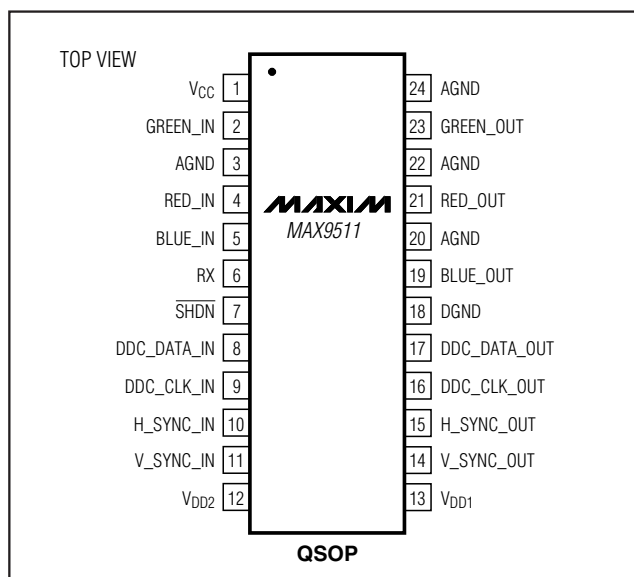
## Features

- ◆ RGB Drivers with Adjustable Slew Rate for EMI Control
- ◆ H Sync and V Sync Drivers with Level Translation
- ◆ Bidirectional Level Translators for DDC Support
- ◆ Simultaneously Drives External Monitor/Projector and Docking Station without Analog RGB Switches—No Stub Reflections
- ◆ Eliminates Up to 34 External Components
- ◆ Small 24-Pin QSOP Package

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9511CEG	0°C to +70°C	24 QSOP	E24-2

## Pin Configuration



# Complete VGA Interface with EMI Suppression

## ABSOLUTE MAXIMUM RATINGS

V<sub>CC</sub> to AGND .....-0.3V to +6V  
 V<sub>DD1</sub>, V<sub>DD2</sub> to DGND .....-0.3V to +6V  
 DGND to AGND .....-0.1V to +0.1V  
 RED\_IN, GREEN\_IN, BLUE\_IN to AGND .....-0.3V to (V<sub>CC</sub> + 0.3V)  
 RED\_OUT, GREEN\_OUT, BLUE\_OUT  
   to AGND .....-0.3V to (V<sub>CC</sub> + 0.3V)  
 RX to AGND .....-0.3V to (V<sub>CC</sub> + 0.3V)  
 H\_SYNC\_IN, V\_SYNC\_IN,  $\overline{\text{SHDN}}$   
   to DGND .....-0.3V to (V<sub>DD2</sub> + 0.3V)  
 H\_SYNC\_OUT, V\_SYNC\_OUT  
   to DGND .....-0.3V to (V<sub>DD1</sub> + 0.3V)  
 DDC\_DATA\_IN  
   to DGND .....(DDC\_DATA\_OUT - 0.3V) to (V<sub>DD2</sub> + 0.3V)

DDC\_DATA\_OUT  
   to DGND .....(DDC\_DATA\_IN - 0.1V) to (V<sub>DD1</sub> + 0.3V)  
 DDC\_CLK\_IN  
   to DGND .....(DDC\_CLK\_OUT - 0.3V) to (V<sub>DD2</sub> + 0.3V)  
 DDC\_CLK\_OUT  
   to DGND .....(DDC\_CLK\_IN - 0.1V) to (V<sub>DD1</sub> + 0.3V)  
 DDC\_DATA\_OUT to DDC\_DATA\_IN .....-0.1V to +6V  
 DDC\_CLK\_OUT to DDC\_CLK\_IN .....-0.1V to +6V  
 Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
   24-Pin QSOP (derate 9.5mW/°C above +70°C) .....762mW  
 Operating Temperature Range .....0°C to +70°C  
 Storage Temperature Range .....-65°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 5V, V<sub>DD1</sub> = 5V, V<sub>DD2</sub> =  $\overline{\text{SHDN}}$  = 3V, R<sub>L</sub> = 150 $\Omega$  to AGND, DGND = AGND, R<sub>RX</sub> = 7k $\Omega$  to AGND, T<sub>A</sub> = 0°C to +70°C. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V <sub>CC</sub>	Inferred from PSRR		4.5		5.5	V
	V <sub>DD1</sub>	Inferred from logic test		4.5		5.5	
	V <sub>DD2</sub>	Inferred from logic test		2.3		3.6	
Quiescent Supply Current	I <sub>CC</sub>	SHDN = V <sub>DD2</sub>	R <sub>RX</sub> = 7kΩ		38	50	mA
			R <sub>RX</sub> = 36kΩ		25	35	
		SHDN = DGND			0.15	0.25	
	I <sub>DD1</sub>	SHDN = V <sub>DD2</sub>			3	6	
		SHDN = DGND			0.027	0.08	
	I <sub>DD2</sub>	SHDN = V <sub>DD2</sub>			220	500	μA
		SHDN = DGND			26	40	
VIDEO							
Input Voltage Range	V <sub>IN</sub>	Inferred from voltage gain		0	0.7	0.9	V
Output Black Level Voltage	V <sub>OUT, BLACK</sub>	RED_IN = GREEN_IN = BLUE_IN = AGND		100	190	290	mV
Voltage Gain	A <sub>V</sub>	0 ≤ V <sub>IN</sub> ≤ 0.9V, R <sub>L</sub> = 75Ω		+1.9	+2	+2.1	V/V
Gain Matching	ΔA <sub>V</sub>	0 ≤ V <sub>IN</sub> ≤ 0.9V, R <sub>L</sub> = 75Ω			1	2	%
Input Resistance	R <sub>IN</sub>	0 ≤ V <sub>IN</sub> ≤ 1V, with load		0.02	60		MΩ
		0.4V ≤ V <sub>IN</sub> ≤ 0.7V, no load		-80	-72	-65	Ω
Output Short-Circuit Current (To AGND)	I <sub>OUT</sub>				40		mA
Load-Detection Voltage	V <sub>X, IN</sub>	(Note 1)				0.315	V
Output Load Detection	R <sub>L, OUT</sub>	V <sub>IN</sub> = 0.4V		200			Ω
Power-Supply Rejection	PSRR	4.5V ≤ V <sub>CC</sub> ≤ 5.5V, V <sub>IN</sub> = 0.5V		40	48		dB
Large-Signal Bandwidth		V <sub>OUT</sub> = 1.6V <sub>P-P</sub> , R <sub>RX</sub> = 7kΩ			370		MHz

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## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>CC</sub> = 5V, V<sub>DD1</sub> = 5V, V<sub>DD2</sub> =  $\overline{\text{SHDN}}$  = 3V, R<sub>L</sub> = 150 $\Omega$  to AGND, DGND = AGND, R<sub>RX</sub> = 7k $\Omega$  to AGND, T<sub>A</sub> = 0°C to +70°C. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate (Notes 2, 3)	SR	R <sub>RX</sub> = 36k $\Omega$ , T <sub>A</sub> = +25°C	250	330	450	V/ $\mu$ s
		R <sub>RX</sub> = 7k $\Omega$ , T <sub>A</sub> = +25°C	900	1100	1300	
Settling Time	t <sub>S</sub>	(Notes 4, 5)		0		ns
Undershoot/Overshoot	t <sub>OS</sub> , t <sub>US</sub>			$\pm 1$		%
Linearity Error	LE	V <sub>IN</sub> = 700mV <sub>P-P</sub> (Notes 6, 7)		0.036		%
Peak Signal-to-Noise Ratio	SNR	f = 100kHz to 100MHz, V <sub>IN</sub> = 700mV <sub>P-P</sub>		50		dB
Channel-to-Channel Skew	$\Delta t$	R to G to B (Note 3)		500	1100	ps
Power-Supply Rejection Ratio	PSRR	f = 100kHz		49		dB
Crosstalk		All hostile, f = 10MHz		55		dB
Input Termination Switch Delay	$\Delta t_{\text{SWD}}$			70		ns
<b>LOGIC</b>						
Input Low Level	V <sub>IL</sub>	H_SYNC_IN, V_SYNC_IN and $\overline{\text{SHDN}}$			0.3 x V <sub>DD2</sub>	V
Input High Level	V <sub>IH</sub>	H_SYNC_IN, V_SYNC_IN and $\overline{\text{SHDN}}$	0.7 x V <sub>DD2</sub>			V
Output Low Level	V <sub>OL</sub>	I <sub>OL</sub> = 4mA H_SYNC_OUT, V <sub>H_SYNC_IN</sub> = DGND V_SYNC_OUT, V <sub>V_SYNC_IN</sub> = DGND			0.55	V
		I <sub>OL</sub> = 50 $\mu$ A DDC_DATA_IN, V <sub>DDC_DATA_OUT</sub> = DGND DDC_CLK_IN, V <sub>DDC_CLK_OUT</sub> = DGND			0.4	
		I <sub>OL</sub> = 3mA DDC_DATA_OUT, V <sub>DDC_DATA_IN</sub> = DGND DDC_CLK_OUT, V <sub>DDC_CLK_IN</sub> = DGND			0.5	
Output High Level	V <sub>OH</sub>	I <sub>OH</sub> = 4mA H_SYNC_OUT, V <sub>H_SYNC_IN</sub> = V <sub>DD2</sub> V_SYNC_OUT, V <sub>V_SYNC_IN</sub> = V <sub>DD2</sub>			V <sub>DD1</sub> - 1.5	V
		I <sub>OH</sub> = 50 $\mu$ A DDC_DATA_IN, V <sub>DDC_DATA_OUT</sub> = V <sub>DD1</sub> DDC_CLK_IN, V <sub>DDC_CLK_OUT</sub> = V <sub>DD1</sub>			V <sub>DD2</sub> - 0.4	
		I <sub>OH</sub> = 50 $\mu$ A DDC_DATA_OUT, V <sub>DDC_DATA_IN</sub> = V <sub>DD2</sub> DDC_CLK_OUT, V <sub>DDC_CLK_IN</sub> = V <sub>DD2</sub>			V <sub>DD1</sub> - 1.5	
SYNC Output Resistance	R <sub>SO</sub>		35	55	85	$\Omega$
$\overline{\text{SHDN}}$ Pulldown Resistance	R <sub>SD</sub>		250	330	500	k $\Omega$
SYNC Input Resistance	R <sub>SI</sub>		30	47	65	k $\Omega$
DDC Pullup Resistance	R <sub>PO</sub>	DDC_DATA_OUT, DDC_CLK_OUT	2	3	4	k $\Omega$
	R <sub>PI</sub>	DDC_DATA_IN, DDC_CLK_IN	3.0	4.7	6.5	

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = 5V$ ,  $V_{DD1} = 5V$ ,  $V_{DD2} = \overline{SHDN} = 3V$ ,  $R_L = 150\Omega$  to AGND, DGND = AGND,  $R_{RX} = 7k\Omega$  to AGND,  $T_A = 0^\circ C$  to  $+70^\circ C$ . Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise/Fall Time	$t_R/t_F$	All SYNC outputs (Notes 2, 3)	$C_{SYNC} = 47pF$ , $T_A = +25^\circ C$		7	ns
			$C_{SYNC} = 470pF$ , $T_A = +25^\circ C$		50 70 100	
		DDC only, $C_L = 47pF$			400	
Propagation Delay	$t_{PLH}$ , $t_{PHL}$	SYNC, $C_{SYNC} = 47pF$ , $T_A = +25^\circ C$ (Notes 3, 8)		12	22	ns
Enable Time		$V_{IN} = 0.7V_{P-P}$ , $\overline{SHDN}$ from DGND to $V_{DD2}$ , outputs settle to $\pm 1\%$ of final value		1200		ns
Disable Time		$V_{IN} = 0.7V_{P-P}$ , $\overline{SHDN}$ from $V_{DD2}$ to DGND, outputs settle to $\pm 1\%$ of final value		400		ns

**Note 1:** This is the voltage at which the input termination switches;  $V_{IN} > V_{X\_IN}$  = switch open,  $V_{IN} < V_{X\_IN}$  = switch closed.

**Note 2:** Measured between the 10% to 90% points on rising or falling edge.

**Note 3:** Not production tested. Guaranteed by design.

**Note 4:** Measured from the END of overshoot/undershoot to  $\pm 5\%$  of final value.

**Note 5:**  $V_{IN} = 700mV$  with a rise time  $> 1ns$ .

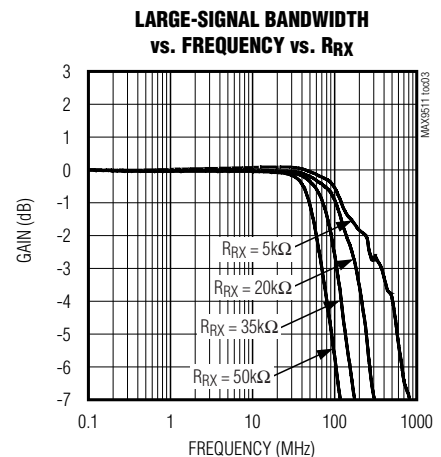
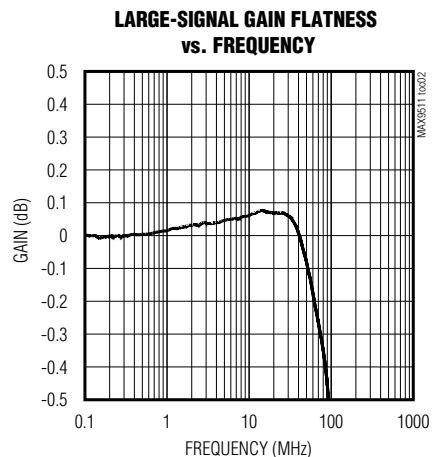
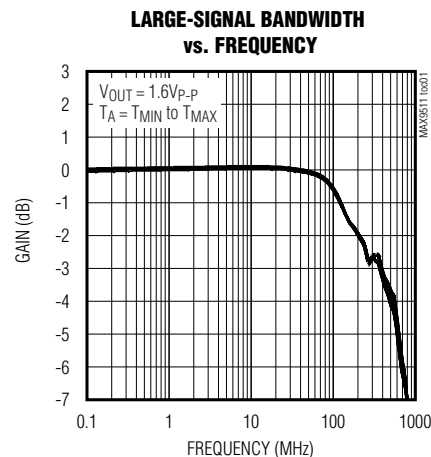
**Note 6:** Linearity error is the maximum difference between the actual and measured output of a video ramp. Done in accordance with VESA Test Procedure, Version 1, 6/11/2001.

**Note 7:** Linearity error measured as percentage of full scale.

**Note 8:** Propagation delay is the time difference between the  $V_{DD2}/2$  input crossing and the 1.4V output crossing.

## Typical Operating Characteristics

( $V_{CC} = 5V$ ,  $V_{DD1} = 5V$ ,  $V_{DD2} = 3V$ ,  $R_L = 150\Omega$  to AGND,  $R_{RX} = 7k\Omega$  to AGND,  $T_A = +25^\circ C$ , unless otherwise noted.)

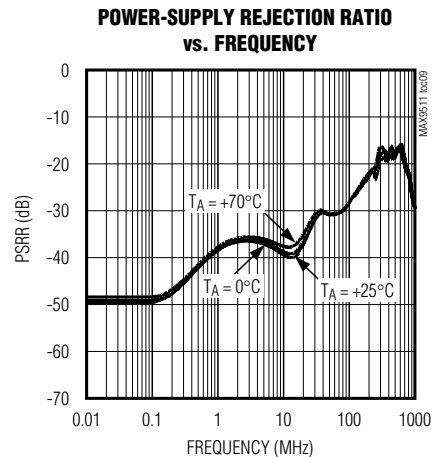
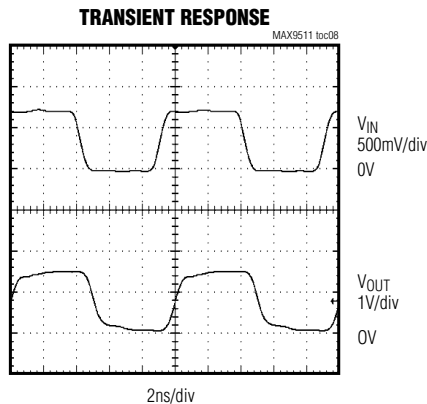
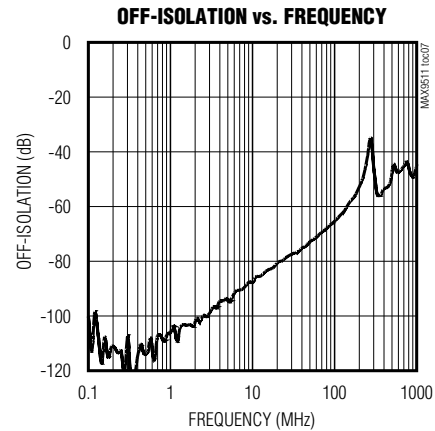
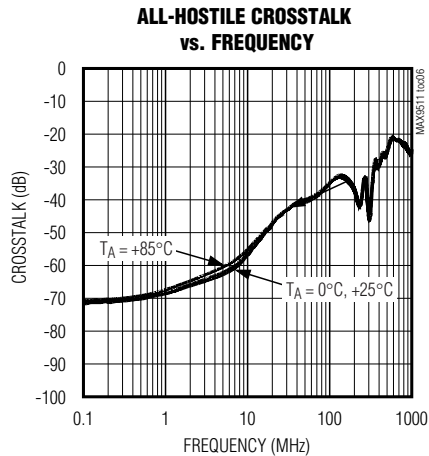
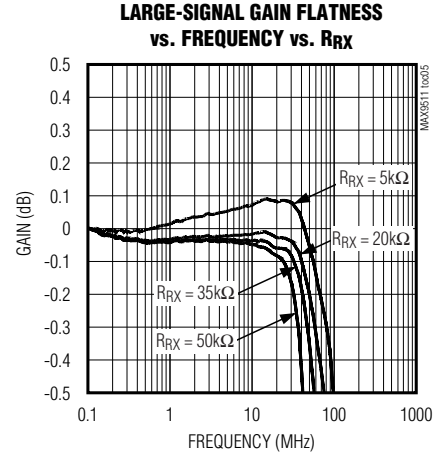
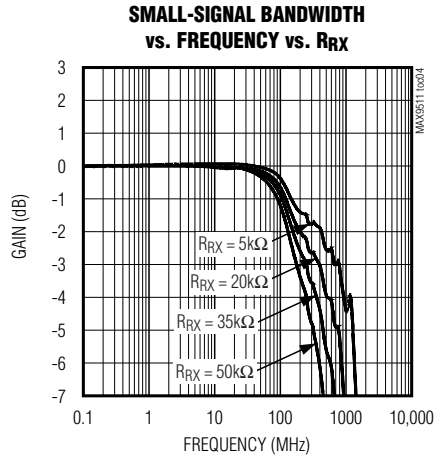


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## Typical Operating Characteristics (continued)

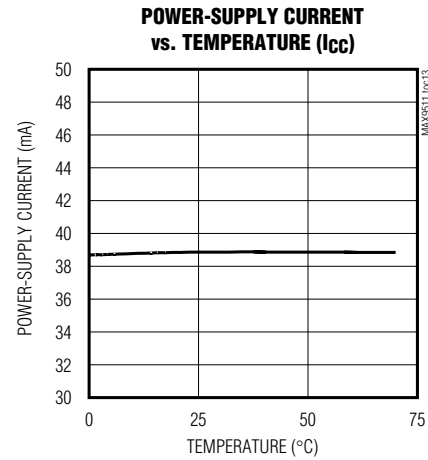
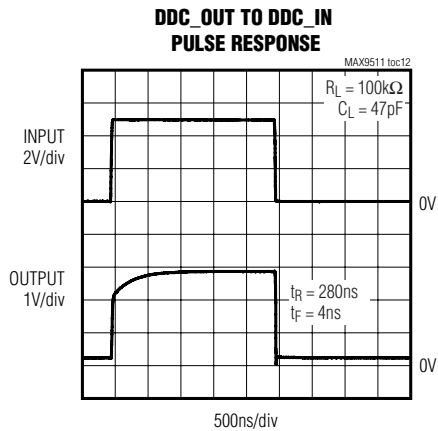
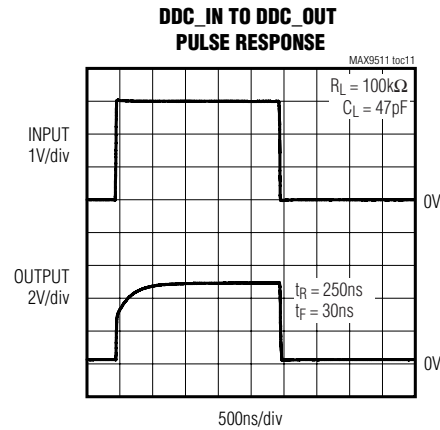
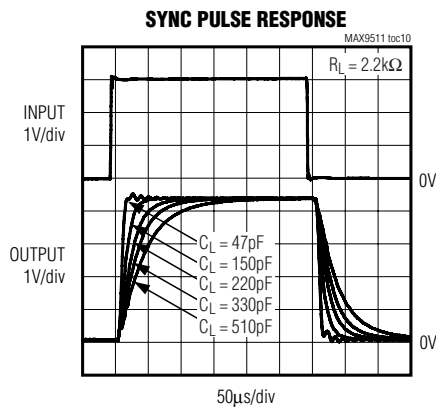
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# Complete VGA Interface with EMI Suppression

## Typical Operating Characteristics (continued)

( $V_{CC} = 5V$ ,  $V_{DD1} = 5V$ ,  $V_{DD2} = 3V$ ,  $R_L = 150\Omega$  to AGND,  $R_{RX} = 7k\Omega$  to AGND,  $T_A = +25^\circ C$ , unless otherwise noted.)

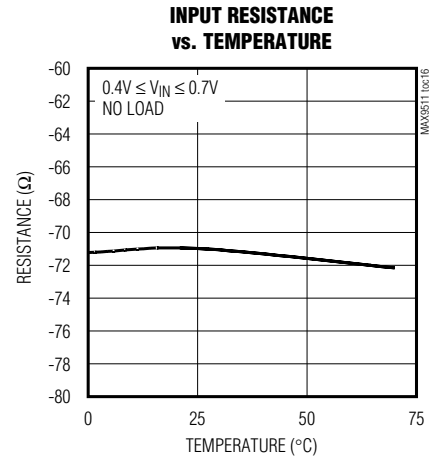
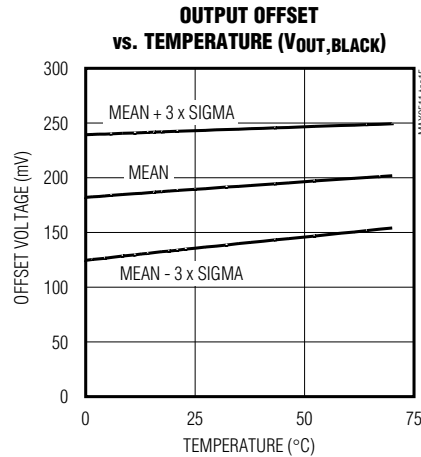
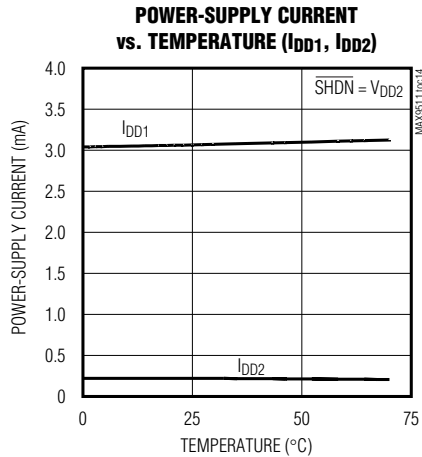


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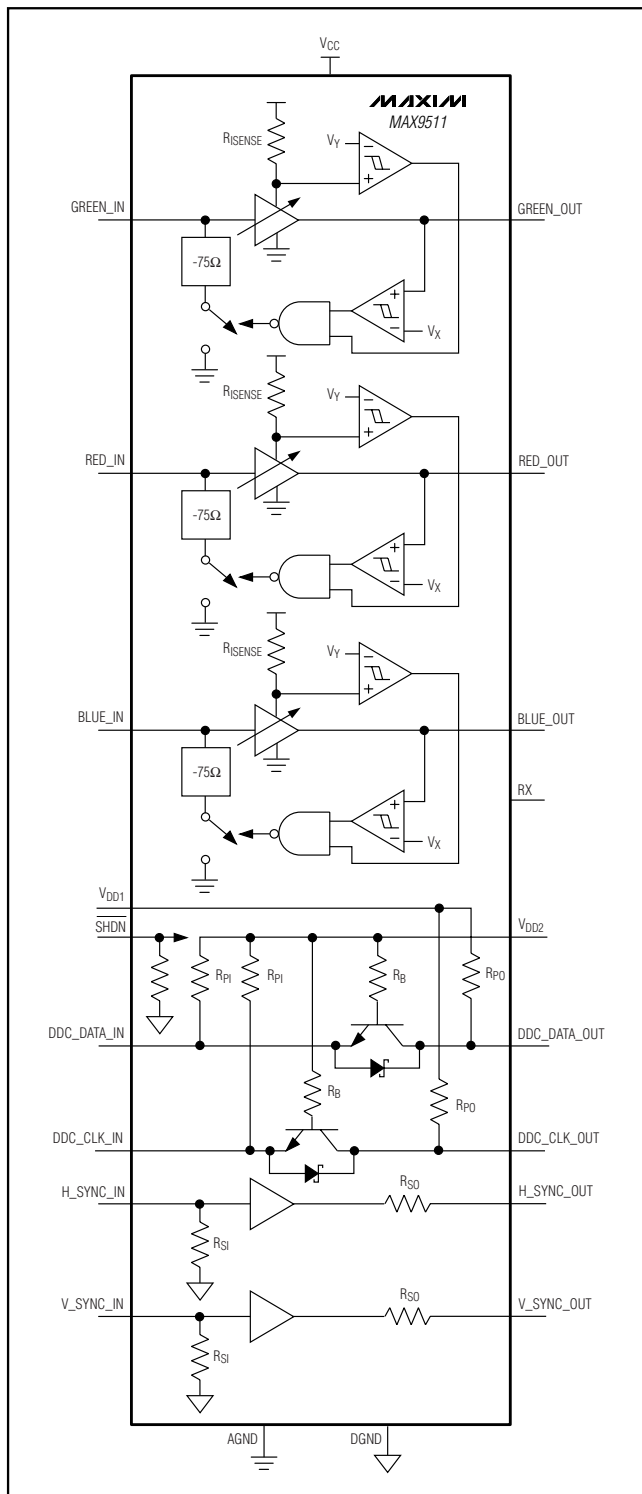


## Pin Description

PIN	NAME	FUNCTION
1	$V_{CC}$	Analog Power Supply
2	GREEN_IN	Green Video Input
3, 20, 22, 24	AGND	Analog Ground
4	RED_IN	Red Video Input
5	BLUE_IN	Blue Video Input
6	RX	Slew-Rate Control. Connect an external resistor from RX to AGND.
7	$\overline{SHDN}$	Active-Low Shutdown. For normal operation connect to $V_{DD2}$ . $\overline{SHDN}$ is internally pulled to DGND.
8	DDC_DATA_IN	DDC Data Input. Defaults to $V_{DD2}$ through an internal pullup resistor.
9	DDC_CLK_IN	DDC Clock Input. Defaults to $V_{DD2}$ through an internal pullup resistor.
10	H_SYNC_IN	Horizontal SYNC Input. Defaults to AGND through an internal pulldown resistor.
11	V_SYNC_IN	Vertical SYNC Input. Defaults to AGND through an internal pulldown resistor.
12	$V_{DD2}$	SYNC/DDC 3V Supply
13	$V_{DD1}$	SYNC/DDC 5V Supply. Supplies 5V to SYNC and DDC output circuitry.
14	V_SYNC_OUT	Vertical Sync Output
15	H_SYNC_OUT	Horizontal Sync Output
16	DDC_CLK_OUT	DDC Clock Output. Defaults to $V_{DD1}$ through an internal pullup resistor.
17	DDC_DATA_OUT	DDC Data Output. Defaults to $V_{DD1}$ through an internal pullup resistor.
18	DGND	Digital Ground
19	BLUE_OUT	Blue Video Output
21	RED_OUT	Red Video Output
23	GREEN_OUT	Green Video Output

# Complete VGA Interface with EMI Suppression

## Block Diagram



## Detailed Description

The MAX9511 solves several difficult problems in interfacing a video graphics controller to a VGA port and/or the docking station connector. First, there is a trade-off between video quality and EMI. The usual method for reducing EMI is to insert a fixed-frequency LC  $\pi$ -filter between the video DAC output and the connector. Given the large component variation of the capacitors and inductors, the frequency response is sharply reduced to meet EMI requirements. As a result, video quality suffers making sharp transitions in the video soft. The MAX9511 video drivers have a variable slew rate, which limits electromagnetic emissions and can be adjusted by an external resistor. As a result, the slew rate of the MAX9511 can be varied to reduce electromagnetic emissions at a given resolution, maximizing video quality. Since the slew rate is variable and set by a resistor instead of fixed by capacitors and inductors, video performance and electromagnetic emissions are consistent during production.

The MAX9511 also has horizontal and vertical sync output drivers, bidirectional level translators for DDC support, and external load-detection circuits that correctly transfer information about the external load to the video graphics controller.

### Load Detection

Most notebook computers implement a power-saving load-detection circuit that disables the external monitor output when no monitor is plugged into the rear panel VGA connector as shown in Figure 1. Upon startup or on command, the video controller generates a sequence of detection pulses out of the current DAC shown, that results in an output voltage of above 315mV when an external monitor ( $R_L$ ) is connected, and above 630mV when disconnected. If the monitor is disconnected at the time of the pulse, the comparator inside the notebook trips and disables the video. When the monitor is plugged in, the resulting pulse will not trip the comparator and the video is enabled.

If the lowpass filter is simply replaced with an amplifier, the monitor termination  $R_L$  is isolated from the video controller and the conventional load-detection scheme does not work.

For this reason, the MAX9511 includes the load-detection circuit. When  $R_L$  is connected (i.e., the monitor is plugged in) to the output of the MAX9511, the internal load-detection circuit disconnects the synthesized  $-75\Omega$  resistor from the input. The resulting  $37.5\Omega$  resistance at the DAC output indicates to the DAC's internal load-detection circuit that the monitor is plugged in. Removing  $R_L$  (i.e., disconnecting the monitor) causes the MAX9511's load-detection circuit to connect the synthesized  $-75\Omega$



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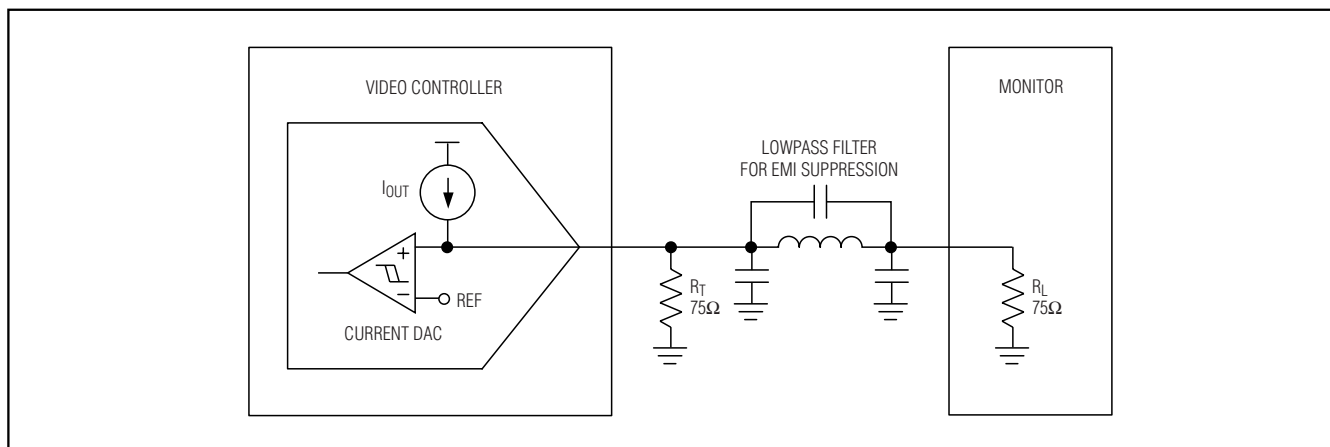


Figure 1. Conventional Load-Detection Scheme

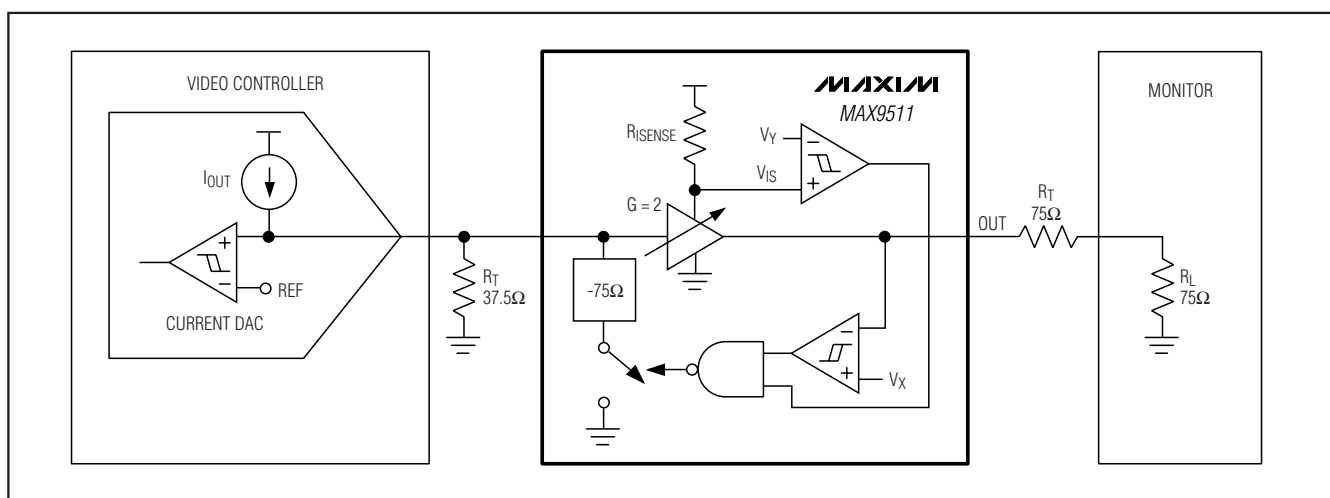


Figure 2. Load-Detection Scheme with MAX9511

resistor to the input. This results in an equivalent impedance of  $75\Omega$  at the DAC output, which indicates to the video controller's internal load-detection circuit that the load is disconnected and the video controller shuts down the video output. Figure 2 and Table 1 demonstrate how the MAX9511 load-detection circuit operates in conjunction with the video controller load detection.

## Output Video Signal Level Shift

The video signal at the MAX9511 output is shifted upwards by approximately 240mV from the input to keep the output stage of the video driver in a linear region of operation. At the connector, the video signal is attenuated by 6dB, canceling the 6dB gain of the video driver. The 240mV level shift is also attenuated by

6dB, and hence the actual video signal seen by the load is only 120mV higher than the video signal at the input of the MAX9511. Monitors and other display devices AC-couple the input signal so the 120mV level shift should not affect the displayed video image.

Table 1. Function of Load-Detection Scheme

AMPLIFIER OUTPUT	MAX9511 INTERNAL SWITCH	RESISTANCE AT DAC OUTPUT
Connected to External Load	Open	$37.5\Omega$
Not Connected to External Load	Closed	$75\Omega$

# Complete VGA Interface with EMI Suppression

## Vertical and Horizontal SYNC

The MAX9511 has separate, noninverting, vertical and horizontal sync buffers. Both sync inputs can level-shift an input as low as 2.3V to a 5V output. Both sync drivers have hysteresis at their input to prevent “chatter” in their outputs. The sync output drivers have a 55Ω (typ) output impedance ( $R_{SO}$ ) to match the cable impedance used for vertical and horizontal sync in most applications. Both sync inputs are pulled to DGND through a 47kΩ resistor if the controller's SYNC source goes high impedance, or if the inputs are left floating, avoiding ambiguous output conditions.

EMI can result from rapid transitions of the sync or the video signals. To reduce the rise and fall times of the sync signal, additional capacitance may be added to the sync outputs. Adding additional capacitance may require “recentering” the display.

## Display Data Channel (DDC)

The MAX9511 bidirectional display data channel (DDC) level translator allows for a lower voltage video controller logic to operate with a higher voltage external monitor logic. Power supplied at  $V_{DD2}$  defines the DDC input voltage thresholds while power supplied at  $V_{DD1}$  defines the DDC output thresholds. Two Schottky-clamped npn transistors shift the lower level DDC inputs to higher logic-level outputs.

DDC\_CLK\_OUT and DDC\_DATA\_OUT are pulled to  $V_{DD1}$  by internal pullup resistors to prevent ambiguous conditions when left floating. At shutdown, DDC inputs can still respond to external commands.

## Slew-Rate Limiting

The MAX9511 outputs are slew-rate limited to reduce EMI. Slew-rate limiting affects the large-signal bandwidth (LSBW) more than the small-signal bandwidth (SSBW), and can be scaled according to the following formula:

$$LSBW(-3dB) = \frac{SR}{2 \times \pi \times V_{OUT}}$$

where  $V_{OUT}$  is the output signal's peak-to-peak voltage and  $LSBW(-3dB)$  is the -3dB bandwidth.

The slew rate of the MAX9511 is controlled by a resistor between RX and AGND. The resistor ( $R_{RX}$ ) can be varied to optimize the EMI suppression to the display resolution while preserving the display quality. The  $R_{RX}$  range is approximately 7kΩ for maximum slew rate and 38kΩ for minimum slew rate (see Figure 3). Slew-rate limiting can be approximated by:

$$SR = 1030 \left( \frac{7000}{R_{RX}} \right) (V/\mu s)$$

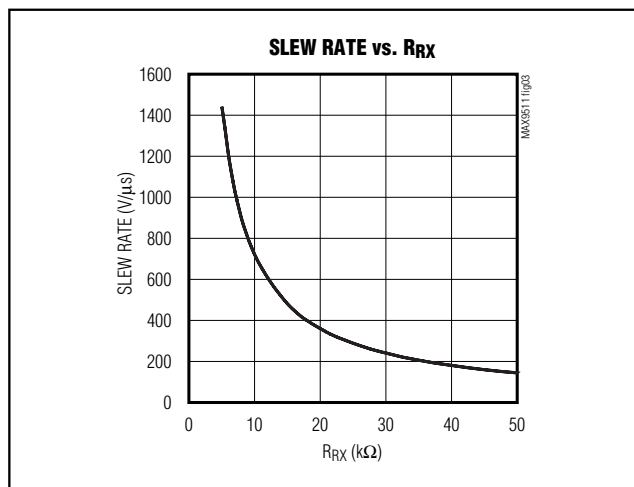


Figure 3. Slew Rate vs.  $R_{RX}$

## Shutdown

The MAX9511 features a low-power shutdown mode for battery-powered/portable applications. Shutdown reduces the quiescent current of the video and sync drivers. Connecting  $\overline{SHDN}$  to ground (DGND) disables the outputs and places the MAX9511 into a low-power shutdown mode.  $\overline{SHDN}$  has a 330kΩ (typ) internal pulldown resistor to DGND. Connect  $\overline{SHDN}$  to  $V_{DD2}$  for normal operation.

## Applications Information

### Customizing Slew Rates for Different Resolutions

When the MAX9511 connects to devices of different resolutions, different slew rates should be used. The slew rate of the MAX9511 is adjustable by varying  $R_{RX}$  between 7kΩ and 38kΩ. By selecting a valid  $R_{RX}$  value for a resolution, the MAX9511 minimizes the EMI and optimizes the video output quality. Shown are two configurations to adjust slew rates using different  $R_{RX}$  values for different video resolutions.

Figure 4 shows how to customize slew rates for three resolutions. This circuit provides three predetermined slew rates by paralleling resistors to create three  $R_{RX}$  values. The combination is controlled by a digital command from the video controller through a switch. This requires that the sample clock rates used by different resolutions are close. The sync bandwidth-limiting capacitors ( $C_{SYNC}$ ) are set for the highest resolution.

# Complete VGA Interface with EMI Suppression

MAX9511

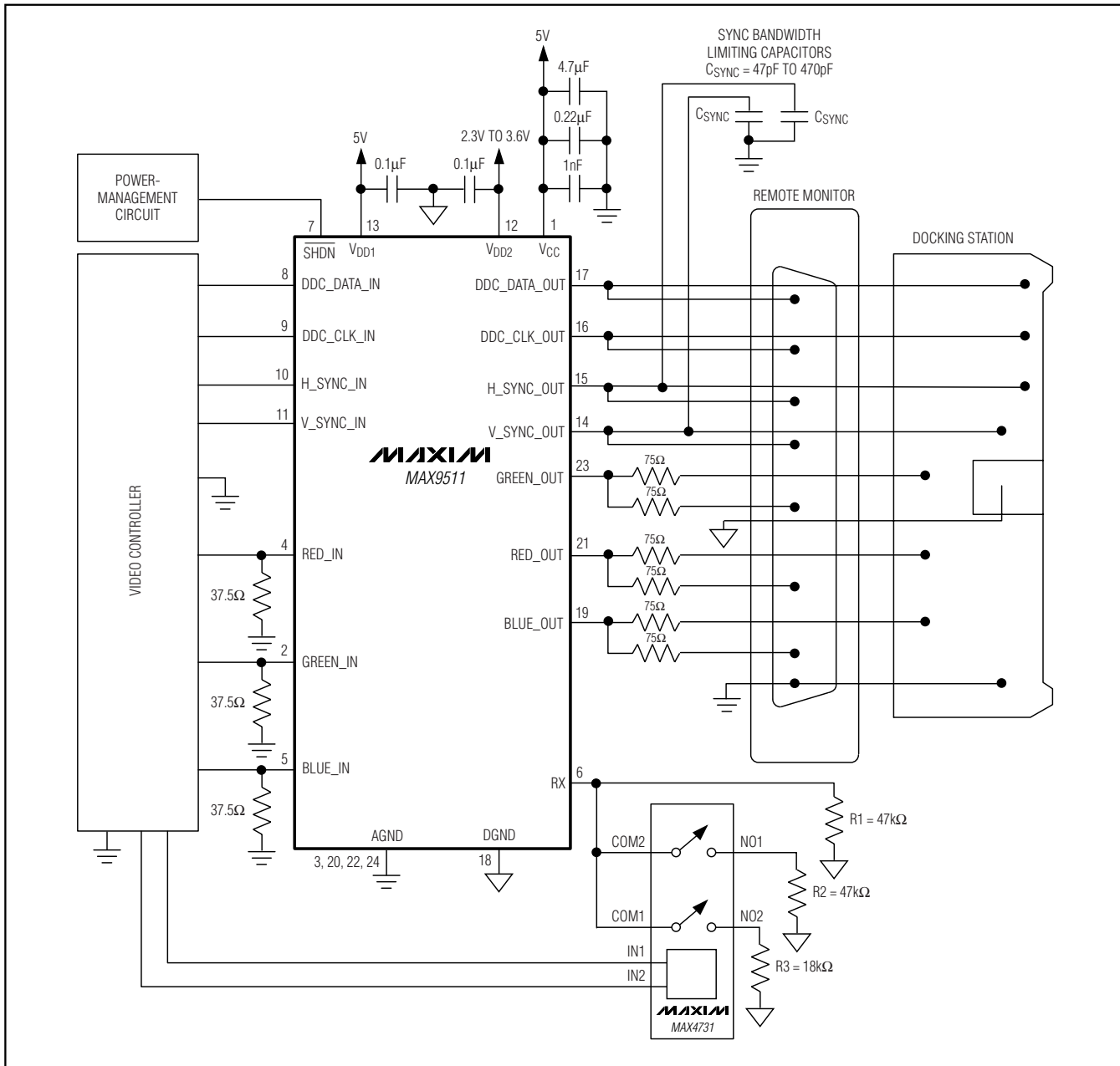


Figure 4. Three Resolution Slew-Rate Control

Figure 4 showcases the setup for three commonly used resolutions: 1600 x 1200, 1280 x 1024, and 1024 x 768. Since the resolution change is relatively slow, the switch does not have to be fast. The impedance of the switch does not need to be low compared to  $R_{RX}$ . When using a high-impedance switch, the resistance

from the switch should be included to calculate  $R_{RX}$ . The MAX4731 50Ω SPST analog switch shown in the figure is used with three external resistors to get  $R_{RX}$  values of 47kΩ, 23.5kΩ, and 10kΩ for 1600 x 1200, 1280 x 1024, and 1024 x 768 resolutions, respectively.

# Complete VGA Interface with EMI Suppression

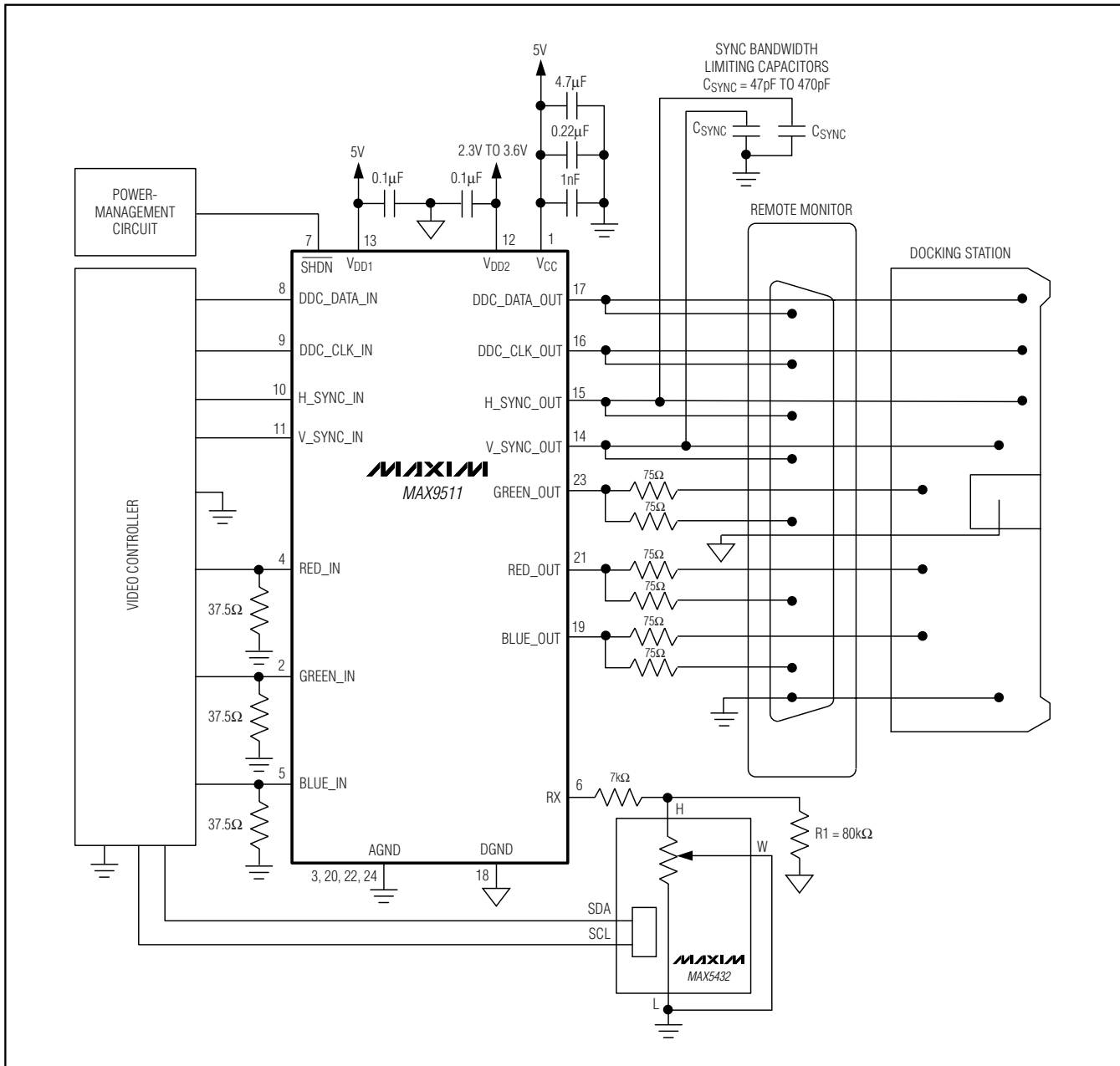


Figure 5. Slew-Rate Control with a Digital Potentiometer

The circuit in Figure 5 uses a MAX5432 digital potentiometer to provide more flexibility in customizing slew rates. An 80kΩ external trim resistor is placed in parallel

with the 50kΩ MAX5432 to limit the maximum value of  $R_{RX}$  to 38kΩ. This setup provides 33 levels of  $R_{RX}$  values through the I<sup>2</sup>C control ports at the MAX5432.

# Complete VGA Interface with EMI Suppression

## Power Supplies

The MAX9511 operates with a 4.5V to 5.5V power supply for video (RGBHV), while DDC and SYNC operate from 2.3V to 3.6V and 4.5V to 5.5V supplies.

## SYNC Bandwidth-Limiting Capacitors

The output impedance,  $R_{SO}$ , of the MAX9511 and an additional capacitance ( $C_{SYNC}$ ) can form a lowpass filter that reduces the jitter of the sync output signal. With  $R_{SO}$  ( $55\Omega$  typ) sync output impedance, the -3dB point of the lowpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{SO} C_{SYNC}}$$

Choose  $C_{SYNC}$  so  $f_{-3dB}$  is well above the highest frequency of interest.

## Power-Supply Bypassing and Ground Management

The MAX9511's high-frequency performance requires proper layout and bypassing. For best performance, place components as close to the device as possible.

Digital or AC transient signals on AGND can create noise at the outputs. Return AGND to the lowest impedance ground available. Bypass the analog supply ( $V_{CC}$ ) with a  $4.7\mu F$  capacitor paralleled with a  $0.22\mu F$  and  $0.001\mu F$  capacitor to AGND, placed as close to the device as possible. Bypass the digital supplies ( $V_{DD1}$ ,  $V_{DD2}$ ) with a  $0.1\mu F$  capacitor to DGND, placed as close to the device as possible. Careful PC board ground layout minimizes crosstalk between the outputs.

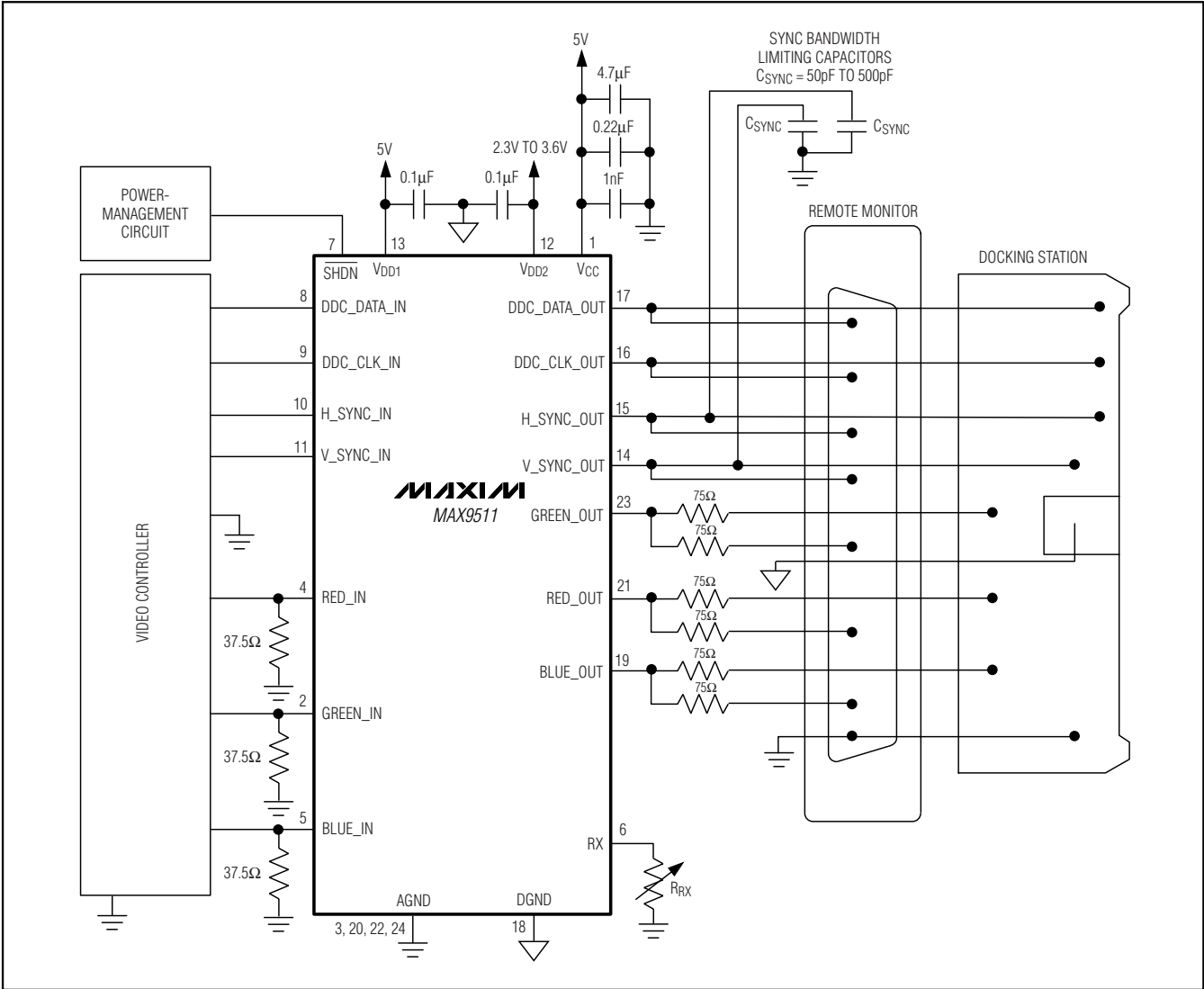
## Chip Information

TRANSISTOR COUNT: 353

PROCESS: BIPOLAR

# Complete VGA Interface with EMI Suppression

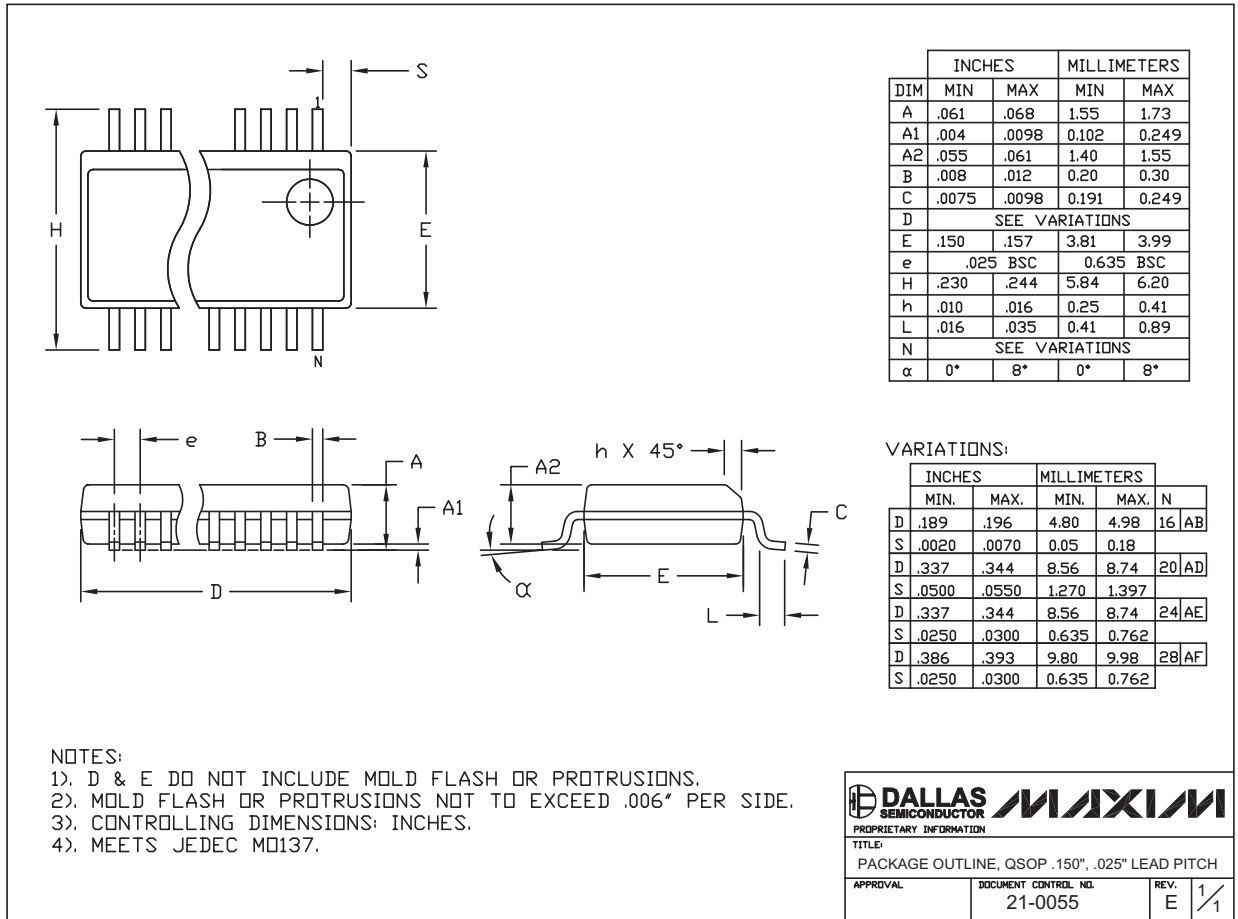
Typical Operating Circuit



# Complete VGA Interface with EMI Suppression

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



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