Low-Voltage Single Asymmetrical SPDT Analog Switch

FEATURES

- Low Voltage Operation (2.7 V to 5.5 V)
- Low On-Resistance - r_{ON}
  - NO = 0.8 Ω
  - NC = 1.2 Ω
- Low Power Consumption
- TTL/CMOS Compatible
- TSOP-6 Package

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems

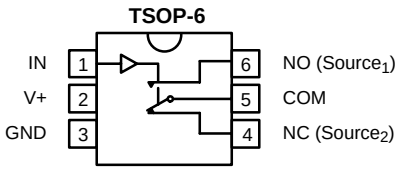
DESCRIPTION

The DG2020 is a single-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed, low on-resistance and small physical size, the DG2020 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2020 is built on Vishay Siliconix's low voltage JI2 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View

Device Marking: E3xxx

TRUTH TABLE		
Logic	**NC**	**NO**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
-40 to 85°C	TSOP-6	DG2020DV

ABSOLUTE MAXIMUM RATINGS

Reference to GND
V+ . . . . . -0.3 to +6 V
IN, COM, NC, NO[a] . . . . . -0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal) . . . . . ±50 mA
Peak Current . . . . . ±200 mA
(Pulsed at 1 ms, 10% duty cycle)
Storage Temperature (D Suffix) . . . . . -65 to 125°C

Power Dissipation (Packages)[b]
TSOP-6[c] . . . . . 570 mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 7.0 mW/°C above 25°C

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.4 or 2.0 V[e]	Temp[a]	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	$r_{ON(NO)}$	V+ = 2.7 V, V_{COM} = 1.5 V, I_{NO}, I_{NC} = 100 mA	Room Full		1.4 1.5	2.0 2.1	Ω
	$r_{ON(NC)}$		Room Full		2.2 2.3	3.2 3.3	
r_{ON} Flatness[d]	$r_{ON(NO)}$ Flatness	V+ = 2.7 V V_{COM} = 0 to V+, I_{NO}, I_{NC} = 100 mA	Room		0.42		
Switch Off Leakage Current[f]	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 1 V/3 V V_{COM} = 3 V/1 V	Room Full	–2.3 –60		2.3 60	nA
	$I_{COM(off)}$		Room Full	–2.3 –60		2.3 60	
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1 V/3 V	Room Full	–2.3 –60		2.3 60	
Digital Control							
Input High Voltage	V_{INH}		Full	2			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance	C_{in}		Full		3.7		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA
Dynamic Characteristics							
Turn-On Time	$t_{ON(NO)}$	V_{NO} or V_{NC} = 2.0 V, R_L = 300 Ω, C_L = 35 pF	Room Full		6	10 11	µs
	$t_{ON(NC)}$		Room Full		5	7 8	
Turn-Off Time	$t_{OFF(NO)}$		Room Full		2	5 5.5	
	$t_{OFF(NC)}$		Room Full		2	4 4.5	
Break-Before-Make Time	t_d	V_{NO} or V_{NC} = 2.0 V, R_L = 300 Ω, C_L = 35 pF	Full	1	3		
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		1		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		–52		dB
Crosstalk[d]	X_{TALK}		Room		–53		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		75		pF
	$C_{NC(off)}$		Room		34		
Channel-On Capacitance[d]	$C_{NO(on)}$		Room		88		
	$C_{NC(on)}$		Room		95		
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	V_{IN} = 0 or V+	Full		0.2	1.0	µA
Power Consumption	P_C		Full			3.3	µW

SPECIFICATIONS (V+ = 5 V)

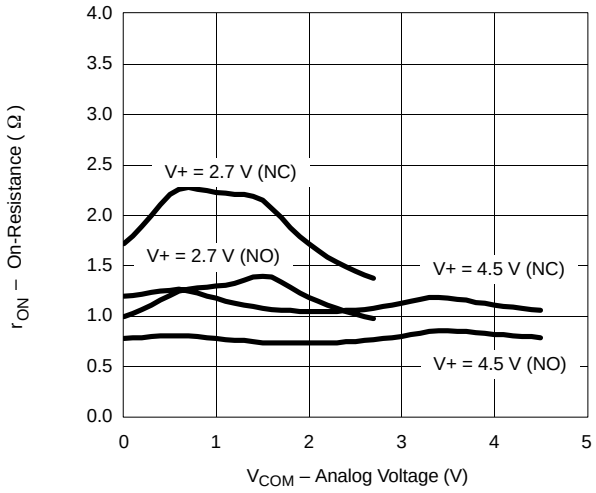
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, V_{IN} = 0.8 or 2.4 V[e]	Temp[a]	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	$r_{ON(NO)}$	V+ = 4.5 V, V_{COM} = 3 V, I_{NO}, I_{NC} = 100 mA	Room Full		0.8 0.9	1.1 1.2	Ω
	$r_{ON(NC)}$		Room Full		1.2 1.3	1.6 1.7	
r_{ON} Flatness[d]	$r_{ON(NO)}$ Flatness	V+ = 4.5 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 100 mA	Room		0.13		
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 5.5 V V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V	Room Full	–5.3 –98		5.3 98	nA
	$I_{COM(off)}$		Room Full	–5.3 –98		5.3 98	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V, V_{NO}, V_{NC} = V_{COM} = 1 V/4.5 V	Room Full	–5.3 –98		5.3 98	
Digital Control							
Input High Voltage	V_{INH}		Full	2.4			V
Input Low Voltage	V_{INL}		Full			0.8	
Input Capacitance	C_{in}		Full		3.5		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA
Dynamic Characteristics							
Turn-On Time	$t_{ON(NO)}$	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF	Room Full		3	6 6.5	µs
	$t_{ON(NC)}$		Room Full		2	5 5.5	
Turn-Off Time	$t_{OFF(NO)}$		Room Full		1	4 4.5	
	$t_{OFF(NC)}$		Room Full		1	3 3.5	
Break-Before-Make Time	t_d	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF	Full	0.3	1.5		
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		5		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		–53		dB
Crosstalk[d]	X_{TALK}		Room		–54		
Source-Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		65		pF
	$C_{NC(off)}$		Room		32		
Channel-On Capacitance[d]	$C_{NO(on)}$		Room		90		
	$C_{NC(on)}$		Room		95		
Power Supply							
Power Supply Range	V+			4.5		5.5	V
Power Supply Current	I+	V_{IN} = 0 or V+	Full		0.2	1.0	µA
Power Consumption	P_C		Full			5.5	µW

Notes:

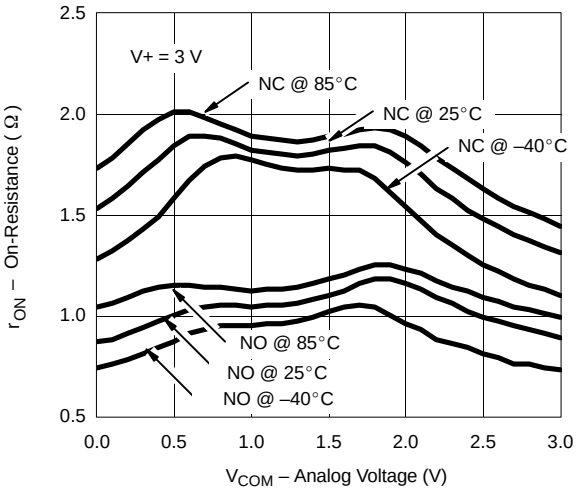
a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5-V leakage testing, not production tested.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

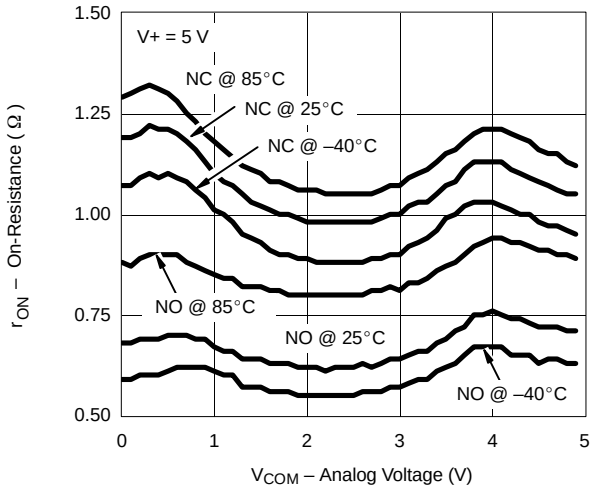
r_{ON} vs. V_{COM} and Supply Voltage



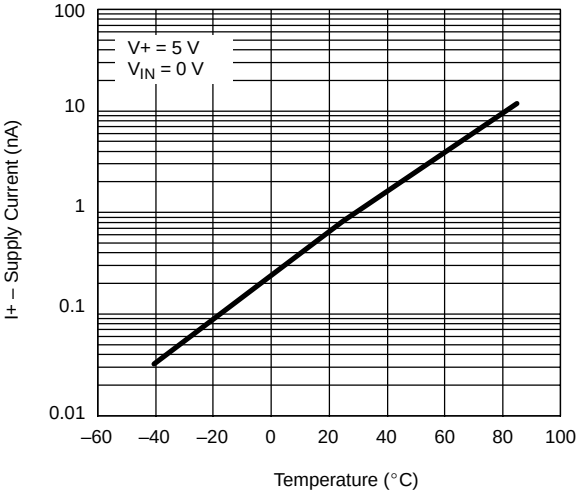
r_{ON} vs. Analog Voltage and Temperature



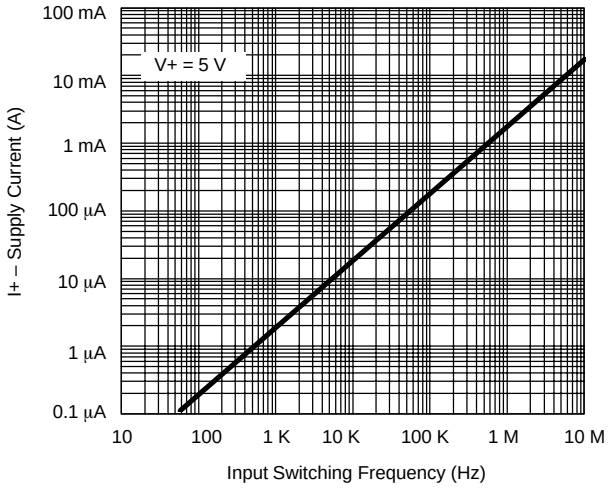
r_{ON} vs. Analog Voltage and Temperature



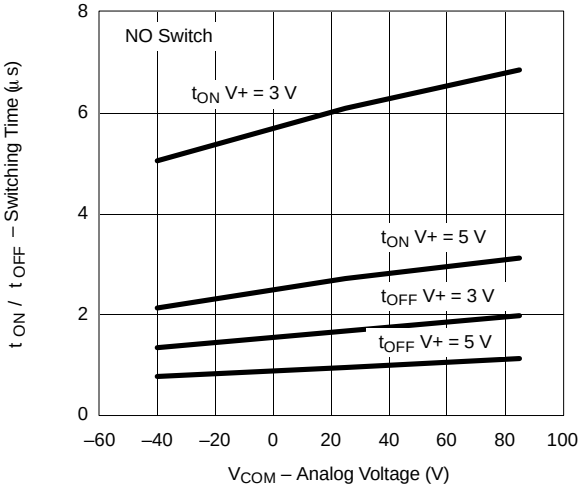
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

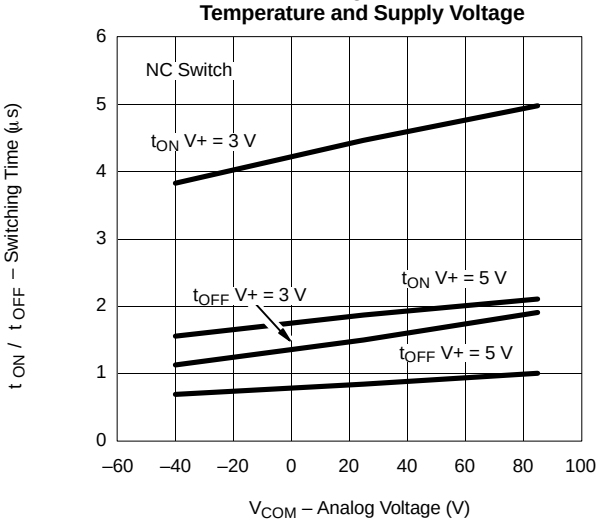


Switching Time vs. Temperature and Supply Voltage

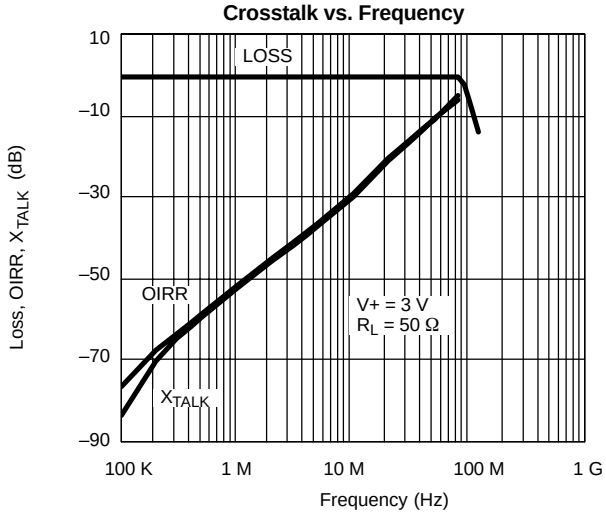


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

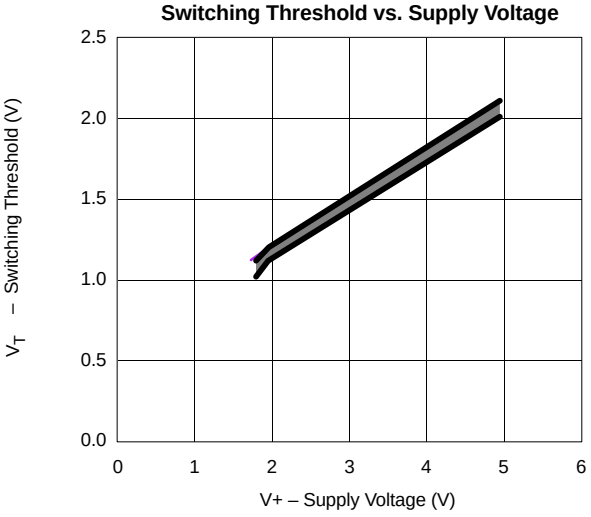
Switching Time vs. Temperature and Supply Voltage



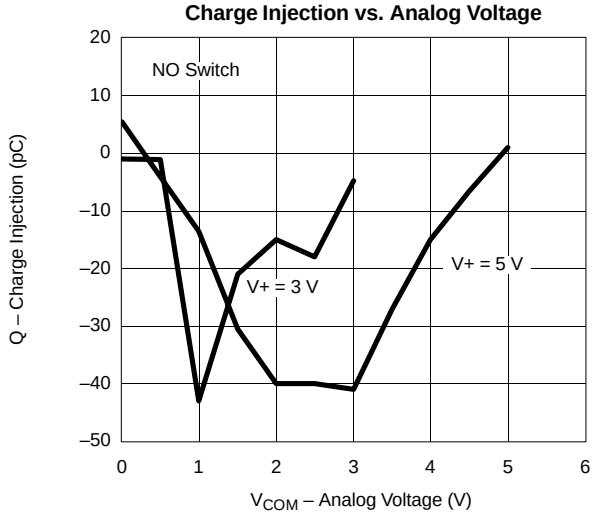
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



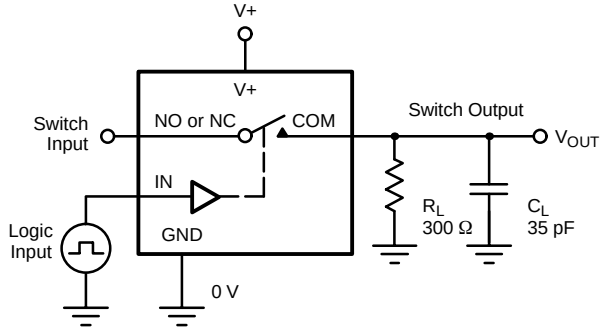
Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

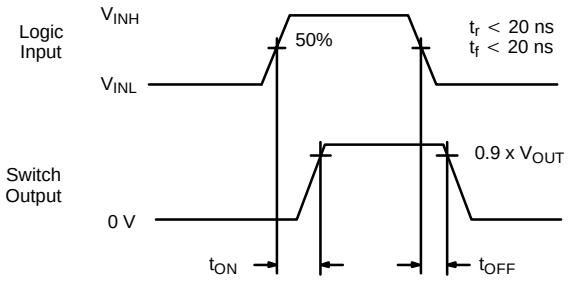


TEST CIRCUITS



C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time

TEST CIRCUITS

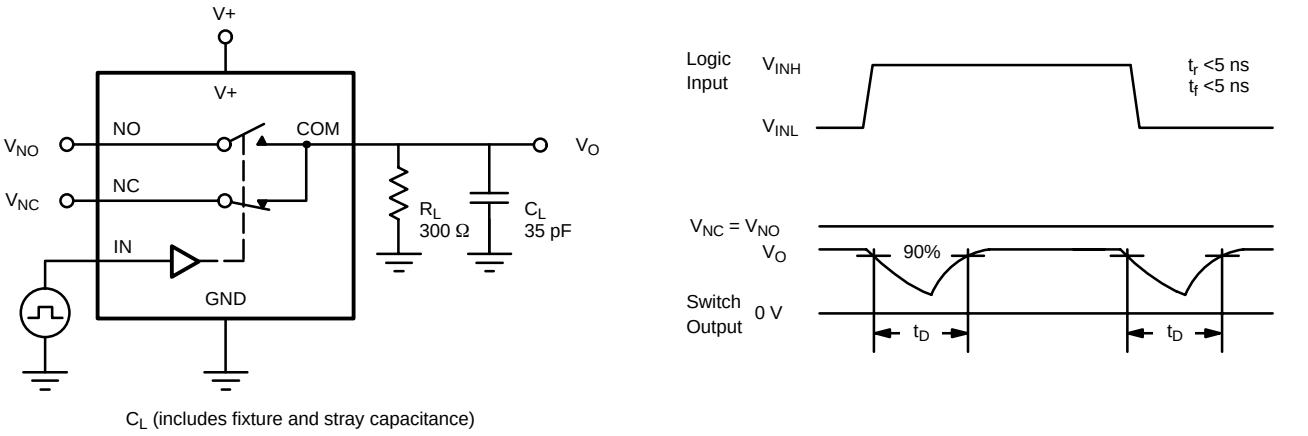
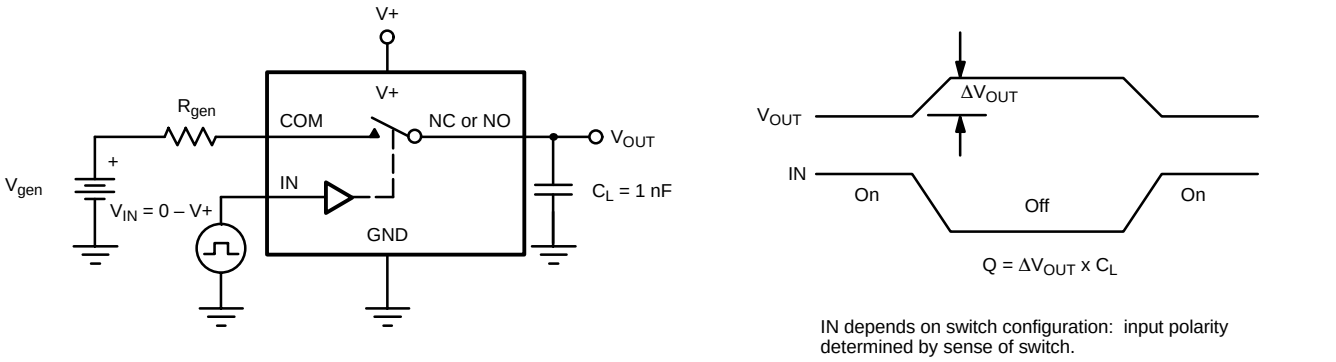


FIGURE 5. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 2. Charge Injection

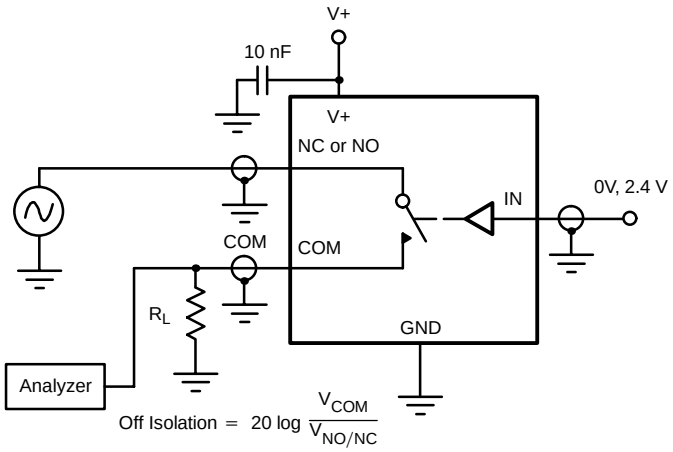


FIGURE 3. Off-Isolation

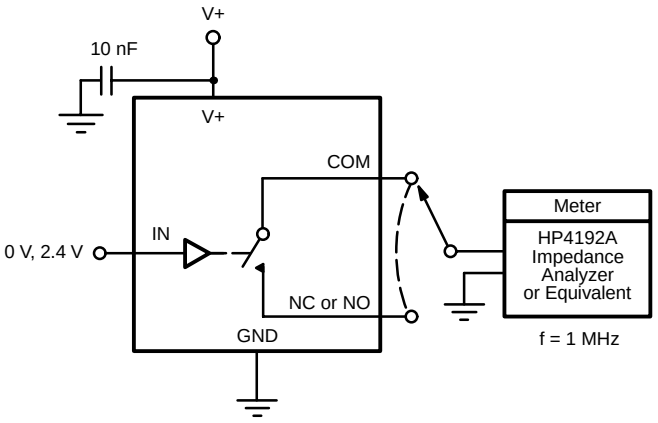


FIGURE 4. Channel Off/On Capacitance