



## Quad SPST CMOS Analog Switch with Latches

### FEATURES

- Accepts 150-ns Write Pulse Width
- 5-V On-Chip Regulator
- Latches Are Transparent with  $\overline{WR}$  Low
- Low On-Resistance: 60  $\Omega$

### BENEFITS

- Compatible with Most  $\mu$ P Buses
- Allows Wide Power Supply Tolerance Without Affecting TTL Compatibility
- Reduced Power Consumption
- Allows Flexibility of Design

### APPLICATIONS

- $\mu$ P Based Systems
- Automatic Test Equipment
- Communication Systems
- Data Acquisition Systems
- Medical Instrumentation
- Factory Automation

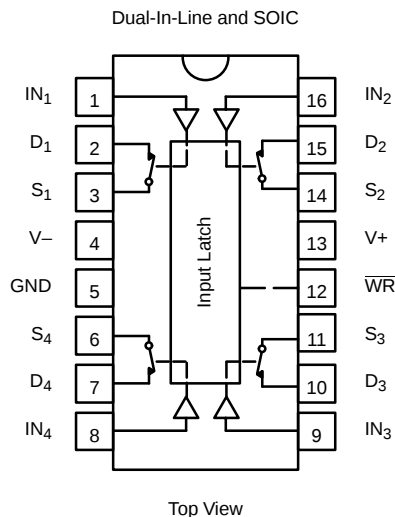
### DESCRIPTION

The DG221B is a monolithic quad single-pole, single-throw analog switch designed for precision switching applications in communication, instrumentation and process control systems. Featuring independent onboard latches and a common  $\overline{WR}$  pin, each DG221B can be memory mapped, and addressed as a single data byte for simultaneous switching.

The DG221B combines low power and low on-resistance (60  $\Omega$  typical) while handling continuous currents up to 20 mA. An epitaxial layer prevents latchup.

The device features true bidirectional performance in the on condition.

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Four Latchable SPST Switches per Package

| TRUTH TABLE |                 |                                                                        |
|-------------|-----------------|------------------------------------------------------------------------|
| $IN_x$      | $\overline{WR}$ | Switch                                                                 |
| 0           | 0               | ON                                                                     |
| 1           | 0               | OFF                                                                    |
| X           |                 | Control data latched-in, switches on or off as selected by last $IN_x$ |
| X           | 1               | Maintains previous state                                               |

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V

| ORDERING INFORMATION |                    |             |
|----------------------|--------------------|-------------|
| Temp Range           | Package            | Part Number |
| -40°C to 85°C        | 16-Pin Plastic DIP | DG221BDJ    |
|                      | 16-Pin Narrow SOIC | DG221BDY    |

# ABSOLUTE MAXIMUM RATINGS

|                                                                     |                                  |
|---------------------------------------------------------------------|----------------------------------|
| Voltages Referenced to V–                                           |                                  |
| V+ .....                                                            | 34 V                             |
| GND .....                                                           | 25 V                             |
| Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub> ..... | (V–) –2 V to (V+) +2 V           |
|                                                                     | or 20 mA, whichever occurs first |
| Continuous Current (Any Terminal) .....                             | 30 mA                            |
| Continuous Current, S or D .....                                    | 20 mA                            |
| Peak Current, S or D (Pulsed 1 ms, 10% duty cycle) .....            | 70 mA                            |

|                                               |              |
|-----------------------------------------------|--------------|
| Storage Temperature: (DJ and DY Suffix) ..... | –65 to 125°C |
| Power Dissipation (Package) <sup>b</sup>      |              |
| 16-Pin Plastic DIP <sup>c</sup> .....         | 470 mW       |
| 16-Pin SOIC <sup>d</sup> .....                | 600 mW       |

## Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 25°C
- Derate 7.7 mW/°C above 75°C

## SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

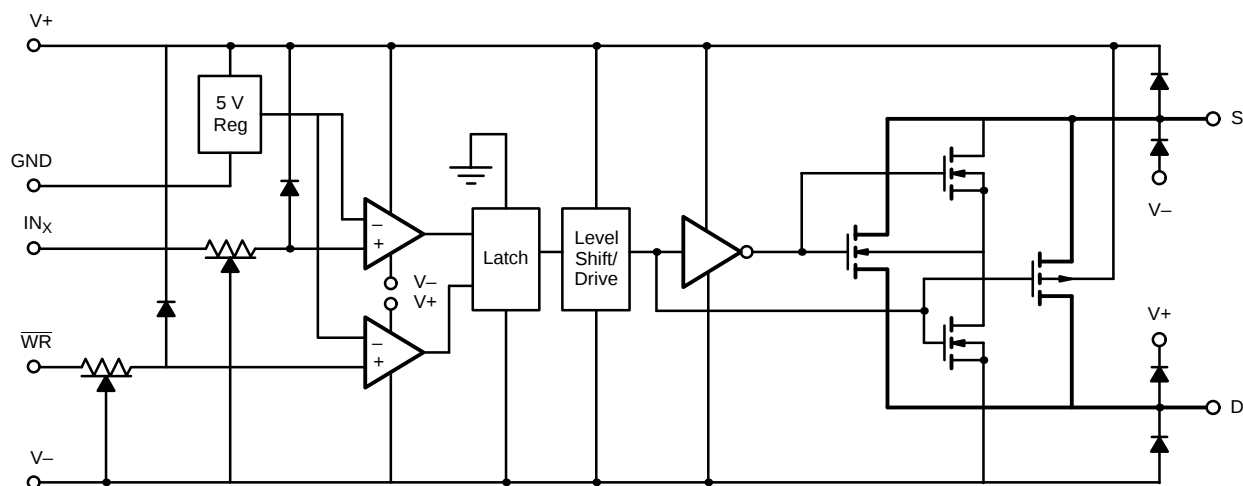


FIGURE 1.

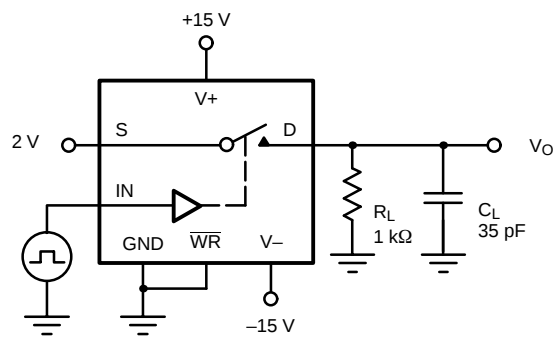


| SPECIFICATIONS <sup>a</sup>      |                                     |                                                                                                                                                                    |                   |                       |                  |                  |      |
|----------------------------------|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-----------------------|------------------|------------------|------|
| Parameter                        | Symbol                              | Test Conditions<br>Unless Otherwise Specified<br>V <sub>+</sub> = 15 V, V <sub>–</sub> = –15 V<br>V <sub>IN</sub> = 2.4 V, 0.8 <sup>f</sup> V, $\overline{WR}$ = 0 | Temp <sup>b</sup> | Limits<br>–40 to 85°C |                  |                  | Unit |
|                                  |                                     |                                                                                                                                                                    |                   | Min <sup>d</sup>      | Typ <sup>c</sup> | Max <sup>d</sup> |      |
| Analog Switch                    |                                     |                                                                                                                                                                    |                   |                       |                  |                  |      |
| Analog Signal Range <sup>e</sup> | V <sub>ANALOG</sub>                 |                                                                                                                                                                    | Full              | –15                   |                  | 15               | V    |
| Drain-Source On-Resistance       | r <sub>DS(on)</sub>                 | I <sub>S</sub> = –10 mA, V <sub>D</sub> = ±10 V                                                                                                                    | Room Full         |                       | 60               | 90<br>135        | Ω    |
| Source Off Leakage Current       | I <sub>S(off)</sub>                 | V <sub>S</sub> = ±14 V, V <sub>D</sub> = ∓14 V                                                                                                                     | Room Full         | –5<br>–100            | ±0.01            | 5<br>100         | nA   |
| Drain Off Leakage Current        | I <sub>D(off)</sub>                 |                                                                                                                                                                    | Room Full         | –5<br>–100            | ±0.02            | 5<br>100         |      |
| Drain On Leakage Current         | I <sub>D(on)</sub>                  | V <sub>S</sub> = V <sub>D</sub> = ±14 V                                                                                                                            | Room Full         | –5<br>–200            | ±0.01            | 5<br>200         |      |
| Digital Control                  |                                     |                                                                                                                                                                    |                   |                       |                  |                  |      |
| Input Current                    | I <sub>INL</sub> , I <sub>INH</sub> | V <sub>IN</sub> = 0 V or = 2.4 V                                                                                                                                   | Room Full         | –1<br>–10             | –0.0004          | 1<br>10          | μA   |
| Dynamic Characteristics          |                                     |                                                                                                                                                                    |                   |                       |                  |                  |      |
| Turn-On Time                     | t <sub>ON</sub>                     | See Figure 2                                                                                                                                                       | Room              |                       |                  | 550              | ns   |
| Turn-Off Time                    | t <sub>OFF</sub>                    |                                                                                                                                                                    | Room              |                       |                  | 340              |      |
| Turn-On Time Write               | t <sub>ON</sub> , $\overline{WR}$   | See Figure 3                                                                                                                                                       | Room              |                       |                  | 550              |      |
| Turn-Off Time Write              | t <sub>OFF</sub> , $\overline{WR}$  |                                                                                                                                                                    | Room              |                       |                  | 340              |      |
| Write Pulse Width                | t <sub>W</sub>                      | See Figure 4                                                                                                                                                       | Room              | 150                   | 120              |                  |      |
| Input Setup Time                 | t <sub>S</sub>                      |                                                                                                                                                                    | Room              | 180                   | 130              |                  |      |
| Input Hold Time                  | t <sub>H</sub>                      |                                                                                                                                                                    | Room              | 20                    | 18               |                  |      |
| Charge Injection                 | Q                                   | C <sub>L</sub> = 1000 pF<br>V <sub>GEN</sub> = 0 V, R <sub>GEN</sub> = 0 Ω                                                                                         | Room              |                       | 20               |                  | pC   |
| Source-Off Capacitance           | C <sub>S(off)</sub>                 | f = 1 MHz, V <sub>S</sub> , V <sub>D</sub> = 0 V                                                                                                                   | Room              |                       | 8                |                  | pF   |
| Drain-Off Capacitance            | C <sub>D(off)</sub>                 |                                                                                                                                                                    | Room              |                       | 9                |                  |      |
| Channel-On Capacitance           | C <sub>D(on)</sub>                  |                                                                                                                                                                    | Room              |                       | 29               |                  |      |
| Off Isolation                    | OIRR                                | V <sub>S</sub> = 1 V <sub>p-p</sub> , f = 100 kHz<br>C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ                                                                 | Room              |                       | 70               |                  | dB   |
| Interchannel Crosstalk           | X <sub>TALK</sub>                   |                                                                                                                                                                    | Room              |                       | 90               |                  |      |
| Power Supplies                   |                                     |                                                                                                                                                                    |                   |                       |                  |                  |      |
| Positive Supply Current          | I <sub>+</sub>                      | All Channels On or Off<br>V <sub>IN</sub> = 0 V or 2.4 V                                                                                                           | Full              |                       | 0.8              | 1.5              | mA   |
| Negative Supply Current          | I <sub>–</sub>                      |                                                                                                                                                                    | Room              | –1                    | –0.4             |                  |      |

## Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

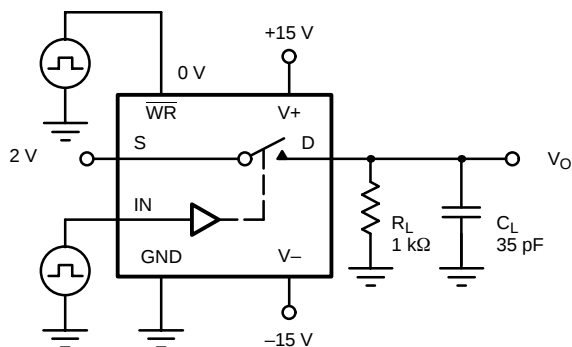
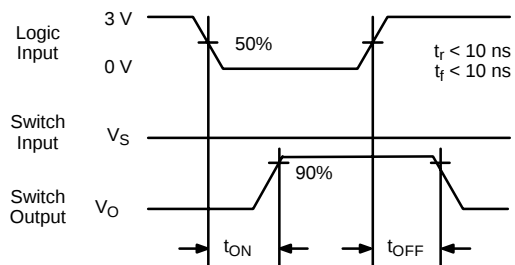
TEST CIRCUITS



$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

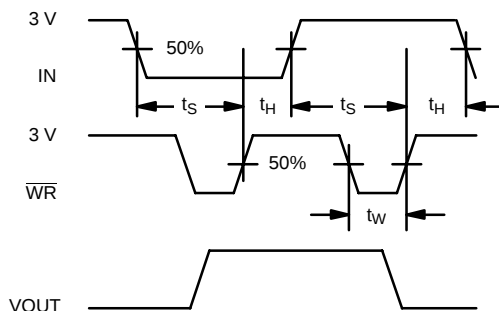
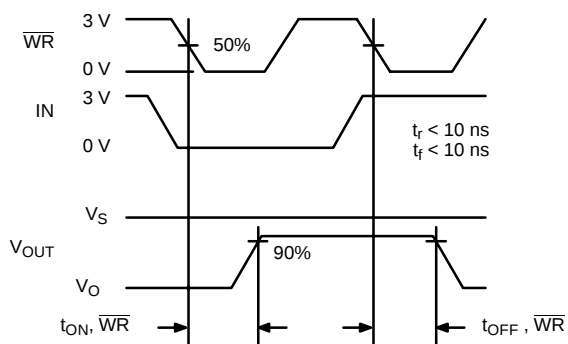
FIGURE 2. Switching Time



$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

FIGURE 3.  $\overline{WR}$  Switching Time

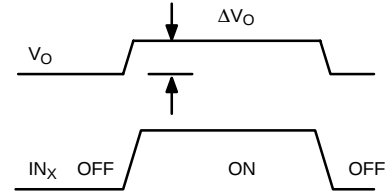
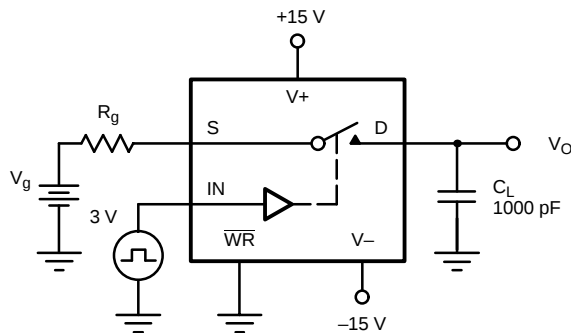


$t_H$  = Hold Time  
 $t_S$  = Setup Time  
 $t_W$  = WR Pulse Width

The latches are level sensitive. When  $\overline{WR}$  is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of  $\overline{WR}$ .

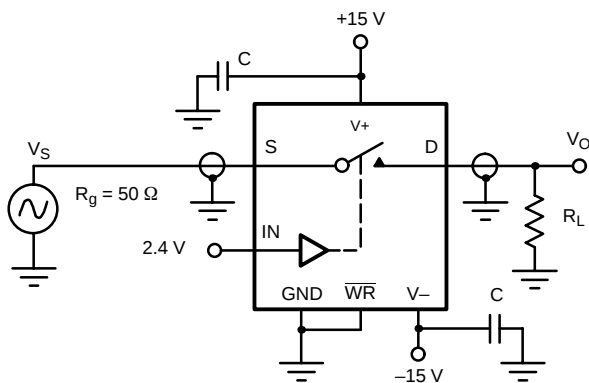
FIGURE 4.  $\overline{WR}$  Setup Conditions

**TEST CIRCUITS**



$\Delta V_O$  = measured voltage error due to charge injection  
The charge injection in coulombs is  $Q = C_L \times \Delta V_O$

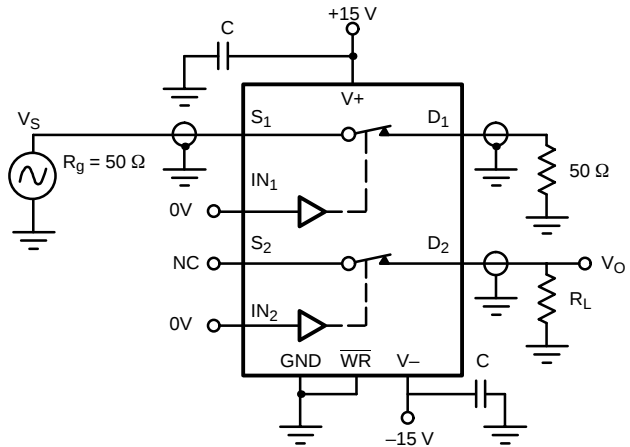
**FIGURE 5.** Charge Injection



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

**FIGURE 6.** Off Isolation



$$X_{\text{TALK}} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

**FIGURE 7.** Channel-to-Channel Crosstalk

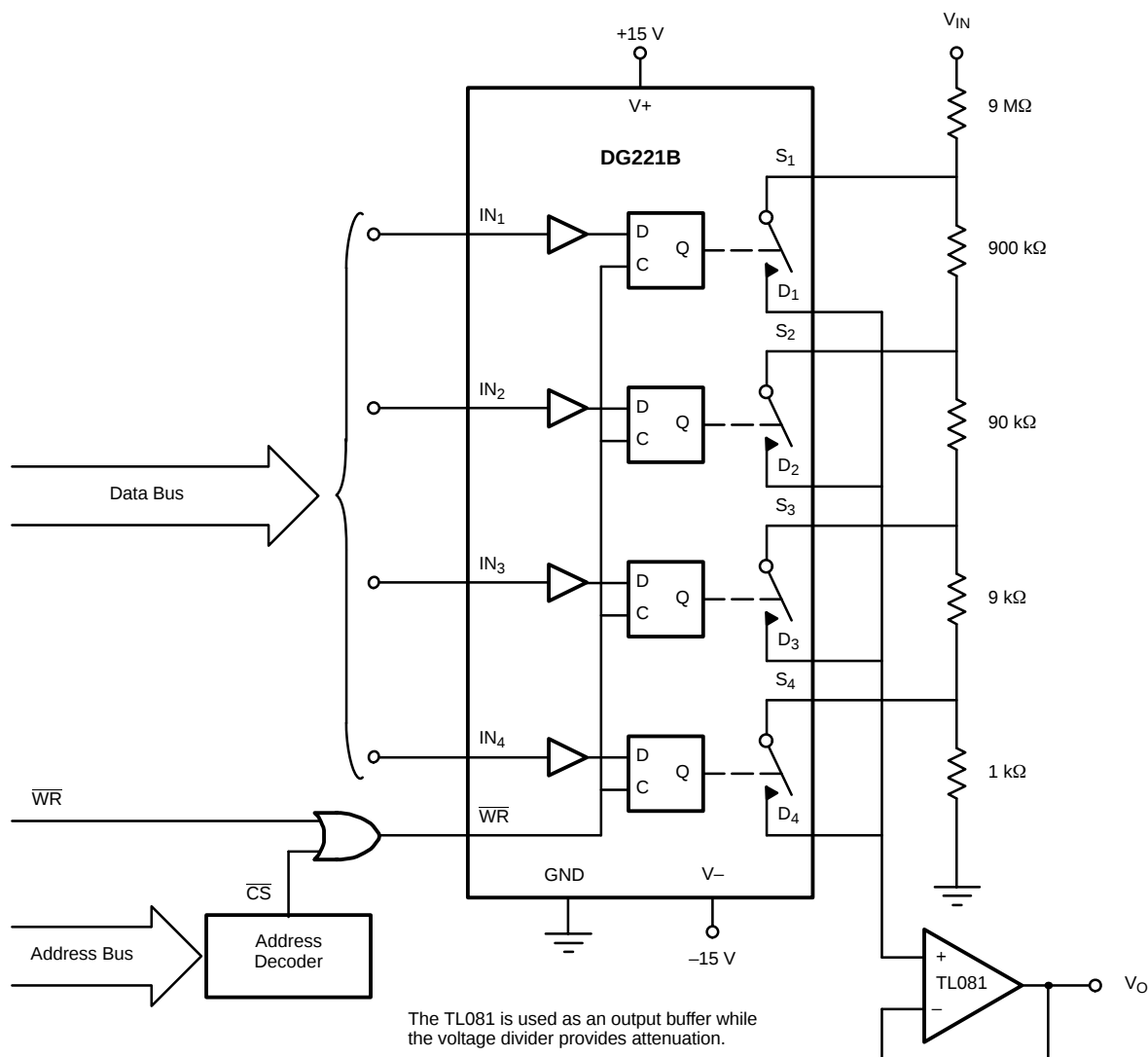
**APPLICATION HINTS<sup>a</sup>**

| V+<br>Positive Supply<br>Voltage<br>(V) | V-<br>Negative Supply<br>Voltage<br>(V) | GND<br>(V) | WR<br>(V) | V <sub>IN</sub><br>Logic Input<br>Voltage<br>V <sub>INH(min)</sub> /V <sub>INL(max)</sub><br>(V) | V <sub>S</sub> or V <sub>D</sub><br>Analog Voltage<br>Range<br>(V) |
|-----------------------------------------|-----------------------------------------|------------|-----------|--------------------------------------------------------------------------------------------------|--------------------------------------------------------------------|
| 15                                      | -15                                     | 0          | 2.4/0.8   | 2.4/0.8                                                                                          | -15 to 15                                                          |
| 10                                      | -10                                     | 0          | 2.4/0.8   | 2.4/0.8                                                                                          | -10 to 10                                                          |
| 10                                      | -5                                      | 0          | 2.4/0.8   | 2.4/0.8                                                                                          | -5 to 10                                                           |

Notes:

a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

## APPLICATIONS

FIGURE 8.  $\mu$ P-Controlled Analog Signal Attenuator

| TRUTH TABLE     |                 |                 |                 |                 |           |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------|
| IN <sub>1</sub> | IN <sub>2</sub> | IN <sub>3</sub> | IN <sub>4</sub> | WR <sup>A</sup> | ON SWITCH |
| 0               | 0               | 0               | 0               | 0               | All       |
| 1               | 1               | 1               | 1               | 0               | None      |
| 0               | 1               | 1               | 1               | 0               | 1         |
| 1               | 0               | 1               | 1               | 0               | 2         |
| 1               | 1               | 0               | 1               | 0               | 3         |
| 1               | 1               | 1               | 0               | 0               | 4         |

| OUTPUT ATTENUATION FOR FIGURE 8 |                 |                 |                 |                 |        |
|---------------------------------|-----------------|-----------------|-----------------|-----------------|--------|
| WR                              | IN <sub>1</sub> | IN <sub>2</sub> | IN <sub>3</sub> | IN <sub>4</sub> | Gain   |
| 0                               | 0               | 1               | 1               | 1               | 0.1    |
| 0                               | 1               | 0               | 1               | 1               | 0.01   |
| 0                               | 1               | 1               | 0               | 1               | 0.001  |
| 0                               | 1               | 1               | 1               | 0               | 0.0001 |

## Notes:

a. WR may be held at "0" for temporary operation similar to DG201A/DG201B. With WR at "0" SW<sub>1</sub> will remain on as long as IN<sub>1</sub> is held at "0".