



High Speed, Low Voltage, 3 Ω, Quad SPDT CMOS Analog Switch

DESCRIPTION

The DG2706 is a high speed, low voltage, low On-resistance, quad SPDT (single pole double throw) analog switch. It operates from a 1.65 V to 4.3 V single power supply and achieves 3 Ω switch On-resistance. When turned on, each switch conducts equally in both directions. Its switch on resistance flatness is 0.6 Ω and channel to channel matching is of 0.3 Ω when powered with single 3.15 V supply. All channels guaranteed break before make switching.

Control logic input has 0.5 V to 1.65 V logic threshold. It features a 190 MHz - 3 dB bandwidth, - 90 dB crosstalk and - 70 dB off-isolation at 1 MHz.

The DG2706 is an ideal fit for low voltage battery powered devices switching audio, video, multi-media data streams, and control signals between different functional circuits or ports.

The DG2707 comes in a small miniQFN-16 lead package (1.8 mm x 2.6 mm x 0.75 mm). As a committed partner to community and the environment, Vishay Siliconix manufactures this product with the lead(Pb)-free device terminations and is 100 % RoHS compliant.

FEATURES

Operation voltage range: 1.65 V to 4.3 V
Guaranteed On-resistance: 3.0 Ω at 3.15 V



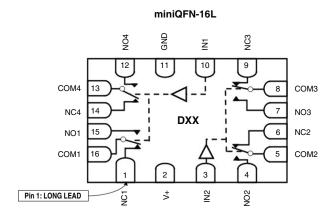
ROHS

- Low voltage logic threshold
- Low crosstalk: 70 dB
- High off-isolation: 90 dB
- Ultra small package: miniQFN16 of 1.8 mm x 2.6 mm

APPLICATIONS

- · Dual SIM card switch
- A/V and analog signal routing
- · Battery operated devices
- Data acquisition systems
- Communications systems
- · Medical and ATE equipments

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View

Device Marking: DXX Traceability Code: D is DG2706DN XX = Date/Lot

| ORDERING INFORMATION | | | | |
|----------------------|------------|----------------|--|--|
| Temp Range | Package | Part Number | | |
| - 40 °C to 85 °C | miniQFN-16 | DG2706DN-T1-E4 | | |

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| TRUTH TABLE DG2706 QUAD SPDT, miniQFN-16L | | | | | |
|---|-------------|-------------------|----------------|--|--|
| Select Input | | On Switches | | | |
| IN1 (Pin 10) | IN2 (Pin 3) | Description (Pin) | Common (Pin) | | |
| 0 | Х | NC1 (Pin 1) | COM1 (Din 16) | | |
| 1 | Х | NO1 (Pin 15) | COM1 (Pin 16) | | |
| 0 | Х | NC4 (Pin 14) | COM4 (Dir. 10) | | |
| 1 | Х | NO4 (Pin 12) | COM4 (Pin 13) | | |
| х — | 0 | NC2 (Pin 6) | COM2 (Pin 5) | | |
| | 1 | NO2 (Pin 4) | | | |
| х — | 0 | NC3 (Pin 9) | COM3 (Pin 3) | | |
| | 1 | NO3 (Pin 7) | | | |

| ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted | | | | |
|---|------------------------------|---------------------|------|--|
| Parameter | | Limit | Unit | |
| Reference to GND | V+ | - 0.3 to 5.0 | V | |
| | IN, COM, NC, NO ^a | - 0.3 to (V+ + 0.3) | V | |
| Current (Any terminal except NO, NC or COM) | | 30 | | |
| Continuous Current (NO, NC, or COM) | | ± 250 | mA | |
| Peak Current (Pulsed at 1 ms, 10 % Duty Cycle) | | ± 500 | | |
| Storage Temperature (D Suffix) | | - 65 to 150 | °C | |
| Thermal Resistance (Package) ^b | miniQFN-16 | 152 °C/W | | |
| Power Dissipation (Package) ^b | miniQFN-16 ^{c, d} | 525 | mW | |

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 6.6 mW/°C above 70 °C
- d. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.





| Parameter | | Test Conditions | Temp.b | Limits - 40 °C to 85 °C | | | |
|--|--|--|--------------|----------------------------|-------------------|-------------------|------|
| | Symbol | Otherwise Unless Specified | | Min. ^d | Typ. ^c | Max. ^d | Unit |
| Analog Switch | - | | | | | | |
| Analog Signal Range ^e | V _{ANALOG} | R _{DS(on)} | Full | 0 | | V+ | V |
| On-Resistance | R _{DS(on)} | V+ = 3.15 V, I _{NO/NC} = 10 mA, V _{COM} = 1.0 V | Room Full | | 3 | 5.5 6 | |
| R _{ON} Match | $\Delta R_{(ON)}$ | V+ = 3.15 V, I _{NO/NC} = 10 mA, V _{COM} = 1.0 V | Room | | 0.3 | | Ω |
| R _{ON} Resistance Flatness | R _{ON} Flatness | $V = 3.15 \text{ V}, I_{NO/NC} = 10 \text{ mA},$ $V_{COM} = 0 \text{ V}, 1 \text{ V}$ | Room | | 0.6 | | |
| | 1 | V+ = 3.6 V, V _{NO/NC} = 0.5 V/3 V, | Room | - 5 | | 5 | |
| Channel Off Leakage Current | I _{NO/NC(off)} | | Full | - 10 | | 10 | |
| | I _{COM(off)} | $V_{COM} = 3 V/0.5 V$ | Room | - 5 | | 5 | nA |
| | ·COM(off) | | Full | - 10 | | 10 | 117 |
| Channel-On Leakage | I _{COM(on)} | $V+ = 3.6 \text{ V}, V_{NO/NC}, V_{COM} = 3 \text{ V}/0.5 \text{ V}$ | Room | - 10 | | 10 | - |
| Current | -CONI(OII) | | Full | - 20 | | 20 | |
| Digital Control | | | | | T | , , | |
| Input High Voltage | V_{INH} | | Full | 1.65 | | | V |
| Input Low Voltage | V_{INL} | | Full | | | 0.4 | |
| Input Current | I _{INL} or I _{INH} | $V_{IN} = 0$ or $V+$ | Full | - 1 | | 1 | μΑ |
| Dynamic Characteristics | | | | | | | |
| Break-Before-Make Time | t _{BBM} | | Room | | 1 | | ns |
| Break Belore Wake Time | , BBIM | | Full | 5 | | | |
| Enable Turn-On Time | nable Turn-Off Time t _{OFF(EN)} | $V_{NO}, V_{NC} = 1.5 \text{ V}, R_L = 50 \Omega, C_L = 35 \text{ pF}$ | Room | | 20 | 45 | |
| | | | Full | | | 55 | |
| Enable Turn-Off Time | | | Room | | 15 | 35 | |
| | | | Full | | | 45 | |
| Charge Injection ^d | Q _{INJ} | $C_L = 1 \text{ nF, } R_{GEN} = 0 \Omega, V_{NC/NO} = 2 \text{ V}$ | Room | | 3 | | pC |
| Off-Isolation ^d | OIRR | $V+ = 3.15 V$, $f = 1 MHz$, $R_L = 50 \Omega$, $C_L = 5 pF$ | Room | | - 70 | | dB |
| Crosstalk ^{d, f} | X _{TALK} | | Room | | - 90 | | GD |
| Bandwidth ^d | BW | $V+ = 3.15 \text{ V}, R_L = 50 \Omega, C_L = 5 \text{ pF}, -3 \text{ dB}$ | Room | | 190 | | MHz |
| Total Harmonic Distortion ^d | THD | V+ = 3.15 V, R_{LOAD} = 600 Ω | Room | | 0.02 | | % |
| | CS _{NC(off)} | V+ = 3.15 V, f = 1 MHz | | | 16 | | |
| N _O , N _C Off Capacitance ^d | CS _{NO(on)} | | Room | | 15 | | pF |
| Channel-On Capacitance ^d | C _{COM(on)} | | | | 31 | | |
| Power Supply | | | | | | | |
| Power Supply Range | V+ | | | 1.65 | | 4.3 | V |
| Power Supply Current | I+ | $V_{IN} = 0$ or V+ | Full | | | 1 | μΑ |

Notes:

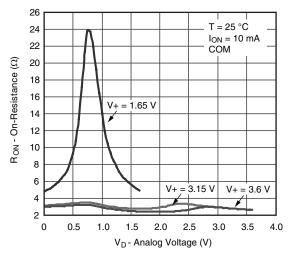
- a. Room = 25 $^{\circ}$ C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, not subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Crosstalk measured between channels.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

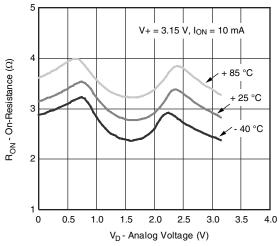
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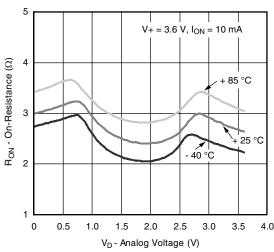
TYPICAL CHARACTERISTICS $T_A = 25$ °C, unless otherwise noted



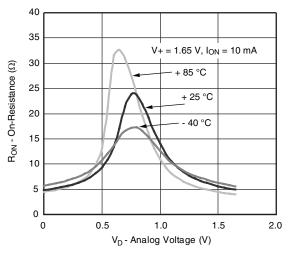
 $R_{ON} \ vs. \ V_D$ and Single Supply Voltage



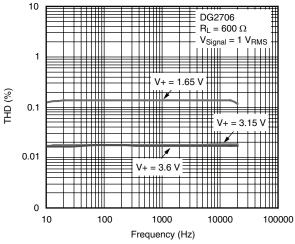
R_{ON} vs. Analog Voltage and Temperature



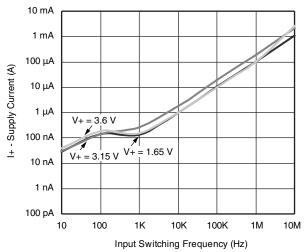
R_{ON} vs. Analog Voltage and Temperature



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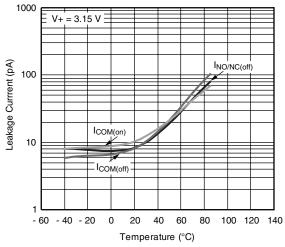
Switching Threshold vs. Supply Voltage

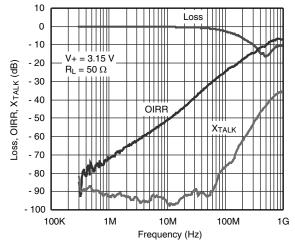


Supply Current vs. Input Switching Frequency



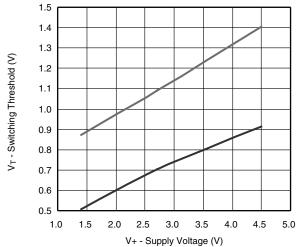
TYPICAL CHARACTERISTICS $T_A = 25$ °C, unless otherwise noted





Leakage Current vs. Temperature

Insertion Loss, Off-Isolation Crosstalk vs. Frequency

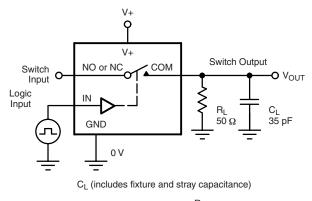


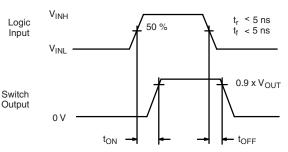
Switching Threshold vs. Supply Voltage

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TEST CIRCUITS





Logic "1" = Switch on Logic input waveforms inverted for switches that have the opposite logic sense.

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Figure 1. Switching Time

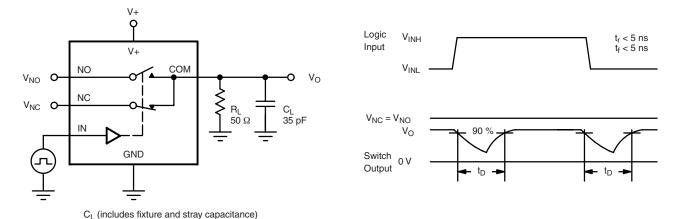


Figure 2. Break-Before-Make Interval

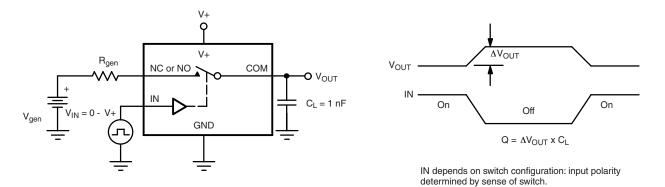


Figure 3. Charge Injection





TEST CIRCUITS

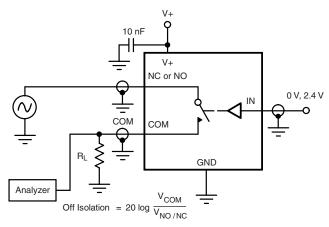


Figure 4. Off-Isolation

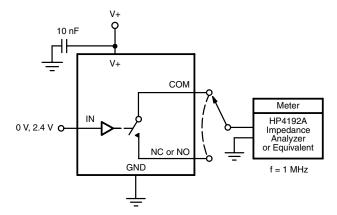


Figure 5. Channel Off/On Capacitance

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