

Improved Quad CMOS Analog Switches

DESCRIPTION

The DG308B/309B analog switches are highly improved versions of the industry-standard DG308A/309. These devices are fabricated in Vishay Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc.

An improved charge injection compensation design minimizes switching transients. The DG308B and DG309B can handle up to ± 22 V input signals. An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

The DG308B is a normally open switch and the DG309B is a normally closed switch. (See Truth Table.)

FEATURES

- ± 22 V Supply Voltage Rating
- CMOS Compatible Logic
- Low On-Resistance - $r_{DS(on)}$: 45 Ω
- Low Leakage - $I_{D(on)}$: 20 pA
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching - t_{ON} : < 200 ns
- Low Glitching - Q: 1 pC



RoHS*
COMPLIANT

BENEFITS

- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Superior to DG308A/309
- Space Savings (TSSOP)

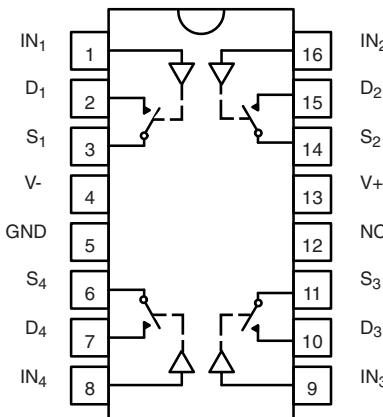
APPLICATIONS

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Disk Drives
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG308B

Dual-In-Line, SOIC and TSSOP



Top View

TRUTH TABLE

Logic	DG308B	DG309B
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5 V

Logic "1" ≥ 11 V

* Pb containing terminations are not RoHS compliant, exemptions may apply

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 °C	16-Pin PlasticDIP	DG308BDJ DG308BDJ-E3
		DG309BDJ DG309BDJ-E3
	16-Pin Narrow SOIC	DG308BDY DG308BDY-E3 DG308BDY-T1 DG308BDY-T1-E3
		DG309BDY DG309BDY-E3 DG309BDY-T1 DG309BDY-T1-E3
	16-Pin TSSOP	DG308BDQ DG308BDQ-E3 DG308BDQ-T1 DG308BDQ-T1-E3
		DG309BDQ DG309BDQ-E3 DG309BDQ-T1 DG309BDQ-T1-E3

ABSOLUTE MAXIMUM RATINGS

Parameter	Limit	Unit
Voltages Referenced, V+ to V-	44	V
GND	25	
Digital Inputs ^a , V _S , V _D	(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Current, Any Terminal	30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max)	100	
Storage Temperature	(AK Suffix)	°C
	(DJ, DY and DQ Suffix)	
Power Dissipation (Package) ^b	16-Pin Plastic DIP ^c	mW
	16-Pin Narrow SOIC and TSSOP ^d	
	16-Pin CerDIP ^e	

Notes:

- a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 6.5 mW/°C above 75 °C.
- d. Derate 7.6 mW/°C above 75 °C.
- e. Derate 12 mW/°C above 75 °C.



DG308B/309B

Vishay Siliconix

SPECIFICATIONS ^a									
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 15 \text{ V}$, $V_- = -15 \text{ V}$ $V_{IN} = 11 \text{ V}, 3.5 \text{ V}^f$	Temp ^b	Typ ^c	A Suffix -55 to 125 °C		D Suffix -40 to 85 °C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		-15	15	-15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = \pm 10 \text{ V}$, $I_S = 1 \text{ mA}$	Room	45		85		85	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Room	2					%
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 14 \text{ V}$, $V_D = \pm 14 \text{ V}$	Room Full	± 0.01	-0.5 -20	0.5 20	-0.5 -5	0.5 5	nA
Drain Off Leakage Current	$I_{D(off)}$	$V_D = \pm 14 \text{ V}$, $V_S = \pm 14 \text{ V}$	Room Full	± 0.01	-0.5 -20	0.5 20	-0.5 -5	0.5 5	
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = \pm 14 \text{ V}$	Room Full	± 0.02	-0.5 -40	0.5 40	-0.5 -10	0.5 10	
Digital Control									
Input, Voltage High	V_{INH}		Full		11		11		V
Input, Voltage Low	V_{INL}		Full			3.5		3.5	
Input Current	I_{INH} or I_{INL}	V_{INH} or V_{INL}	Full		-1	1	-1	1	μA
Input Capacitance	C_{IN}		Room	5					pF
Dynamic Characteristics									
Turn-On Time	t_{ON}	$V_S = 3 \text{ V}$, See Figure 2	Room			200		200	ns
Turn-Off Time	t_{OFF}		Room			150		150	
Charge Injection	Q	$C_L = 1000 \text{ pF}$, $V_g = 0 \text{ V}$, $R_g = 0 \Omega$	Room	1					pC
Source-Off Capacitance	$C_{S(off)}$	$V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$,	Room	5					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	5					
Channel-On Capacitance	$C_{D(on)}$	$V_D = V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$	Room	16					
Off-Isolation	OIRR	$C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, $V_S = 1 \text{ V}_{RMS}$, $f = 100 \text{ kHz}$	Room	90					dB
Channel-to-Channel Crosstalk	X_{TALK}		Room	95					
Power Supply									
Positive Supply Current	I_+	$V_{IN} = 0 \text{ V}$ or 15 V	Room Full			1 5		1 5	μA
Negative Supply Current	I_-		Room Full		-1 -5		-1 -5		
Power Supply Range for Continuous Operation	V_{OP}		Full		± 4	± 22	± 4	± 22	V

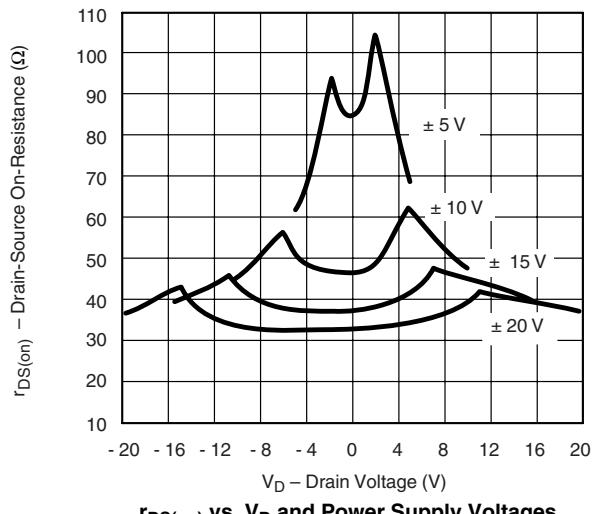
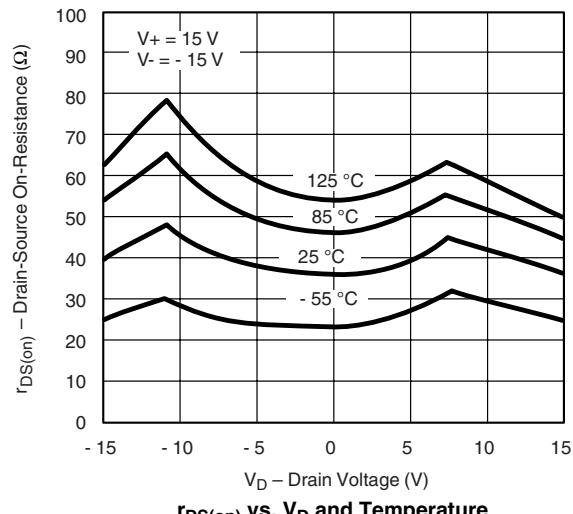
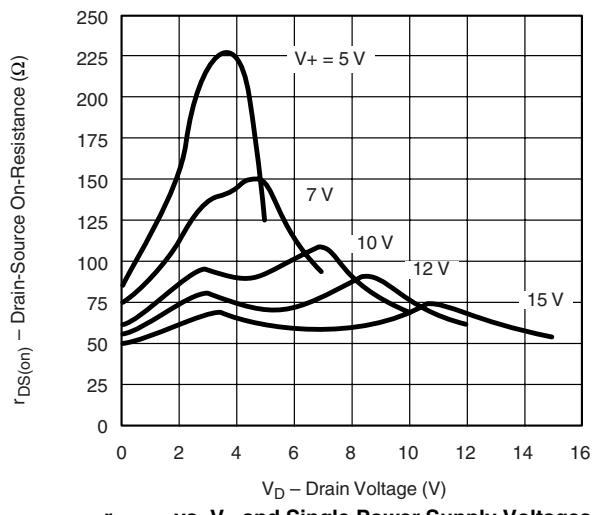
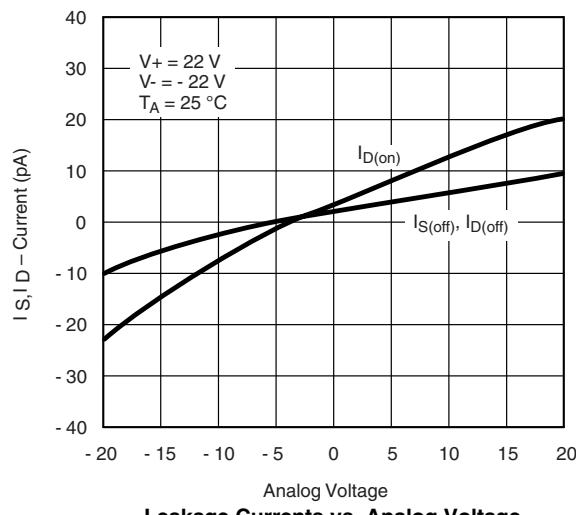
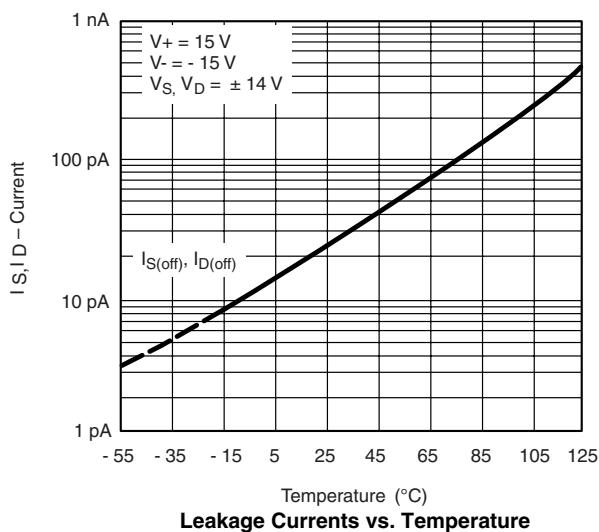
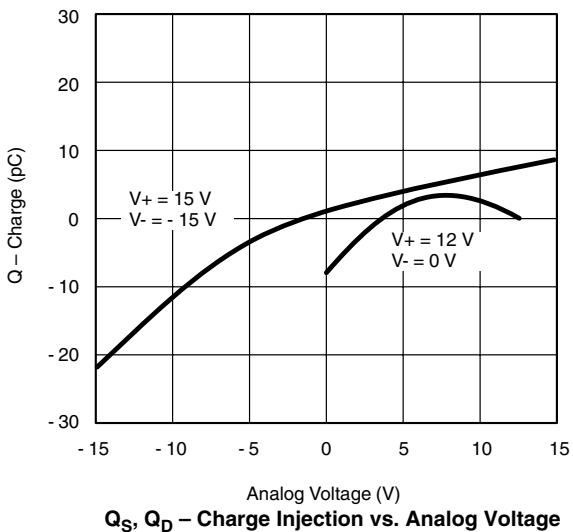
SPECIFICATIONS FOR SINGLE SUPPLY^a

Parameter	Symbol	Test Conditions Unless Specified $V_+ = 12 \text{ V}$, $V_- = 0 \text{ V}$ $V_{IN} = 11 \text{ V}, 3.5 \text{ V}^f$	Temp ^b	Typ ^c	A Suffix		D Suffix		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = 3 \text{ V}, 8 \text{ V}, I_S = 1 \text{ mA}$	Room Full	90		160 200		160 200	Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	$V_S = 8 \text{ V}$, See Figure 2	Room			300		300	ns
Turn-Off Time	t_{OFF}		Room			200		200	
Charge Injection	Q	$C_L = 1 \text{ nF}, V_{gen} = 6 \text{ V}, R_{gen} = 0 \Omega$	Room	4					pC
Power Supply									
Positive Supply Current	I+	$V_{IN} = 0 \text{ V or } 12 \text{ V}$	Room Full			1 5		1 5	μA
Negative Supply Current	I-		Room Full		- 1 - 5		- 1 - 5		
Power Supply Range for Continuous Operation	V_{OP}		Full		4	44	4	44	V

Notes:

- a. Refer to PROCESS OPTION FLOWCHART .
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

r_{DS(on)} vs. V_D and Power Supply Voltages

r_{DS(on)} vs. V_D and Temperature

r_{DS(on)} vs. V_D and Single Power Supply Voltages

Leakage Currents vs. Analog Voltage

Leakage Currents vs. Temperature

Q_s, Q_d – Charge Injection vs. Analog Voltage

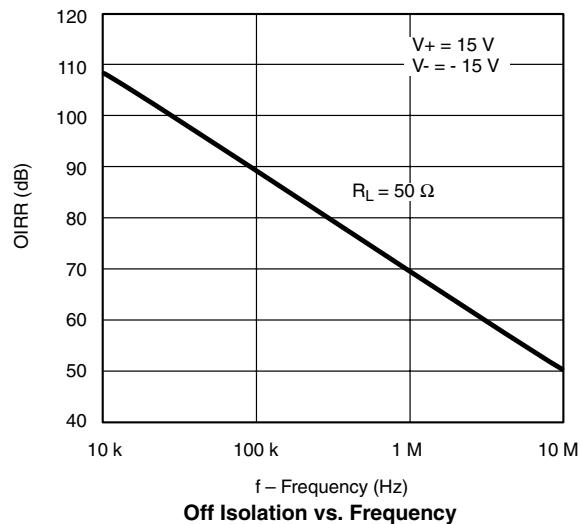
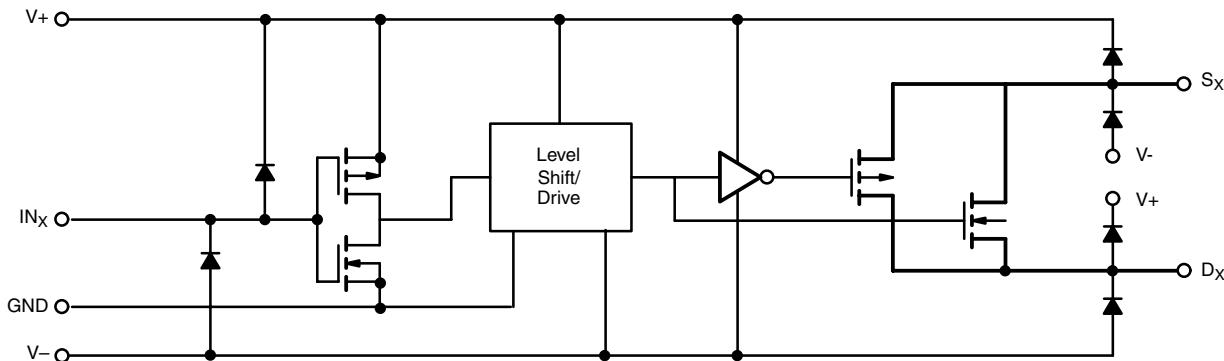
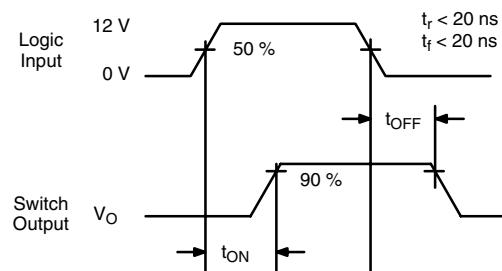
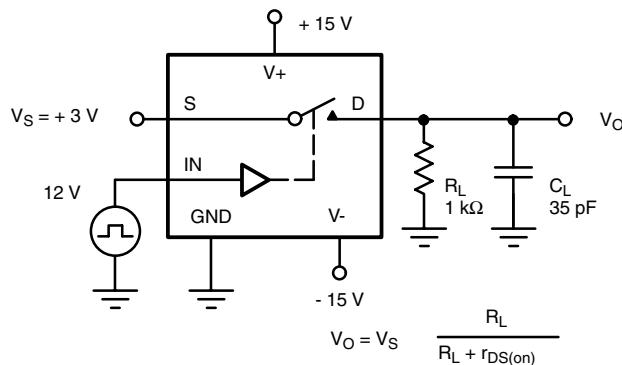
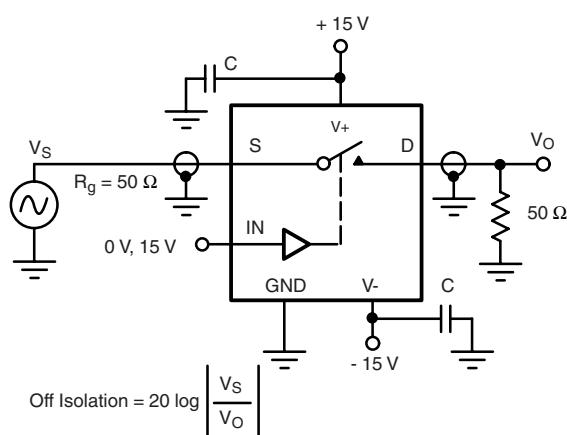
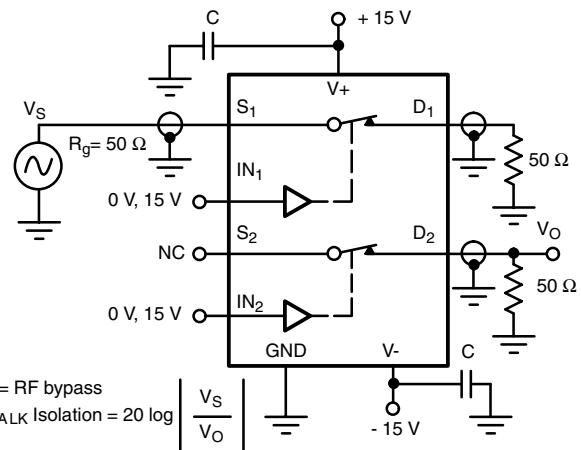
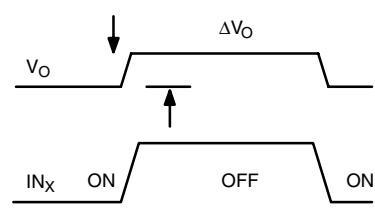
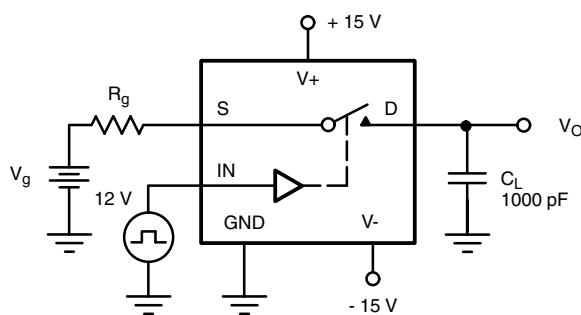
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**SCHEMATIC DIAGRAM (TYPICAL CHANNEL)**

Figure 1.

TEST CIRCUITS

Figure 2. Switching Time

Figure 3. Off Isolation

Figure 4. Channel-to-Channel Crosstalk

Figure 5. Charge Injection

ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $Q = C_L \times \Delta V_O$

APPLICATIONS

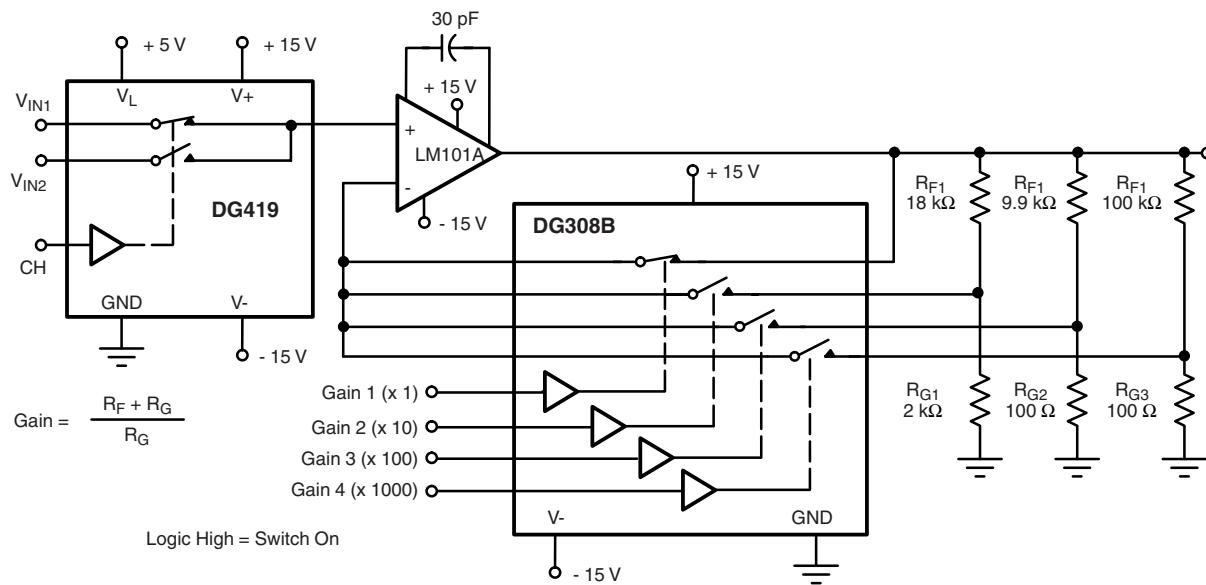


Figure 6. A Precision Amplifier with Digitally Programmable Inputs and Gains

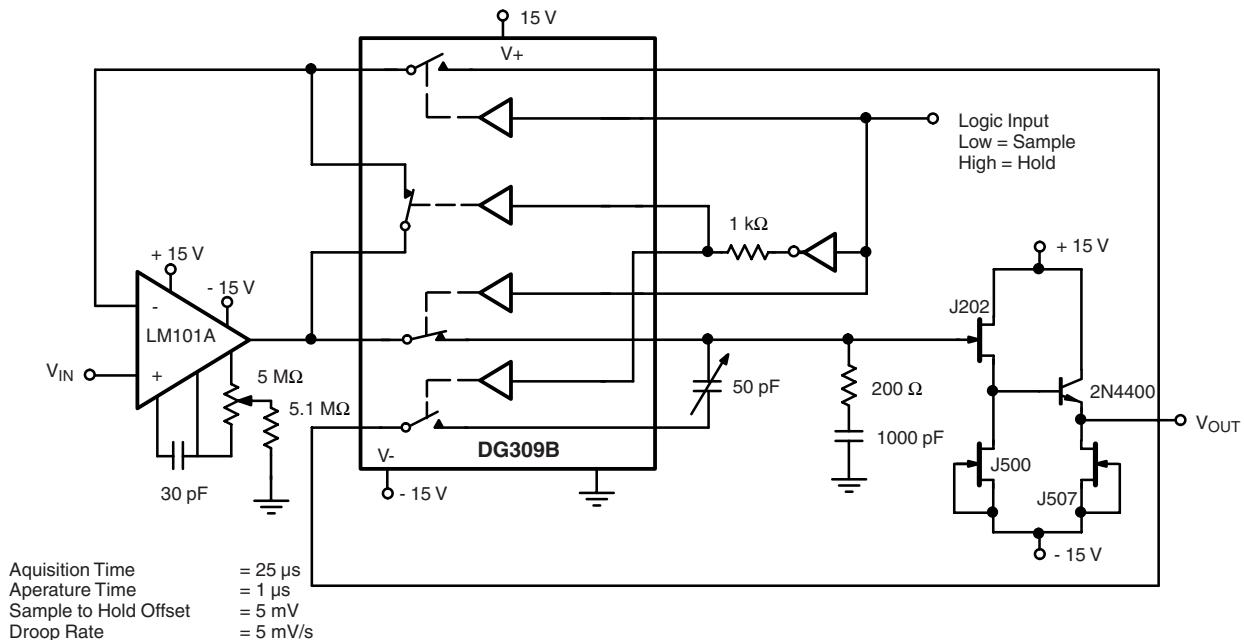
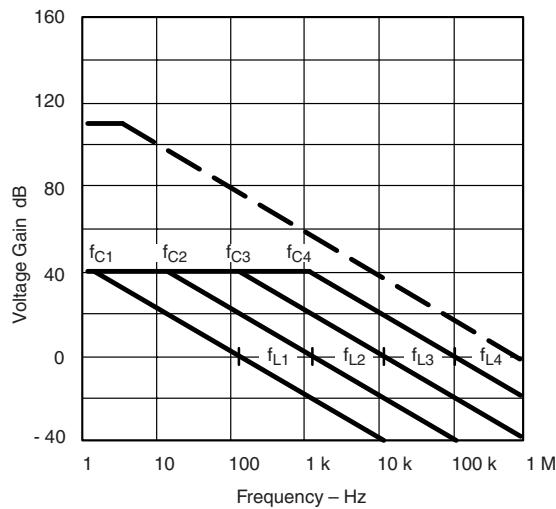
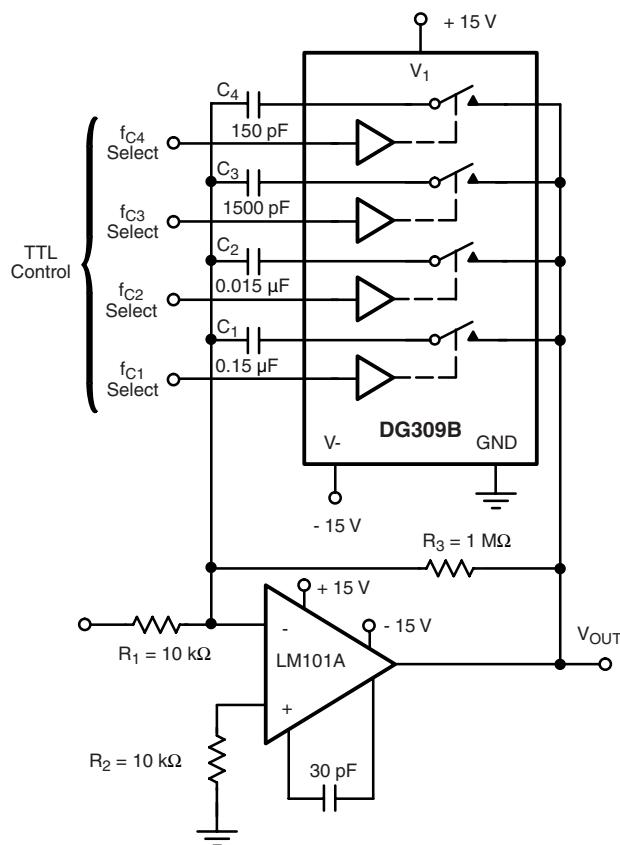


Figure 7. Sample-and-Hold

APPLICATIONS


$$A_L \text{ (Voltage Gain Below Break Frequency)} = \frac{R_3}{R_1} = 100 \text{ (40 dB)}$$

$$f_C \text{ (Break Frequency)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (Unity Gain Frequency)} = \frac{1}{2\pi R_1 C_X}$$

$$\text{Max Attenuation} = \frac{r_{DS(on)}}{10 \text{ k}\Omega} \approx -40 \text{ dB}$$

Figure 8. Active Low Pass Filter with Digitally Selected Break Frequency

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