16-Ch/Dual 8-Ch High-Performance CMOS Analog Multiplexers

DESCRIPTION

The DG406B is a 16-channel single-ended analog multiplexer designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address. The DG407B selects one of eight differential inputs to a common differential output. Break-before-make switching action protects against momentary shorting of inputs.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG406B/407B include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 volts, allowing operation with ± 20 V supplies. Additionally single (12 V) supply operation is allowed. An epitaxial layer prevents latchup.

FEATURES

- Low On-Resistance - $r_{DS(on)}$: 45 Ω
- Low Charge Injection - Q: 11 pC
- Fast Transition Time - t_{TRANS}: 115 ns
- Low Power: 0.2 mW
- Single Supply Capability

Pb-free Available

RoHS* COMPLIANT

BENEFITS

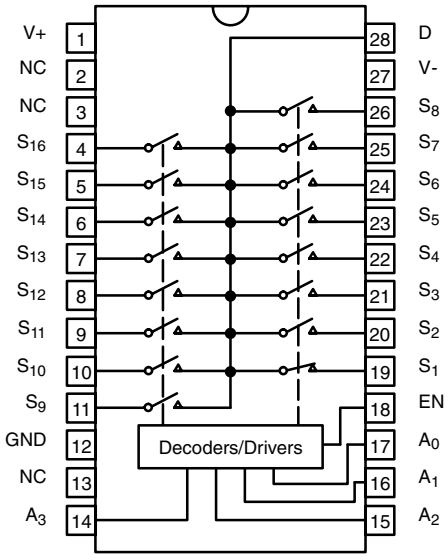
- Higher Accuracy
- Reduced Glitching
- Improved Data Throughput
- Reduced Power Consumption
- Increased Ruggedness
- Wide Supply Ranges: ± 5 V to ± 20 V

APPLICATIONS

- Data Acquisition Systems
- Audio Signal Routing
- Medical Instrumentation
- ATE Systems
- Battery Powered Systems
- High-Rel Systems
- Single Supply Systems

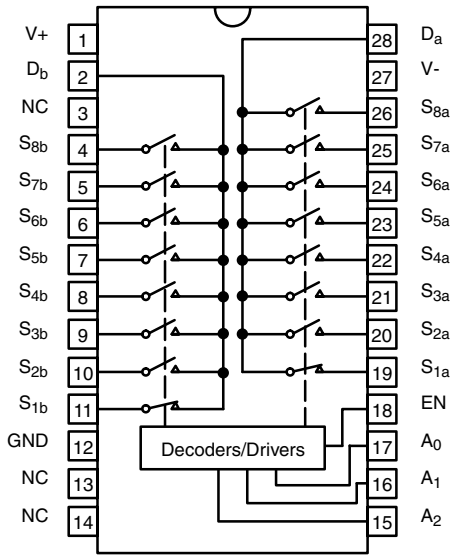
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG406B **Dual-In-Line and SOIC Wide-Body**



Top View

DG407B **Dual-In-Line and SOIC Wide-Body**

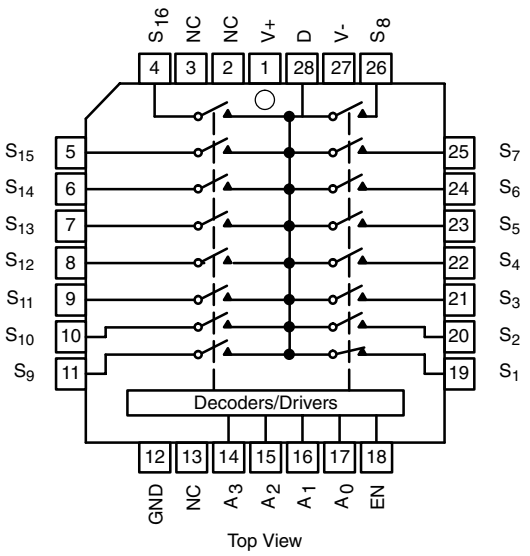


Top View

* Pb containing terminations are not RoHS compliant, exemptions may apply

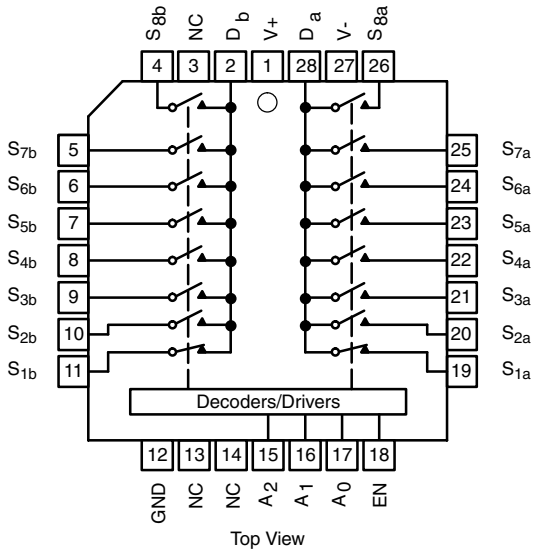
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG406B **PLCC and LCC**



Top View

DG407B **PLCC and LCC**



Top View

TRUTH TABLE - DG406B					
A_3	A_2	A_1	A_0	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

TRUTH TABLE - DG407B				
A_2	A_1	A_0	EN	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Do not Care

ORDERING INFORMATION - DG406B		
Temp Range	Package	Part Number
- 40 to 85 °C	28-Pin Plastic DIP	DG406BDJ DG406BDJ-E3
	28-Pin PLCC	DG406BDN DG406BDN-T1-E3
	28-Pin Widebody SOIC	DG406BDW DG406BDW-E3

ORDERING INFORMATION - DG407B		
Temp Range	Package	Part Number
- 40 to 85 °C	28-Pin Plastic DIP	DG407BDJ DG407BDJ-E3
	28-Pin PLCC	DG407BDN DG407BDN-T1-E3
	28-Pin Widebody SOIC	DG407BDW DG407BDW-E3

ABSOLUTE MAXIMUM RATINGS			
Parameter		**Limit**	**Unit**
Voltages Referenced to V-	V+	44	V
	GND	25	
Digital Inputs[a], V_S, V_D		(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first	
Current (Any Terminal)		30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % Duty Cycle Max)		100	
Storage Temperature		- 65 to 150	°C
Power Dissipation (Package)[b]	28-Pin Plastic DIP[c]	625	mW
	28-Pin CerDIP[d]	1.2	W
	28-Pin Plastic PLCC[c]	450	mW
	LCC-28[e]	1.35	W
	28-Pin Widebody SOIC[f]	450	mW

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 8.3 mW/°C above 75 °C.
d. Derate 16 mW/°C above 75 °C.
e. Derate 18 mW/°C above 75 °C.
f. Derate 6 mW/°C above 75 °C.

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp[b]	Typ[c]	A Suffix - 55 to 125 °C Min[d]	A Suffix - 55 to 125 °C Max[d]	D Suffix - 40 to 85 °C Min[d]	D Suffix - 40 to 85 °C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ± 10 V, I_S = - 10 mA Sequence Each Switch On		Room Full	45		60 87		60 74	Ω
$r_{DS(on)}$ Matching Between Channels[g]	$\Delta r_{DS(on)}$	V_D = ± 10 V		Room	5					%
Source Off Leakage Current	$I_{S(off)}$	V_{EN} = 0 V V_D = ± 10 V V_S = ± 10 V		Room Full		- 0.5 - 50	0.5 50	- 0.5 - 5	0.5 5	nA
Drain Off Leakage Current	$I_{D(off)}$		DG406B	Room Full		- 1 - 200	1 200	- 1 - 40	1 40	
			DG407B	Room Full		- 1 - 100	1 100	- 1 - 20	1 20	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ± 10 Sequence Each Switch On	DG406B	Room Full		- 1 - 200	1 200	- 1 - 40	1 40	
			DG407B	Room Full		- 1 - 100	1 100	- 1 - 20	1 20	
Digital Control										
Logic High Input Voltage	V_{INH}			Full		2.4		2.4		V
Logic Low Input Voltage	V_{INL}			Full			0.8		0.8	
Logic High Input Current	I_{AH}	V_A = 2.4 V, 15 V		Full		- 1	1	- 1	1	µA
Logic Low Input Current	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Full		- 1	1	- 1	1	
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	6					pF
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 2		Room Full	115		148 170		148 161	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 4		Room Full	39	10 29		10 21		
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3		Room Full	75		107 134		107 123	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room Full	50		88 98		88 94	
Charge Injection	Q	C_L = 1 nF, V_S = 0 V, R_S = 0 Ω		Room	11					pC
Off Isolation[h]	OIRR	V_{EN} = 0 V, R_L = 50 Ω f = 1 MHz		Room	- 86					dB
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 1 MHz		Room	6					pF
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V V_D = 0 V f = 1 MHz		Room	108					
			DG407B	Room	54					
Drain On Capacitance	$C_{D(on)}$		DG406B	Room	114					
			DG407B	Room	57					
Power Supplies										
Positive Supply Current	I+	V_{EN} = V_A = 0 or 5 V		Room Full	23		30 75		30 75	µA
Negative Supply Current	I-			Room Full	- 0.02	- 1 - 10		- 1 - 10		
Positive Supply Current	I+	V_{EN} = 2.4 V, V_A = 0 V		Room Full	28		500 900		500 700	
Negative Supply Current	I-			Room Full	- 0.01	- 20 - 20		- 20 - 20		

SPECIFICATIONS FOR SINGLE SUPPLY

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V- = 0 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp[b]	Typ[c]	A Suffix - 55 to 125 °C Min[d]	A Suffix - 55 to 125 °C Max[d]	D Suffix - 40 to 85 °C Min[d]	D Suffix - 40 to 85 °C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = 3 V, I_S = - 1 mA Sequence Each Switch On		Room	78		100		100	Ω
$r_{DS(on)}$ Matching Between Channels[g]	$\Delta r_{DS(on)}$			Room	5					%
Source Off Leakage Current[a]	$I_{S(off)}$	V_{EN} = 0 V		Room		- 0.5	0.5	- 0.5	0.5	nA
Drain Off Leakage Current[a]	$I_{D(off)}$	V_D = 10 V or 0.5 V, V_S = 0.5 V or 10 V	DG406B	Room		- 1	1	- 1	1	
			DG407B	Room		- 1	1	- 1	1	
Drain On Leakage Current[a]	$I_{D(on)}$	V_S = V_D = ± 10 V Sequence Each Switch On	DG406B	Room		- 1	1	- 1	1	
			DG407B	Room		- 1	1	- 1	1	
Dynamic Characteristics										
Switching Time of Multiplexer	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V, V_{IN} = 2.4 V		Room	130		163		163	ns
Enable Turn-On Time	$t_{ON(EN)}$	V_{INH} = 2.4 V, V_{INL} = 0 V V_{S1} = 5 V		Room	93		125		125	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room	63		94		94	
Charge Injection	Q	C_L = 1 nF, V_S = 6 V, R_S = 0		Room	9					pC
Power Supplies										
Positive Supply Current	I+	V_{EN} = 0 V or 5 V, V_A = 0 V or 5 V		Room Full	13		30 75		30 75	µA
Negative Supply Current	I-			Room Full	- 0.01	- 20 - 20		- 20 - 20		

Notes:

a. Guaranteed by ± 15 V leakage test, not production tested.

b. Room = 25 °C, Full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

e. Guaranteed by design, not subject to production test.

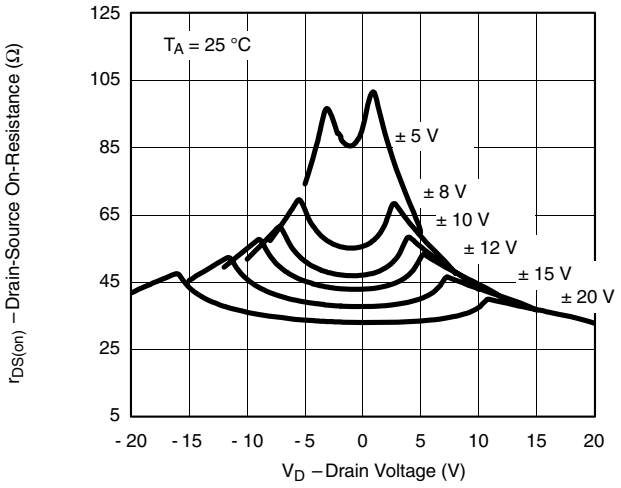
f. V_{IN} = input voltage to perform proper function.

g. $\Delta r_{DS(on)} = r_{DS(on)}$ MAX - $r_{DS(on)}$ MIN.

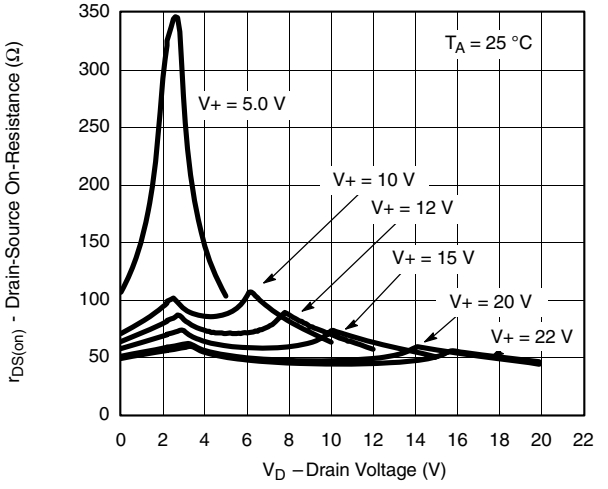
h. Worst case isolation occurs on Channel 4 due to proximity to the drain pin.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

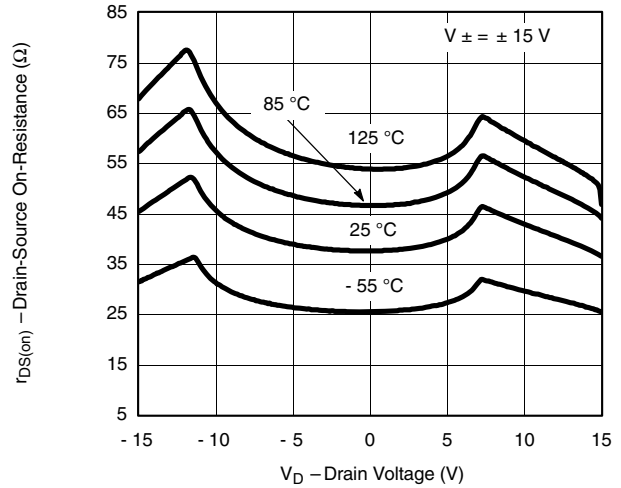
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



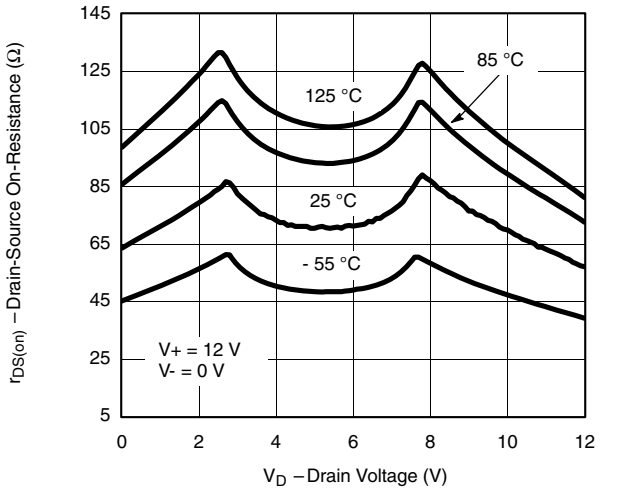
On-Resistance vs. V_D and Dual Supply Voltage



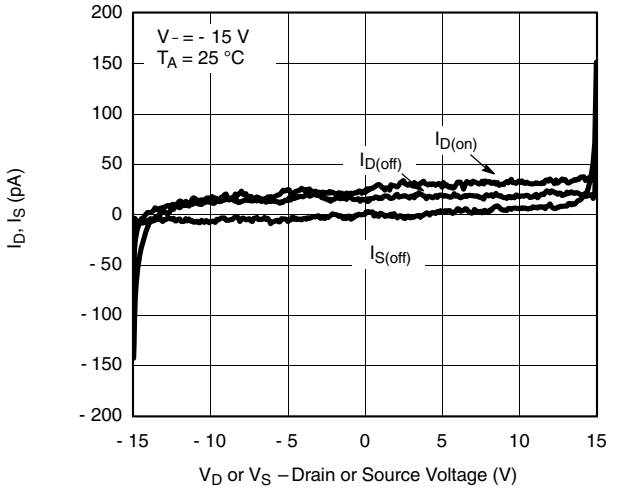
On-Resistance vs. V_D and Unipolar Supply Voltage



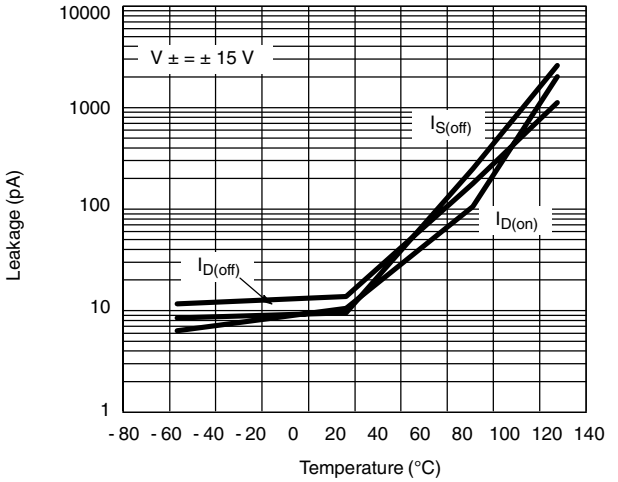
On-Resistance vs. V_D and Temperature



On-Resistance vs. V_D and Temperature

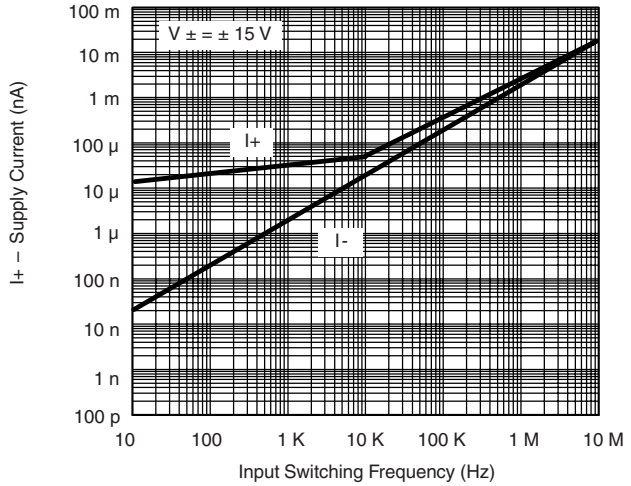


Leakage vs. Analog Voltage

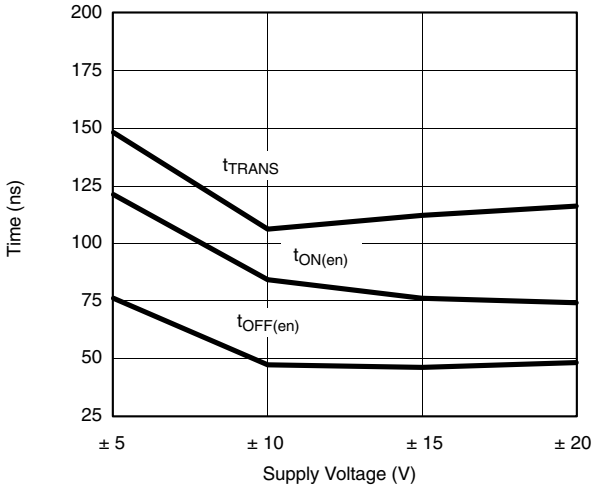


Leakage vs. Current

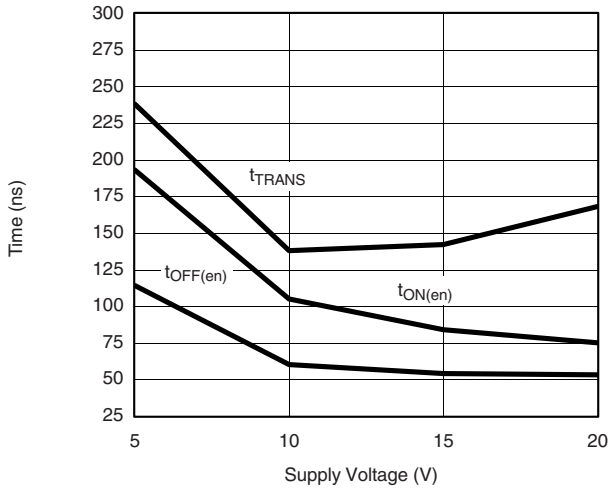
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



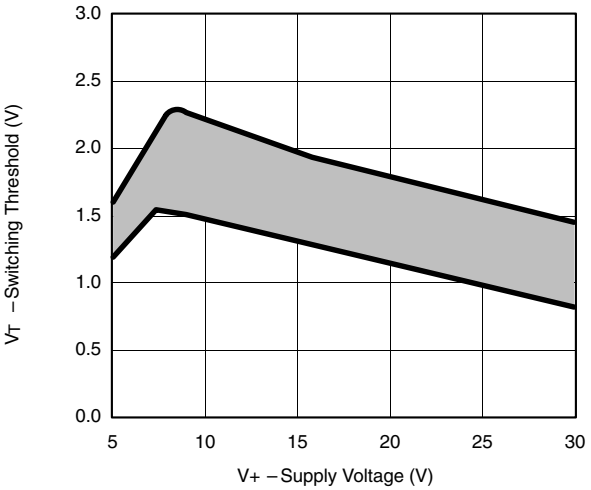
Supply Current vs. Input Switching Frequency



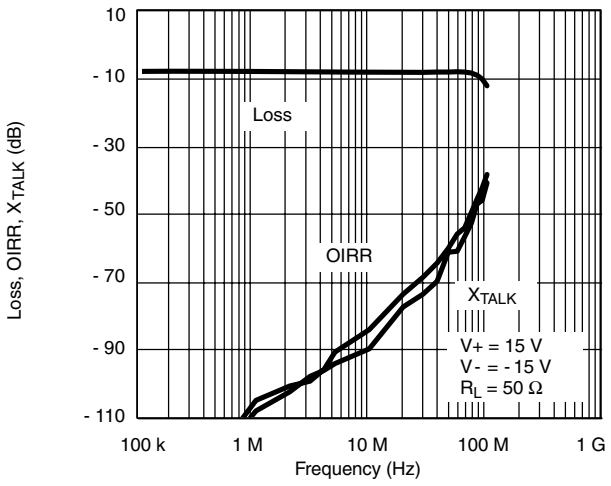
Switching Time vs. Bipolar Supplies



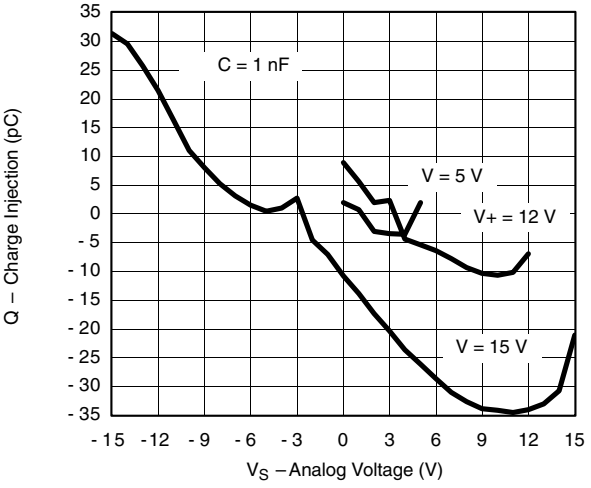
Switching Time vs. Single Supplies



Switching Threshold vs. Supply Voltage

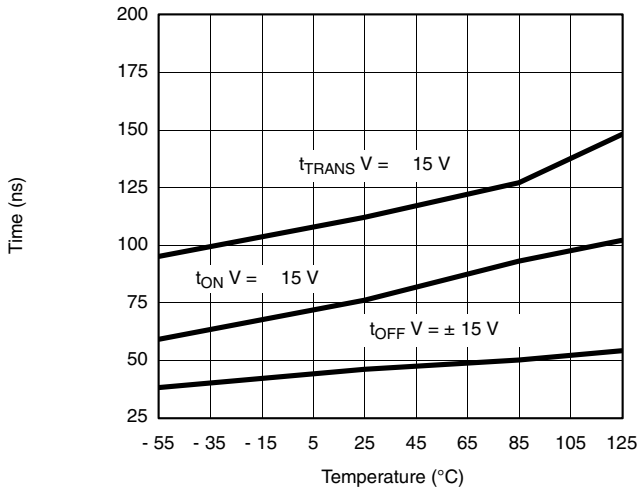


Insertion Loss, Off -Isolation
Crosstalk vs. Frequency



Charge Injection vs. Analog Voltage

TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



Switching Time vs. Temperature

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

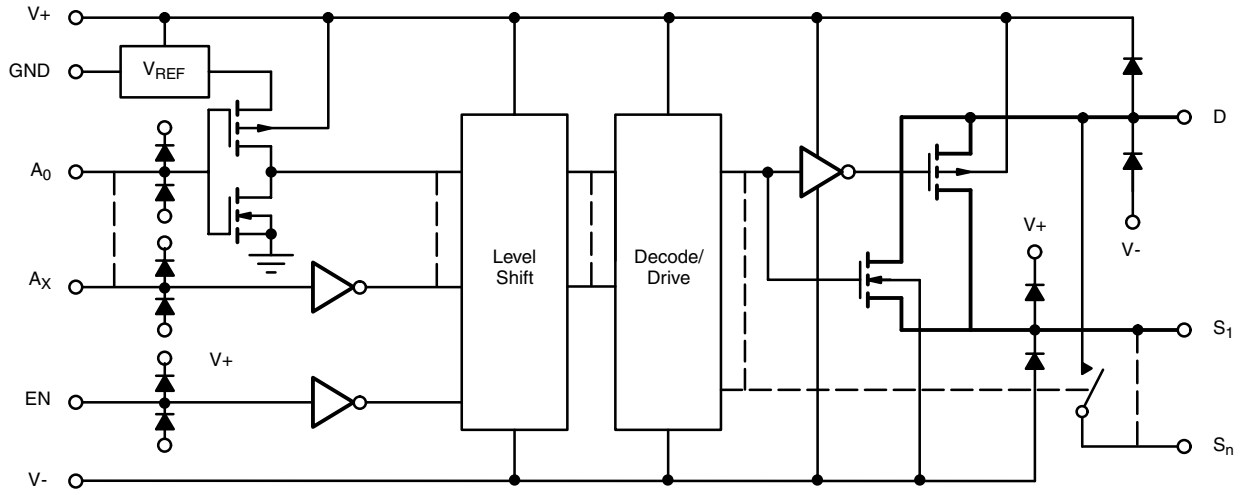
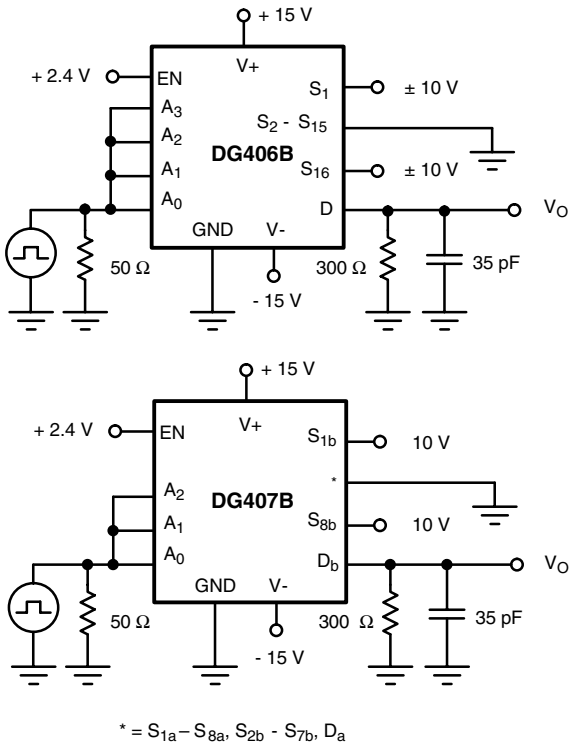


Figure 1.

TEST CIRCUITS



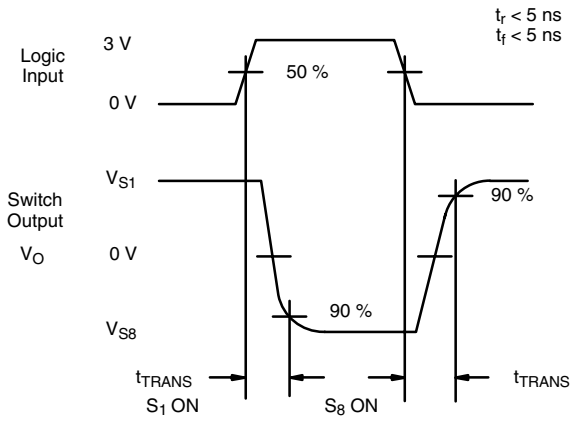
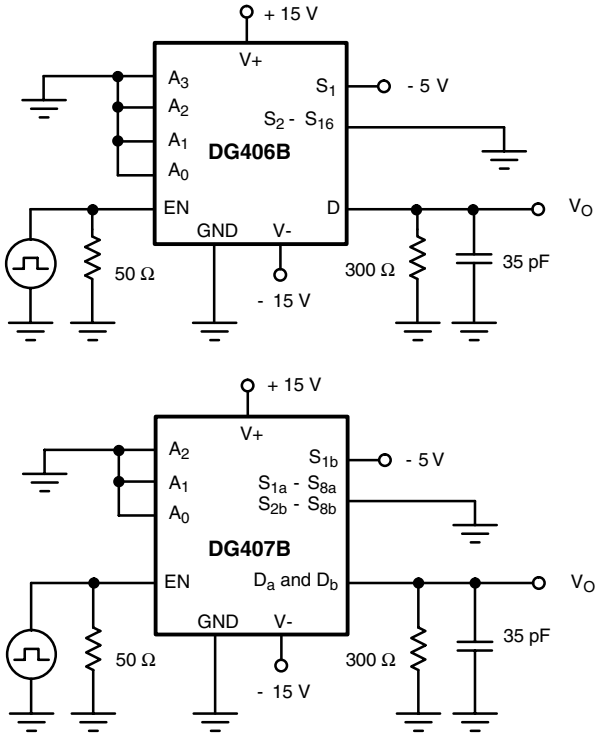


Figure 2. Transition Time



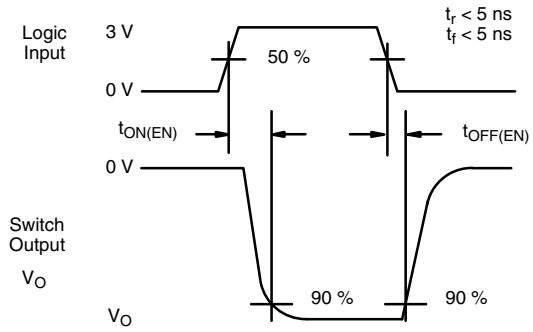


Figure 3. Enable Switching Time

TEST CIRCUITS

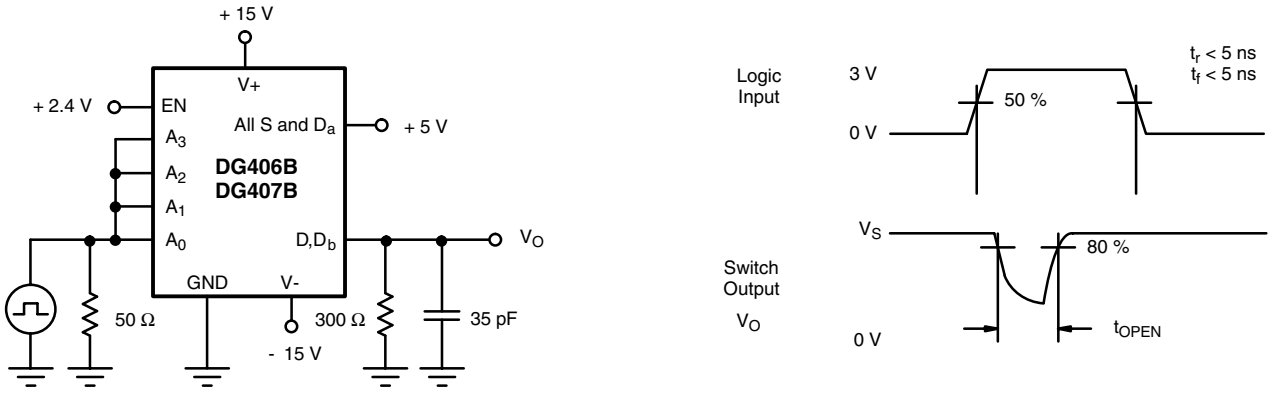


Figure 4. Break-Before-Make Interval

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72552.

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