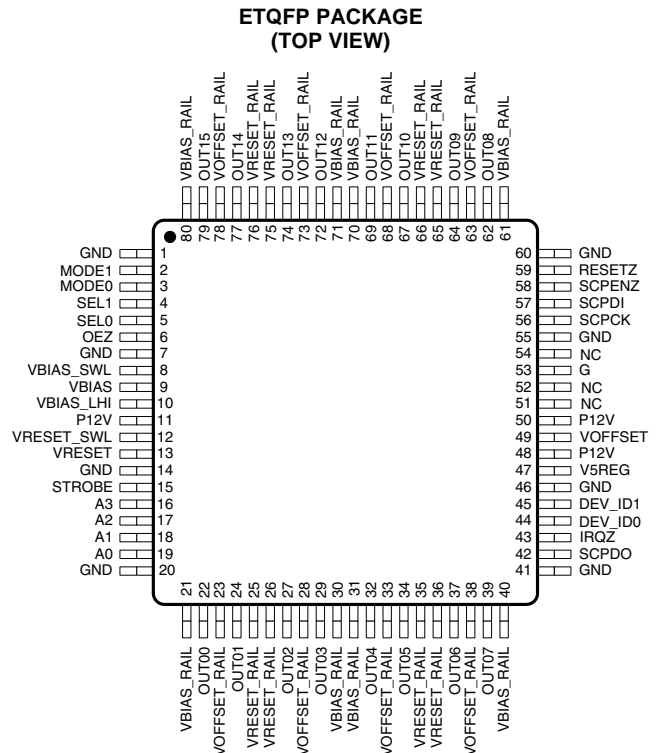


DLP® DLPA200 DMD Micromirror Driver

Check for Samples: [DLPA200](#)

FEATURES

- Designed for use as a part of a DLP Chipset
- Generates the Micromirror Clocking Pulses required by the DLP Digital Micromirror Device (DMD)
- Generates specialized voltage levels required for micromirror clocking pulse generation
- Operates from a single 12-V power supply
- Provides a V_{BIAS} voltage level, used by the DMD to control the array border mirrors
- Provides a V_{OFFSET} voltage level, used by the DMD as DMDVCC2
- All logic inputs are LVTTTL and CMOS compatible
- Packaged in an Pb-free Thermally Enhanced Surface-Mount Package: 80-pin, 0.5 mm-pitch, enlarged terminal pitch, thin profile quad flat pack (eTQFP)



DESCRIPTION

The DLPA200 is designed to be used as a part of a complete DLP chipset. A DLP chipset typically consists of a DMD, a DMD Controller, DMD Controller Firmware, and the DMD Micromirror Driver.

Within a chipset, the DLPR200 is responsible for generating micromirror clocking pulses. These clocking pulses (also referred to as micromirror reset pulses) are what cause the DMD micromirrors to switch from one binary landed state to another (as dictated by the binary contents of the DMD CMOS memory array).

A DMD Controller is responsible for writing data to the DMD CMOS memory array, and then commanding the DLPR200 to generate the required micromirror clocking pulses.

The DLPA200 consists of three functional blocks: A High-Voltage Power Supply function, a DMD Micromirror Clock Generation function, and a Serial Communication function.

The High-Voltage Power Supply function generates three specialized voltage levels: V_{BIAS} (19 to 28 V), V_{RESET} (–19 to –28 V), and V_{OFFSET} (4.5 to 10 V).

The Micromirror Clock Generation function uses the three voltages generated by the High-Voltage Power Supply function to create the sixteen micromirror clock pluses (output the OUTx pins of the DLPA200).

The Serial Communication function allows the chipset Controller to: control the generation of V_{BIAS} , V_{RESET} , and V_{OFFSET} ; control the generation of the micromirror clock pulses; status the general operation of the DLPA200.



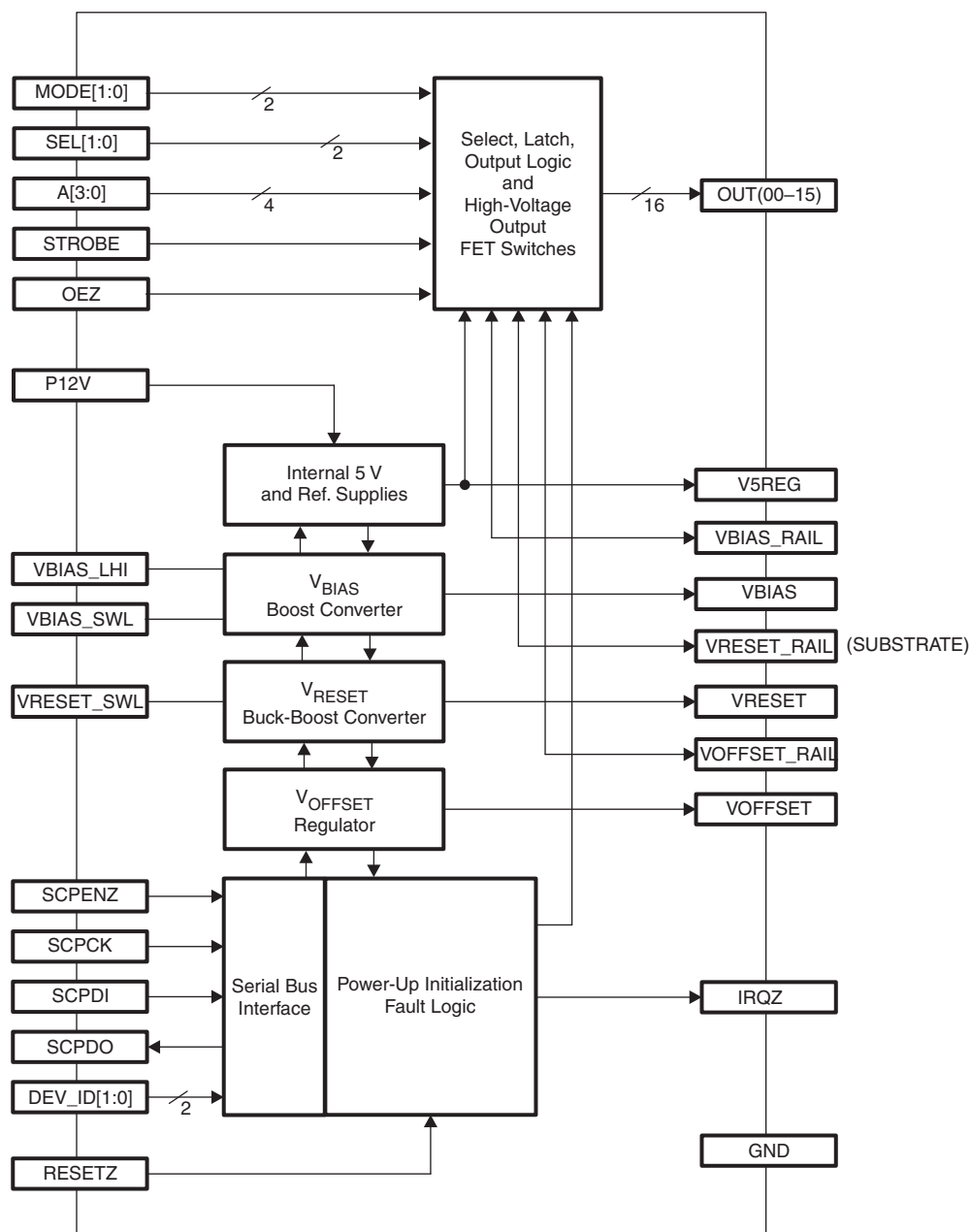
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DLP is a registered trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2010, Texas Instruments Incorporated

Functional Block Diagram



Device Marking

The device marking consists of the fields shown in [Figure 1](#).

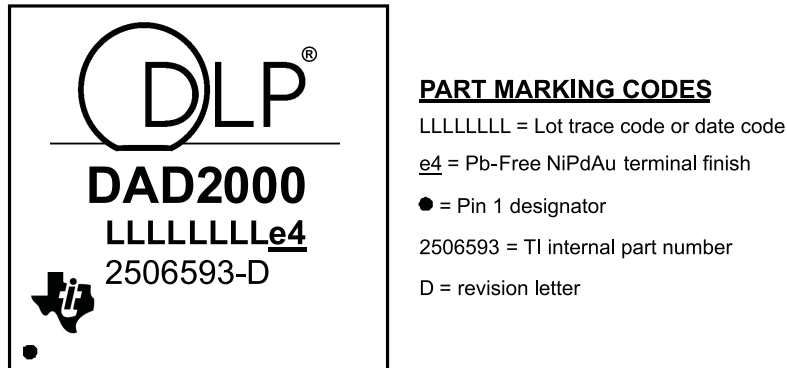


Figure 1. Device Marking (Device Top View)

TERMINAL FUNCTIONS

TERMINAL		I/O (INPUT DEFAULT)	DESCRIPTION
NAME	NO.		
OUT00	22	Output	16 micromirror clocking waveform outputs (enabled by $\overline{OE} = 0$).
OUT01	24	Output	
OUT02	27	Output	
OUT03	29	Output	
OUT04	32	Output	
OUT05	34	Output	
OUT06	37	Output	
OUT07	39	Output	
OUT08	62	Output	
OUT09	64	Output	
OUT10	67	Output	
OUT11	69	Output	
OUT12	72	Output	
OUT13	74	Output	
OUT14	77	Output	
OUT15	79	Output	
A0	19	Input (pull down)	Output Address. Used to select which OUTxx pin is active at a given time.
A1	18	Input (pull down)	
A2	17	Input (pull down)	
A3	16	Input (pull down)	
MODE0	3	Input (pull down)	Mode Select. Used to determine the operating mode of the DLPA200.
MODE1	2	Input (pull down)	
SEL0	5	Input (pull down)	Output Voltage Select. Used to switch the voltage applied to the addressed OUTxx pin.
SEL1	4	Input (pull down)	
STROBE	15	Input (pull down)	A rising edge on STROBE latches in the control signals after a tri-state delay.
\overline{OE}	6	Input (pull up)	Asynchronous input controls whether the 16 OUTxx pins are active or are in a high-impedance state. $\overline{OE} = 0$: Enabled. $\overline{OE} = 1$: High Z.
\overline{RESET}	59	Input (pull up)	Resets the DLPA200 internal logic. Active low. Asynchronous.
\overline{SCPEN}	58	Input (pull up)	Enables serial bus data transfers. Active low.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O (INPUT DEFAULT)	DESCRIPTION
NAME	NO.		
SCPDI	57	Input (pull down)	Serial bus data input. Clocked in on the falling edge of SCPCK.
SCPCK	56	Input (pull down)	Serial bus clock. Provided by chipset Controller.
SCPDO	42	Output	Serial bus data output (open drain). Clocked out on the rising edge of SCPCK. A 1kΩ pull up resistor to the Chip-Set Controller V _{DD} supply is recommended.
$\overline{\text{IRQ}}$	43	Output	Interrupt request output to the chipset Controller. Active low. A 1 kΩ pull up resistor to the Chip-Set Controller V _{DD} supply is recommended.
DEV_ID1	45	Input (pull up)	Serial bus device address: 00 = all; 01 = device 1; 10 = device 2; 11 = device 3.
DEV_ID0	44	Input (pull up)	
VBIAS	9	Power	One of three specialized voltages which are generated by the DLPA200.
VBIAS_LHI	10	Power	Current limiter output for VBIAS supply. (also the VBIAS switching inductor input)
VBIAS_SWL	8	Power	Connection point for VBIAS supply switching inductor.
VBIAS_RAIL	21, 30, 31, 40, 61, 70, 71, 80	Power (substrate)	The internally-used VBIAS supply rail. Internally isolated from VBIAS.
VRESET	13	Power	One of three specialized voltages which are generated by the DLPA200. The package thermal pad is tied to this voltage level.
VRESET_SWL	12	Power	Connection point for VRESET supply switching inductor..
VRESET_RAIL ⁽¹⁾	25, 26, 35,36, 65, 66, 75, 76	Power	The internally-used VRESET supply rail. Internally isolated from VRESET. ⁽¹⁾
VOFFSET	49	Power	One of three specialized voltages which are generated by the DLPA200.
VOFFSET_RAIL	23, 28, 33, 38, 63, 68, 73, 78	Power	The internally-used VOFFSET supply rail. Internally isolated from VOFFSET.
GND	1, 7, 14, 20, 41, 46, 53, 55, 60	Power	Common ground
V5REG	47	Power	The 5-volt logic supply output.
P12V	11, 48, 50	Power	The main power input to the DLPA200.
NC	51, 52, 54	No Connect	No connect

(1) Exposed thermal pad is internally connected to VRESET_RAIL.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under " [Absolute Maximum Ratings](#)" may cause permanent damage to the device. The [Absolute Maximum Ratings](#) are stress ratings only, and functional performance of the device at these or any other conditions beyond those indicated under " [Recommended Operating Conditions](#)" is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

CONDITIONS			MIN	TYP	MAX	UNIT
P12V	Load supply voltage				14	V
V _{RESET_S}	VRESET_SWL	Measured with respect to VRESET_RAIL			–1	V
V _{BIAS_R}	VBIAS_RAIL	Measured with respect to VRESET_RAIL			60	V
V _{OFFSET_R}	VOFFSET_RAIL	Measured with respect to VRESET_RAIL			40.5	V
V _{IN}	Logic inputs		–0.3		7	V
V _{OUT}	Open drain logic outputs				7	V
T _J	Maximum junction temperature				125	°C
T _A	Operating temperature range		0		75	°C
T _{STORE}	Storage temperature range		–55		150	°C
R _{C-j}	Thermal resistance	V _{BIAS} = 26 V, V _{RESET} = –26 V, V _{OFFSET} = 10 V, Output load = 390 pF and 39R on each output, Phase by one with global mode, Channel repetition frequency = 50 kHz, Additional external loads: I _{BIAS} = 5 mA, I _{OFFSET} = 30 mA, I _{5REG} = 30 mA		3		°C/W
ESD	Human Body Model				2	kV
	Charge Device Model				800	V

RECOMMENDED OPERATING CONDITIONS

at $T_A = 25^\circ\text{C}$, $P12V = 10.8\text{ V}$ to 13.2 V (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the [Recommended Operating Conditions](#). No level of performance is implied when operating the device above or below the [Recommended Operating Conditions](#) limits.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Control Logic						
V_{IL}	Low-level logic input voltage				0.8	V
V_{IH}	High-level logic input voltage		1.97			V
I_{IH}	High-level logic input current	$V_{IN} = 5\text{ V}$, input with pulldown. See terminal functions table.		40	50	μA
I_{IL}	Low-level logic input current	$V_{IN} = 0\text{ V}$, input with pullup. See terminal functions table.	-50	-40		μA
I_{IH}	High-level logic input leakage current	$V_{IN} = 0\text{ V}$, input with pulldown	-1		1	μA
I_{IL}	Low-level logic input leakage current	$V_{IN} = 5\text{ V}$, input with pullup	-1		1	μA
V_{OL}	Open drain logic outputs	$I = 4\text{ mA}$			0.4	V
I_{OL}	Logic output leakage current	$V = 3.3\text{ V}$			1	μA
Power						
I_{P12V1}	P12V supply current ⁽¹⁾	Global shadow at 50 kHz, OUT load = $39\ \Omega$ and 390 pF, $V5REG = 30\text{ mA}$, $V_{BIAS} = 26\text{ V}$ at 5 mA, $V_{OFFSET} = 10\text{ V}$ at 30 mA, $V_{RESET} = -26\text{ V}$		200		mA
I_{P12V2}		Outputs disabled and no external loads, $V_{BIAS} = 19\text{ V}$, $V_{OFFSET} = 4.5\text{ V}$, $V_{RESET} = -19\text{ V}$			22	mA
T_{JTSDR}	Thermal shutdown temperature	With device temperature rising	145	160	175	$^\circ\text{C}$
		Hysteresis	5	10	15	$^\circ\text{C}$
	Delta between thermal shutdown and thermal warning		5	10	15	$^\circ\text{C}$
$T_{JTW R}$	Thermal warning temperature	With device temperature rising	125	140	155	$^\circ\text{C}$
		Hysteresis	5	10	15	$^\circ\text{C}$

(1) During power up the inrush power supply current can be as high as 1 A for a momentary period of time.

ELECTRICAL CHARACTERISTICS

5-V Linear Regulator

$T_A = 25^\circ\text{C}$, $P12V = 10.8\text{ V}$ to 13.2 V (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V5REG$	Output voltage	Average voltage, $I_{out} = 4\text{ mA}$ to 50 mA	4.75	5	5.25	V
I_{IL}	Output current: internal logic		4		20	mA
I_{IE}	Output current: external circuitry		0		30	mA
I_{CL5}	Current limit		80			mA
V_{UV5}	Undervoltage threshold	$I_{out} = 50\text{ mA}$ $V5REG$ voltage increasing, $P12V = 5.4\text{ V}$		4.1		V
		$V5REG$ voltage falling, $P12V = 5.2\text{ V}$		3.9		
V_{RIP}	Output ripple voltage ⁽¹⁾				200	mVpk-pk
V_{OS5}	Voltage overshoot at start up				2	% $V5REG$
t_{ss}	Power up	Measured between 10 to 90% of $V5REG$			1	ms

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

ELECTRICAL CHARACTERISTICS

Bias Voltage Boost Converter

T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{RL} Output current: reset outputs	Load = 400pF, 39 Ω, repetition frequency = 50 kHz	0		18	mA
I _{QL} Output current: quiescent / drivers	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz			3	mA
I _{DL} Output current: DMD load		0		5	mA
I _{CLFB} Current limit flag	Corresponding current on output at P12V = 10.8 V	30			mA
I _{CLB} Current limit	Measured on input	330	376	460	mA
V _{UVB} VBIAS undervoltage threshold	Bias voltage falling	50		92	%VBIAS
V _{UVLHI} VBIAS_LHI undervoltage threshold	VBIAS_LHI voltage increasing		8		V
	VBIAS_LHI voltage falling		6.5		V
R _{DS} Boost switch R _{dson}	T _J = 25°C		2		Ω
V _{RIP} Output ripple voltage ⁽¹⁾				200	mVpk-pk
F _{SW} Switching frequency		1.35	1.5	1.65	MHz
V _{OSB} Voltage overshoot at start up				2	%VBIAS
t _{ss} Power up	C _{out} = 3.3 μF, Measured between 10 to 90% of target V _{BIAS}			1	ms
t _{dis} Discharge current sink		400			mA

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

ELECTRICAL CHARACTERISTICS

Reset Voltage Buck-Boost Converter

T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{RL} Output current: reset outputs	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz	0		18	mA
I _{QL} Output current: quiescent / drivers	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz			3	mA
I _{CLFR} Current limit flag	Corresponding current on output at P12V = 10.8 V	25			mA
I _{CLR} Current limit	Measured on input	400		800	mA
V _{UVR} Undervoltage threshold	Reset voltage falling	50		92	%VRESET
R _{DS} Buck-boost switch R _{dson}	T _J = 25°C		8		Ω
V _{RIP} Output ripple voltage ⁽¹⁾				200	mVpk-pk
F _{SW} Switching frequency		1.35	1.5	1.65	MHz
V _{OSR} Voltage overshoot at start up				2	%VRESET
t _{ss} Power up	C _{out} = 3.3 μF, Measured between 10 to 90% of target V _{RESET}			1	ms
t _{dis} Discharge current sink		400			mA

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

ELECTRICAL CHARACTERISTICS**V_{OFFSET}/DMDVCC2 Regulator**T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{RL}	Output current: reset outputs	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz	0		12.2	mA
I _{QL}	Output current: quiescent / drivers	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz			3	mA
I _{DL}	Output current: DMDVCC2		0		30	mA
I _{CLO}	Current limit		100			mA
V _{UVO}	Undervoltage threshold	V _{OFFSET} voltage falling	50		92	%V _{OFFSET}
V _{RIP}	Output ripple voltage ⁽¹⁾				100	mVpk-pk
V _{OSO}	Voltage overshoot at start-up				2	%V _{OFFSET}
t _{ss}	Power up	C _{out} = 4.7 μF, Measured between 10 to 90% of target V _{OFFSET}			1	ms
t _{dis}	Discharge time constant				100	μs

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

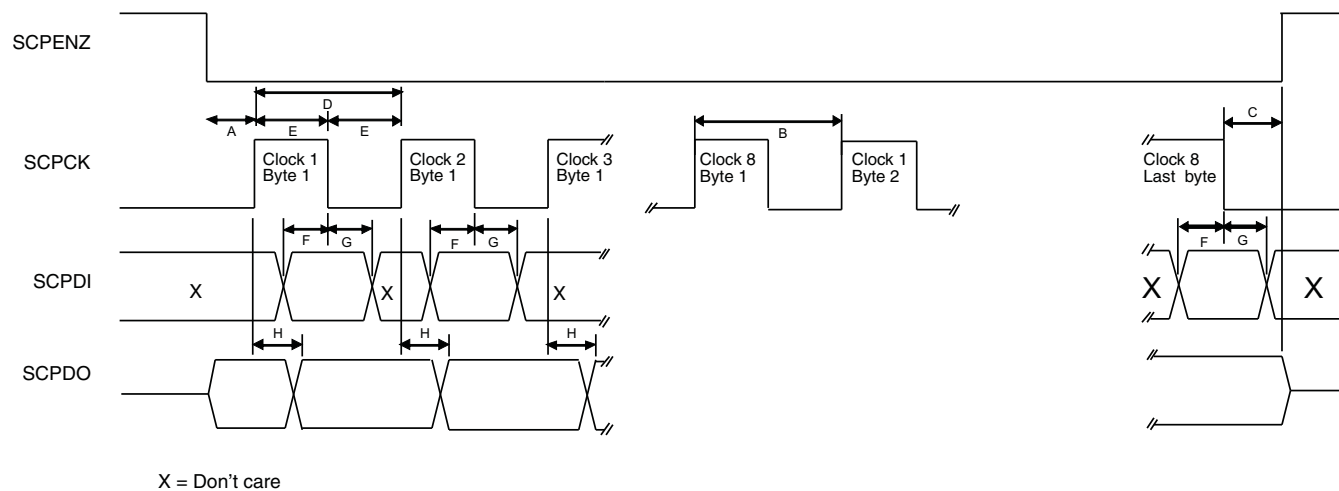
SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Serial Communication Port Interface						
A ⁽¹⁾	Setup $\overline{\text{SCPEN}}$ Low To SCPCK	Reference to rising edge of SCPCK	360			ns
B ⁽¹⁾	Byte To Byte Delay	Nominally 1 SCPCK cycle, rising edge to rising edge	1.9			μs
C ⁽¹⁾	Setup SCPDI To $\overline{\text{SCPEN}}$ High	Last byte to slave disable	360			ns
D ⁽¹⁾	SCPCK Frequency ⁽²⁾		0		526	kHz
	SCPCK Period		1.9	2		μs
E ⁽¹⁾	SCPCK High Or Low Time		300			ns
F ⁽¹⁾	SCPDI Set-Up Time	Reference to falling edge of SCPCK	300			ns
G ⁽¹⁾	SCPDI Hold Time	Reference from falling edge of SCPCK	300			ns
H ⁽¹⁾	SCPDO Propagation Delay	Reference from rising edge of SCPCK			300	ns
	$\overline{\text{SCPEN}}$, SCPCK, SCPDI, $\overline{\text{RESET}}$ Filter (Pulse Reject)		150			ns
Output Micromirror Clocking Pulses						
F _{PREP}	Phased reset repetition frequency each output pin (non-overlapping)				50	kHz
F _{GREP}	Global reset repetition frequency all output pins				50	kHz
I _{RLK}	VRESET output leakage current	$\overline{\text{OE}} = 1$, VRESET_RAIL = -28.5V		-1	-10	μA
I _{BLK}	VBIAS output leakage current	$\overline{\text{OE}} = 1$, VBIAS_RAIL = 28.5V		1	10	μA
I _{OLK}	VOFFSET output leakage current	$\overline{\text{OE}} = 1$, VOFFSET_RAIL = 10.25V		1	10	μA
Output Micromirror Clocking Pulse Controls						
t _{SPW}	STROBE Pulsewidth		10			ns
t _{SP}	STROBE Period		20			ns
t _{OHZ}	Output Time To High Z	$\overline{\text{OE}}$ Pin = High			100	ns
t _{OEN}	Output Enable Time From High Z	$\overline{\text{OE}}$ Pin = Low			100	ns
t _{SUS}	Set-Up Time	From A[3:0], MODE[1:0], and SEL[1:0] to STROBE edge	8			ns
t _{HOS}	Hold time	From A[3:0], MODE[1:0], and SEL[1:0] to STROBE edge	8			ns
t _{PBR}	Propagation time	From STROBE to VBIAS/VRESET edge 50% point.	80		200	ns
t _{PRO}		From STROBE to VRESET/VOFFSET edge 50% point.	80		200	ns
t _{POB}		From STROBE to VOFFSET/VBIAS edge 50% point.	80		200	ns
t _{DEL}	Edge-to-edge propagation delta	Maximum difference between the slowest and fastest propagation times for any given reset output.			40	ns
t _{CHCH}	Output channel-to-channel propagation delta	Maximum difference between the slowest and fastest propagation times for any two outputs for any given edge.			20	ns

(1) See [Figure 2](#)

(2) There is no minimum speed for the serial port. It can be written to statically for diagnostic purposes.

**Figure 2. Serial Interface Timing**

PRINCIPLES OF OPERATION

5-V Linear Regulator

The 5-V linear regulator supplies the 5 V requirement of the DLPA200 internal logic.

Figure 3 shows the block diagram of this module. The input de-coupling capacitors are shared with other internal DLPA200 modules. See [Component Selection Guidelines](#) for recommended component values.

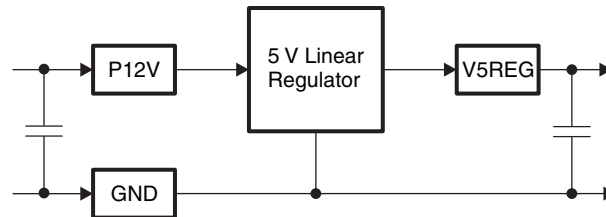


Figure 3. 5-Volt Linear Regulator Block Diagram

Bias Voltage Boost Converter

The bias voltage converter is a switching supply that operates at 1.5 MHz. The bias switching device switches 180° out-of-phase with the reset switching device.

The converter supplies the internal bias voltage for the high voltage FET switches and the external V_{BIAS} for the DMD border mirrors. The V_{BIAS} voltage level can be different for different generations of DMDs. The V_{BIAS} voltage level is configured by the DLP Controller chip over a serial communication interface. Four control bits select the voltage level while a fifth bit is the on/off control. The module provides two status bits to indicate latched and unlatched status bits for under-voltage (V_{UV}) and current-limit (C_L) conditions.

Figure 4 shows the block diagram of this module. The input de-coupling capacitors are shared with other internal DLPA200 modules. See [Component Selection Guidelines](#) for recommended component values.

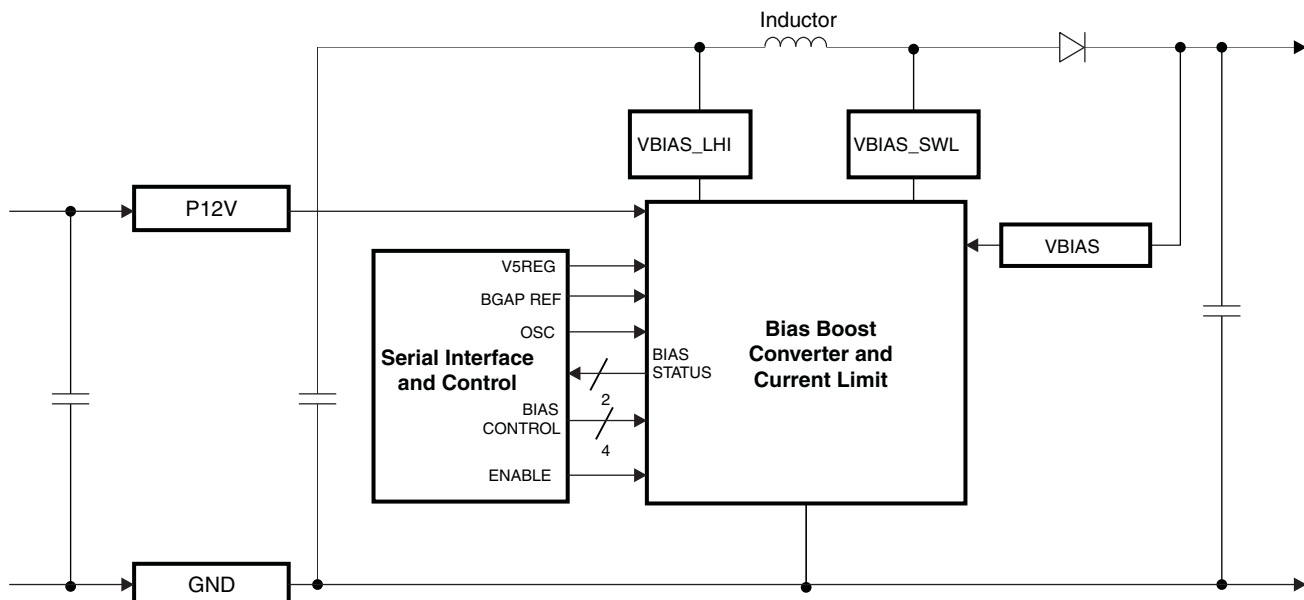


Figure 4. Bias Voltage Boost Converter Block Diagram

Reset Voltage Buck-Boost Converter

The reset voltage buck-boost converter is a switching supply that operates at 1.5 MHz. The reset switching device switches 180° out-of-phase with the bias switching device.

The converter supplies the internal reset voltage levels for the high voltage FET switches. The V_{RESET} voltage level can be different for different generations of DMDs. The V_{RESET} voltage level is configured by the DLP Controller chip over a serial communication interface. Four control bits select the voltage level while a fifth bit is the on/off control. The module provides two status bits to indicate latched and unlatched status bits for under-voltage (V_{UV}) and current-limit (C_L) conditions.

Figure 5 shows the block diagram of this module. The input de-coupling capacitors are shared with other internal DLPA200 modules. See [Component Selection Guidelines](#) for recommended component values.

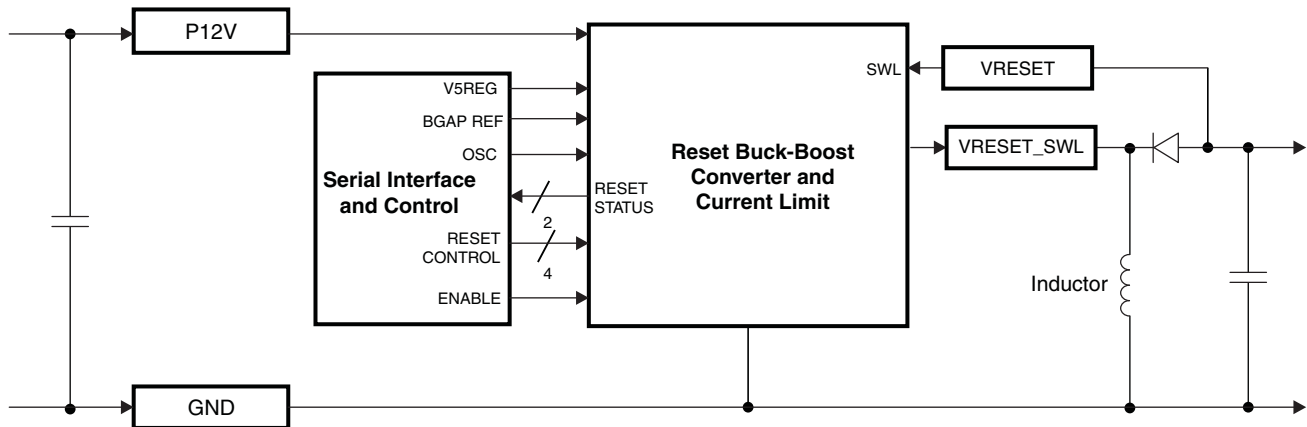


Figure 5. Reset Voltage Buck-Boost Converter Block Diagram

V_{OFFSET} /DMDVCC2 Regulator

The V_{OFFSET} /DMDVCC2 regulator supplies the internal V_{OFFSET} voltage for the high voltage FET switches and the external DMDVCC2 for the DMD. The V_{OFFSET} voltage level can be different for different generations of DMDs. The V_{OFFSET} voltage level is configured by the DLP Controller chip over a serial communication interface. Four control bits select the voltage level while a fifth bit is the on/off control. The module provides 2 status bits to indicate latched and unlatched status bits for under-voltage (V_{UV}) and current-limit (C_L) conditions.

Figure 6 shows the block diagram of this module. The input de-coupling capacitors are shared with other DLPA200 modules. See [Component Selection Guidelines](#) for recommended component values.

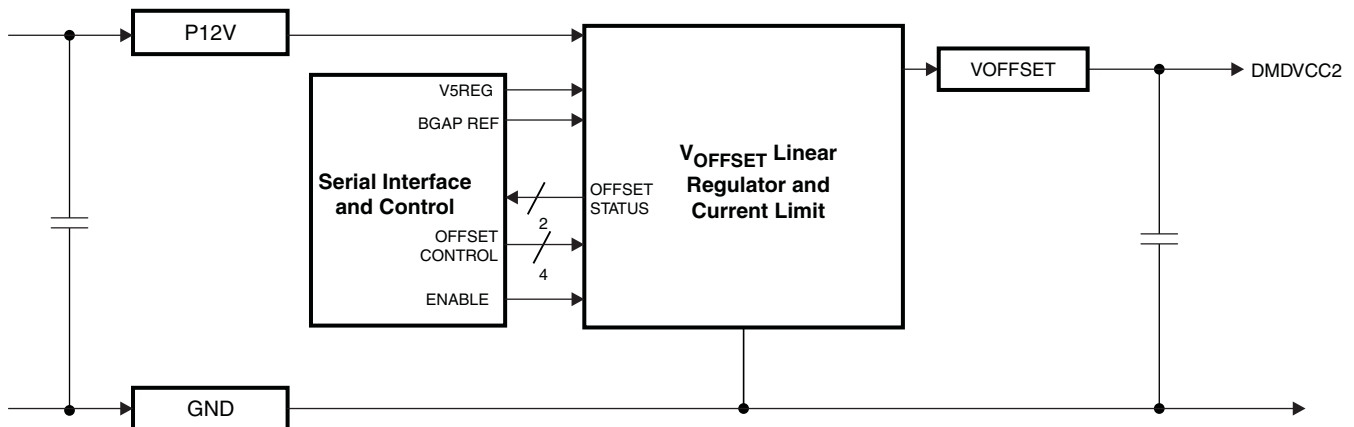


Figure 6. Offset Voltage Boost Converter Block Diagram

Driver Output Logic Block

The clocking waveform present on each OUTxx pin is managed by the DLP Controller chip, as shown in Figure 7.

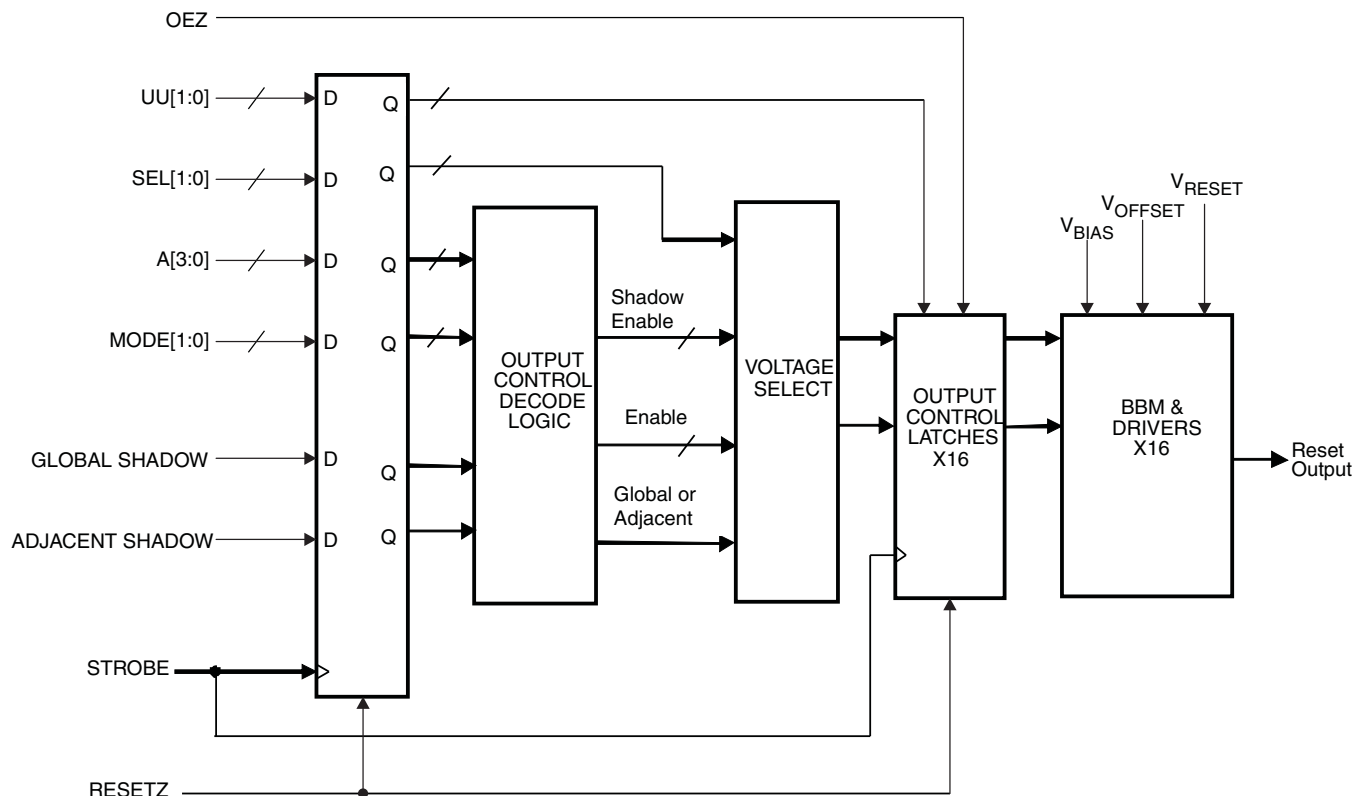


Figure 7. Driver Output Logic Block

PWB LAYOUT AND ROUTING GUIDELINES

WARNING

Board layout and routing guidelines must be followed explicitly and all external components used must be in the range of values and of the quality recommended for proper operation of the DLPA200. Important: Thermal pad(s) must be tied to VRESET_RAIL, do not connect to ground.

WARNING

Thermal pad(s) must be tied to VRESET_RAIL, do not connect to ground.

General Guidelines

Suitable Kelvin connections should be provided for the switching regulator feedback pins: VBIAS (pin 9) and VRESET (pin 13).

The etch traces that connect the switching devices: VBIAS_SWL (pin 8) and VRESET_SWL (pin 12) should be as short and wide as possible to minimize leakage inductances. The etch traces that connect the switching converter components (inductors, flywheel diodes and filtering capacitors) should also be as short and wide as possible. The electrical loops that these components form should be as small and compact as possible, with the ground referenced components forming a star connection.

Due to the fast switching transitions appearing on the sixteen reset OUTx pins, it is recommended to keep these traces as short as possible. Also, to minimize potential cross-talk between outputs, it is advisable to maintain as much clearance between each of the output traces.

Grounding Guidelines

The PWB should have an internal ground plane that extends under the DLPA200. All 9 ground pins (1, 7, 14, 20, 41, 46, 53, 55, and 60) must be connected to the ground plane using the shortest possible runs and vias. All filter and bypass capacitors must be placed near the pin being filtered or bypassed for the shortest possible runs to the part and to the ground plane.

Thermal Guidelines

The DLPA200 package should be thermally bonded or soldered to an external thermal pad on the PWB surface. The recommended dimensions of the thermal pad are 10 x 10 mm centered under the part. The metal bottom of the package is tied internally to the substrate at the VRESET_RAIL voltage level. Therefore, the thermal pad on the board must be isolated from any other extraneous circuit or ground and no circuit vias are allowed inside the pad area. Thermal pads are required on both sides of the PWB and should be connected together through an array of 5 x 5 thermal vias, 0.5 mm in diameter. **Thermal pads and the thermal vias are connected to VRESET_RAIL and isolated from ground, or any other circuit.** An internal P12V or VBB plane should be located directly underneath the top layer and have an isolated area under the DLPA200. This isolated area must be a minimum of 20 cm² and connect to the thermal pad of the DLPA200 through the thermal vias. The potential of the isolated area will also be at VRESET_RAIL. The internal ground plane should extend under the DLPA200 to help carry the heat away.

Careful consideration should be taken with respect to DLPA200 placement in the vicinity of local PWB hotspots. Heat generated from adjacent components may impact the DLPA200 thermal characteristics.

Power Supply Rail Guidelines

[Table 1](#) through [Table 5](#) provides discrete component selection guidelines.

The P12V filter and bypass capacitors should be distributed and connected to pin 11 and pins 48 & 50. These capacitors should be placed as near to their respective pins as possible and if necessary, should be placed on the bottom layer.

The V5REG filter and bypass capacitors must be placed near and connected to pin 47.

The VBIAS_RAIL etch runs should be routed in the following order: pin 40, pin 31, pin 30, pin 21, pin 80, pin 71, pin 70, and pin 61. The etch runs should be short and direct as they must carry 35 ns current spikes of up to 0.64 amps peak. Bypass capacitors should be located near and connected to pins 30 and 71 to provide bypassing on both sides.

The VBIAS_LHI filter and bypass capacitors must be placed near and connected to pin 10.

The VBIAS filter and bypass capacitors must be placed near and connected to pin 9. VBIAS pin 9 must also be connected (optionally with a 0-ohm resistor) to VBIAS_RAIL at or between pins 21 and 80.

The VRESET_RAIL etch runs should be routed in the following order: pin 36, pin 35, pin 26, pin 25, pin 76, pin 75, pin 66, and pin 65. The etch runs should be short and direct as they must carry 35 ns current spikes of up to 0.64 amps peak. Bypass capacitors should be placed near and connected to pins 35 and 66 to provide bypassing on both sides.

The VRESET filter and bypass capacitors must be located near and connected to pin 13. VRESET pin 13 must also be connected (optionally with a 0-ohm resistor) to VRESET_RAIL at or between pins 25 and 76.

The VOFFSET_RAIL etch runs should be routed in the following order: pin 23, pin 28, pin 33, pin 38, pin 63, pin 68, pin 73, and pin 78. The etch runs should be short and direct as they must carry 35 ns current spikes of up to 0.64 amps peak. Bypass capacitors should be placed near and connected to pins 28 and 73 to provide bypassing on both sides.

The VOFFSET filter and bypass capacitors must be placed near and connected to pin 49. VOFFSET pin 49 must also be connected (optionally with a 0-ohm resistor) to VOFFSET_RAIL at or between pins 38 and 63.

WARNING

Aluminum electrolytic capacitors may not be suitable for the DLPA200 application. At the switching frequencies used in the DLPA200 (up to 1.5MHz), aluminum electrolytic capacitors drop significantly in capacitance and increase in ESR resulting in voltage spikes on the power supply rails, which could cause the device to shut down or perform in an unreliable manner.

COMPONENT SELECTION GUIDELINES

Table 1. 5-V Regulator

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
P12V filter capacitor	10 to 33 μ F, 20 VDC, 1 Ω max ESR	Tantalum or ceramic	Pos: P12V, pin 11 (locate near pin 11)	Neg: Ground
P12V bypass capacitor	0.1 μ F, 50 VDC, 0.1 Ω max ESR	Ceramic	P12V, pin 11 (locate near pin 11)	Ground
V5REG filter capacitor	0.1 ⁽¹⁾ to 1.0 μ F, 10 VDC, 2.5 Ω max ESR	Tantalum or ceramic	Pos: V5REG, pin 47 (locate near pin 47)	Neg: Ground
V5REG bypass capacitor	0.1 μ F ⁽¹⁾ , 16 VDC, 0.1 Ω max ESR	Ceramic	V5REG, pin 47 (locate near pin 47)	Ground

(1) To ensure stability of the linear regulator, the capacitance should not be less than 0.1 μ F.

Table 2. Bias Voltage Boost Converter

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
LHI filter capacitor	10 μ F, 20 VDC, 1 Ω max ESR	Tantalum or ceramic	Pos: VBIAS_LHI, pin 10 (locate near pin 10)	Neg: Ground
LHI bypass capacitor	0.1 μ F, 50 VDC, 0.1 Ω max ESR	Ceramic	VBIAS_LHI, pin 10 (locate near pin 10)	Ground
VBIAS filter capacitor	1 to 10 μ F, 35 VDC, 1 Ω max ESR; (3.3 μ F nominal value)	Tantalum or ceramic	Pos: VBIAS, pin 9 (locate near pin 9)	Neg: Ground
VBIAS bypass capacitor	0.1 μ F, 50 VDC, 0.1 Ω max ESR	Ceramic	VBIAS, pin 9 (locate near pin 9)	Ground
VBIAS_RAIL bypass capacitors (2 required)	0.1 μ F, 50 VDC, 0.1 Ω max ESR	Ceramic	VBIAS_RAIL, pins 30 and 71 (locate near pins 30 and 71)	Ground
Resistor jumper (optional)	0-ohm normally (1 Ω for testing ⁽¹⁾)		VBIAS, pin 9	VBIAS_RAIL, pins 21 or 80
Inductor	22 μ H, 0.5 amp, 160 m Ω ESR	Coil Craft DT1608C-223 (or equivalent)	VBIAS_LHI, pin 10	VBIAS_SWL, pin 8
Schottky diode	0.5A, 40V (minimum)	Motorola MBR0540T1 or STMicroelectronics STPS0540Z, STPS0560Z (or equivalent)	Anode: VBIAS_SWL, pin 8	Cathode: VBIAS, pin 9

(1) Allows for VBIAS current measurement.

Table 3. Reset Voltage Boost Converter

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
VRESET filter capacitor	1 to 10 μ F, 35 VDC, 1 Ω max ESR; (3.3 μ F nominal value)	Tantalum or ceramic	Neg: VRESET, pin 13 (locate near pin 13)	Pos: Ground
VRESET bypass capacitor	0.1 μ F, 50 VDC, 0.1 Ω max ESR	Ceramic	VRESET, pin 13 (locate near pin 13)	Ground

Table 3. Reset Voltage Boost Converter (continued)

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
VRESET_RAIL bypass capacitors (2 required)	0.1 μ F, 50 VDC, 0.1 Ω max ESR	Ceramic	VRESET_RAIL, pins 35 and 66 (locate near pins 35 and 66)	Ground
Resistor jumper (optional)	0-ohm normally (1 Ω for testing ⁽¹⁾)		VRESET, pin 13	VRESET_RAIL, pins 25 or 76
Inductor	22 μ H, 0.5A, 160 m Ω	Coil Craft DT1608C-223 (or equivalent)	VRESET_SWL, pin 12	Ground
Schottky diode	0.5 A (minimum), 60 V	STMicroelectronics STPS0560Z or International Rectifier 10MQ060N (or equivalent)	Cathode: VRESET_SWL, pin 12	Anode: VRESET, pin 13

(1) Allows for VRESET current measurement.

Table 4. Offset Voltage Regulator

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
VOFFSET/VCC2 filter capacitors (2 required)	1.0 ⁽¹⁾ to 4.7 ⁽²⁾ μ F, 35 VDC, 1 Ω max ESR	Tantalum or ceramic	Pos: VOFFSET, pin 49 (1st near pin 49) Pos: DMDVCC2 pins (locate 2nd at DMD)	Neg: Ground at DLPA200 Neg: Ground at DMD
VOFFSET/VCC2 bypass capacitors (5 required)	0.1 μ F, 50 VDC, 0.1 Ω max ESR	Ceramic	VOFFSET, pin 49 (locate 1 near pin 49) DMD DMDVCC2 pins (locate 4 near DMD pins)	Ground at DLPA200 Ground at DMD
VOFFSET_RAIL bypass capacitor (2 required)	0.1 μ F, 50 VDC, 0.1 Ω max ESR	Ceramic	VOFFSET_RAIL, pins 28 and 73 (locate near pins 28 and 73)	Ground
Resistor jumper (optional)	0-ohm normal (1 Ω for testing ⁽³⁾)		VOFFSET, pin 49	VOFFSET_RAIL, pins 38 or 63
Resistor jumper (optional)	0-ohm normal (1 Ω for testing ⁽⁴⁾)		VOFFSET, pin 49	DMDVCC2 pins

(1) To ensure stability of the linear regulator, the absolute minimum output capacitance should not be less than 1.0 μ F.

(2) Recommended value is 3.3 μ F each. Different values are acceptable, provided that the sum of the two is 6.8 μ F maximum.

(3) Allows for VOFFSET current measurement

(4) Allows for DMDVCC2 current measurement

Table 5. Pullup Resistors

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
Resistor	1 k Ω		SCPDO, pin 42	Chipset controller 3.3-V V_{DD}
Resistor	1 k Ω		\overline{IRQ} , pin 43	Chipset Controller 3.3-V V_{DD}
Resistor (optional)	1 k Ω		\overline{OE} , pin 6	Chipset Controller 3.3-V V_{DD}

Revision History

REVISION	DATE	SECTION(S)	COMMENT
*	March 2010	All	Initial release
A	June 2010	Device Marking	Modified Device marking to show TI internal part number

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
DLPA200PFC	ACTIVE	TQFP	PFC	80	1	Pb-Free (RoHS)	Call TI	Level-2-260C-1 YEAR	Purchase Samples
DLPA200PFCT	ACTIVE	TQFP	PFC	80	10	Pb-Free (RoHS)	Call TI	Level-2-260C-1 YEAR	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

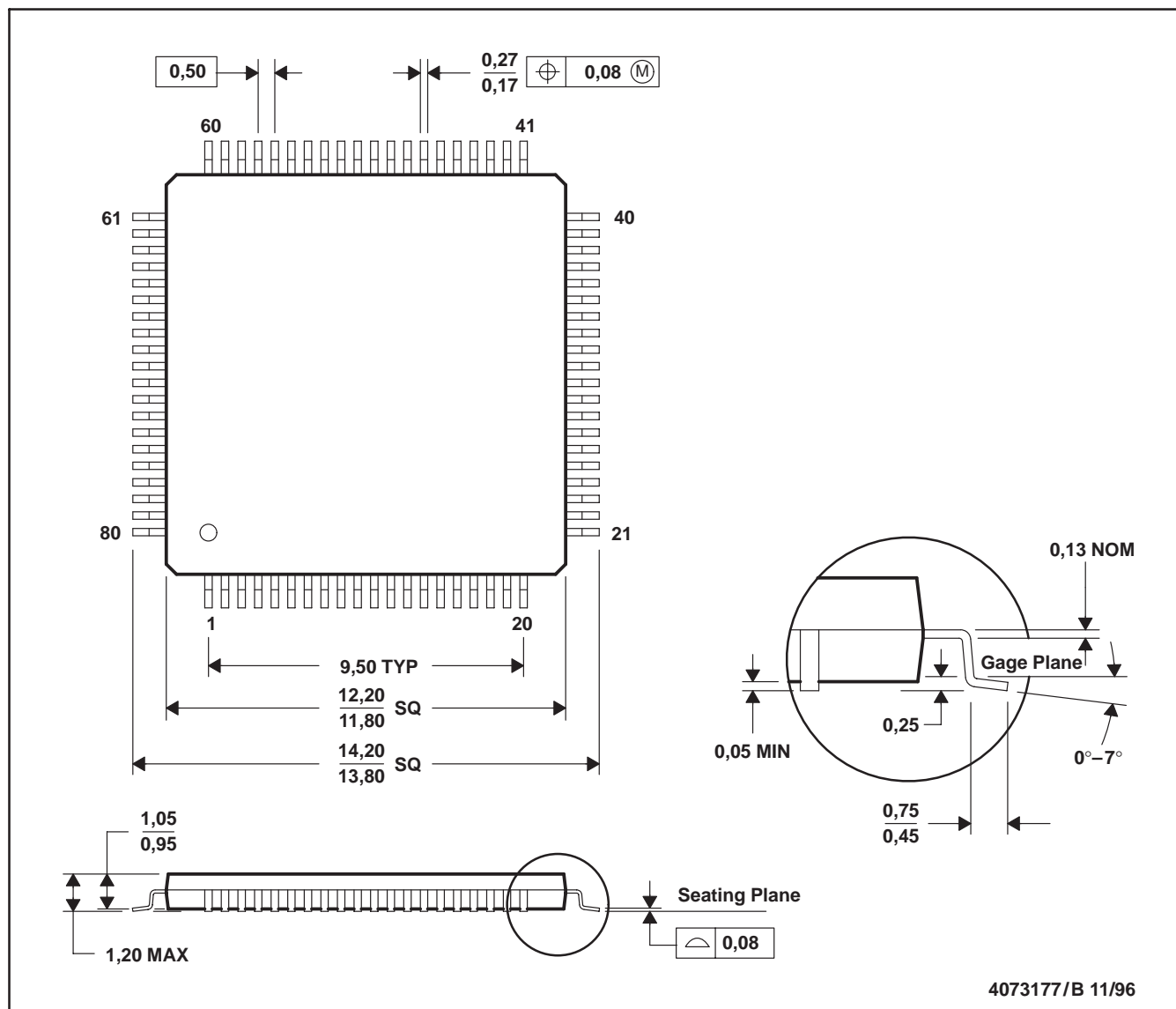
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PFC (S-PQFP-G80)

PLASTIC QUAD FLATPACK



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps