DLP® Digital Controller for the DLP5500 DMD

Check for Samples: DLPC200

FEATURES

- **Operates the DLPA200 and DLP5500**
- **Two 24-Bit Input Ports (RGB888) With Pixel Clock Support up to 80 MHz**
  - **Port 1 supports HDMI input**
  - **Port 2 supports input via an expansion card**
- **Supports EDID via I^2C**
- **Input Image Size 1024 x 768 (XGA)**
- **Device Configuration control interface**
  - **USB**
  - **SPI**
- **Video Input (via Port 1 or Port 2), 60 Hz:**
  - **Programmable Degamma**
  - **Spatial-Temporal Multiplexing (Dithering)**
- **Structured light pattern mode**
  - **Download Pattern Data directly to device**
  - **Display patterns up to 5000 Hz for binary patterns**
  - **Display patterns up to 700 Hz for 8 bits per pixel patterns**
  - **Programmable reordering of patterns**
- **200 MHz LVDS 1.0 (DDR) DMD Interface**
- **Supports three outputs for camera syncing**
- **Supports two inputs for external triggers**
- **Supports eight General Perpose I/O**
- **External Memory Support: 133 MHz DDR-2 SDRAM**
- **Serial FLASH Interface**
- **Parallel FLASH Interface**
- **System Control:**
  - **Programmable LED Current Control Adjustment of Red, Green, Blue and Infrared LEDs**
  - **Control of analog mirror driver (DLPA200)**
  - **DMD Horizontal and Vertical Image Flip**
  - **Built-in Test Pattern Generation**
  - **In-field Remote Download of Firmware Updates**
- **Packaged in 780-Pin Fineline Ball-Grid Array (FBGA)**

DESCRIPTION

The DLPC200 performs image processing and control, along with DMD data formatting, for driving a 0.55 XGA DMD (DLP5500).

The DLPC200 is one of three components in the 0.55 XGA Chipset (see Figure 1). Proper function and operation of the DLP5500 requires that it be used in conjunction with the other components of the 0.55 XGA Chip-Set. Refer to the 0.55 XGA Chip-Set Data Sheet for further details (TI literature number DLPZ004).

In DLP electronics solutions, image data is 100% digital from the DLPC200 input port to the image projected on to the display screen. The image stays in digital form and is never converted into an analog signal. The DLPC200 processes the digital input image and converts the data into a format needed by the DMD. The DMD then reflects light to the screen using binary pulse-width-modulation (PWM) for each pixel mirror.

The DLPC200 interfaces with an LED driver via an SPI interface. It sends strobes to indicate when each of the red, green, blue or infrared LEDs should be enabled or disabled and command packets are used to control the brightness of the LEDs.

Commands or programmable patterns can be input to the DLPC200 over either a SPI interface or an USB interface. When patterns are used the DLPC200 can be synchronized to a camera or external source. This allows the external interface to sync to the patterns displayed or for the patterns to be synchronized to the external source.

The DLCP200 allows the user to redefine the display order of the patterns that have been downloaded to memory. This allows any pattern stored in memory to be displayed in any order. Degamma and dithering are never applied to patterns but can be applied to data processed through either of the two pixel ports.

See Table 1 for frame rates that can be supported by the DLPC200.

Table 1. FRAME RATES

MODE		MIN	MAX	Unit
Structured Light	1 bit per pixel	6	5000	Hz
	8 bits per pixel		700	
Video		6	60	Hz

The digital input interface levels for image data is nominally 1.8 V or 3.3 V. Port 1 input is 3.3 V and Port 2 input is 1.8 V.

DLPR200F firmware is provided by Texas Instruments to support the operation of video and structured light mode. To locate DLPR200F, go to www.ti.com and search for the keyword “DLPR200”.

Related Documents

DOCUMENT	TI LITERATURE NUMBER
DLP 0.55 XGA Chip-Set data sheet	DLPZ004
DLPA200 DMD Analog Reset Driver	DLPS015
DLP5500 0.55 XGA DMD data sheet	DLPS013

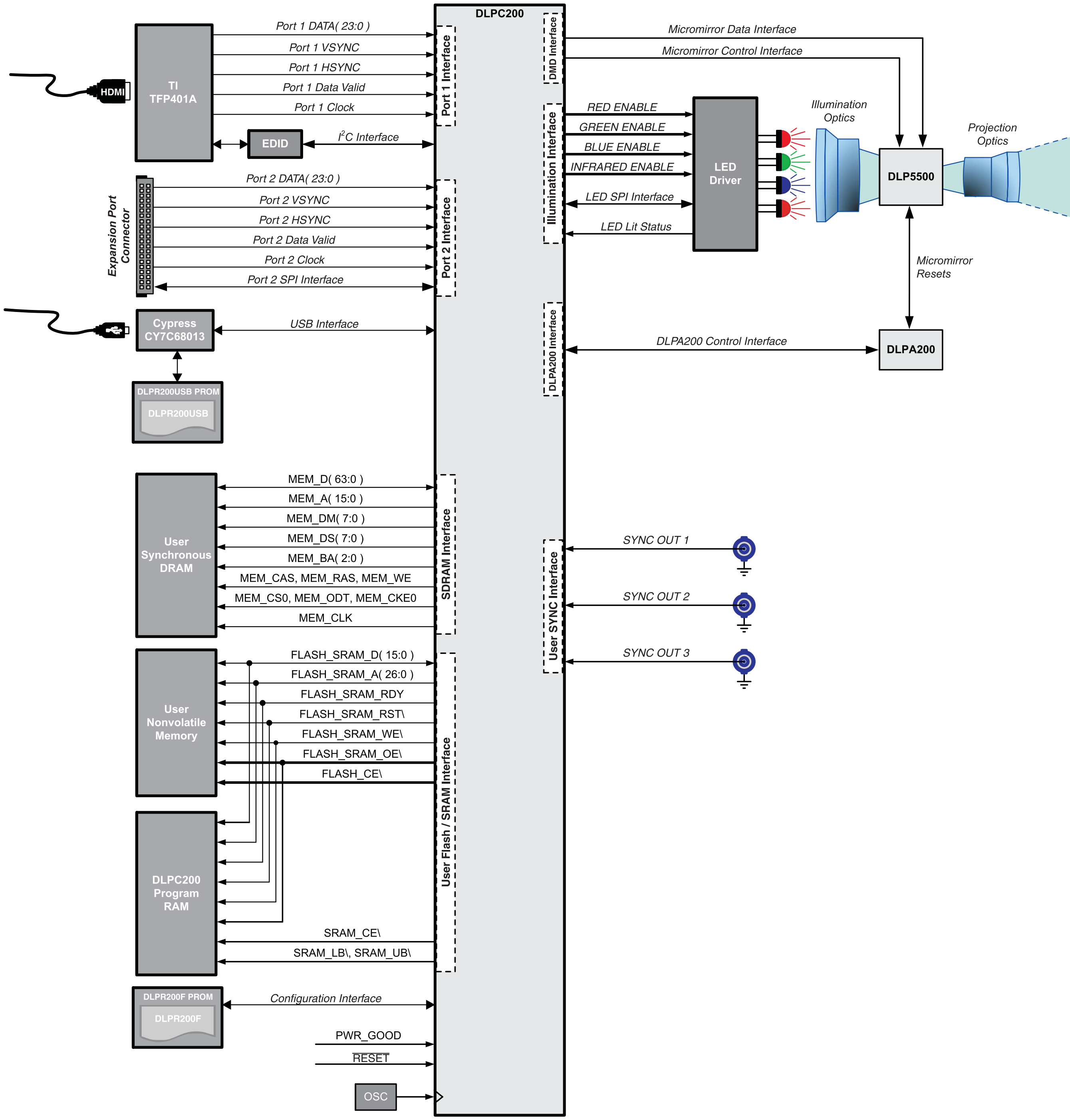


Figure 1. Typical Application

PROJECTOR IMAGE AND CONTROL PORT SIGNALS

The DLPC200 provides two input ports for graphics and motion video inputs. The signals listed below support the two input interface modes.

Below are the two input image interface modes, signal descriptions, and pins needed on the DLPC200.

- PORT 1, 28 pins (HDMI connector)
  - PORT1_D(23-0) – Projector Data
  - PORT1_VSYNC – Vertical Sync
  - PORT1_HSYNC – Horizontal Sync
  - PORT1_IVALID – Data Enable
  - PORT1_CLK – Projector Clock (rising edge, or falling edge, to capture input data)
- PORT 2, 28 pins (Expansion connector)
  - PORT2_D(23-0) – Projector Data
  - PORT2_VSYNC – Vertical Sync
  - PORT2_HSYNC – Horizontal Sync
  - PORT2_IVALID – Data Enable
  - PORT2_CLK – Projector Clock (rising edge, or falling edge, to capture input data)

Two control interfaces, USB and SPI, are provided to configure the DLPC200, as well as to transmit pattern data to memory for structured light mode. Below are the pins needed for the SPI and USB control interfaces.

- USB, 48 MHz
  - USB_CLK - USB clock
  - USB_CTRL1 - FIFO full flag
  - USB_CTRL2 - FIFO empty flag
  - USB_FD(15-0) - USB data
  - USB_PA02 - FIFO output enable for reads
  - USB_PA04 - FIFO address bit
  - USB_PA05 - FIFO address bit
  - USB_RDY1 - Write enable
  - USB_RDY0 - Read enable
- SPI, 5 MHz
  - SLAVE_SPI_CLK - SPI clock
  - SLAVE_SPI_ACK - busy signal that holds off additional transactions until the slave has completed processing data
  - SLAVE_SPI_MISO - output from slave
  - SLAVE_SPI_MOSI - output from master
  - SLAVE_SPI_CS - Slave select

Images are displayed via control of the DMD and DAD. The DLPC200 DMD interface consists of a 200 MHz (nominal) half bus DDR output-only interface with LVDS signaling. The serial communications port (SCP), 125 kHz nominal, is used to read or write control data to both the DMD and the DAD. The signals listed below support data transfer to the DMD and DAD.

- DMD, 200 MHz
  - DMD_CLK_AP, DMD_CLK_AN - DMD clock for A
  - DMD_CLK_BP, DMD_CLK_BN - DMD clock for B
  - DMD_DAT_AP, DMD_DAT_AN(1,3,5,7,9,11,13,15) - Data bus A (odd numbered pins are used for half bus)
  - DMD_DAT_BP, DMD_DAT_BN(1,3,5,7,9,11,13,15) - Data bus B (odd numbered pins are used for half bus)
  - DMD_SCRTL_AP, DMD_SCRTL_AN - S-control for A
  - DMD_SCRTL_BP, DMD_SCRTL_BN - S-control for B

- DAD, 125 kHz
  - SCP_DMD_RST_CLK - SCP clock
  - SCP_DMD_EN - enable DMD communication
  - SCP_RST_EN - enable DAD communication
  - SCP_DMD_RST_DI - input data
  - SCP_DMD_RST_DO - output data

The Terminal Functions table describes the input/output characteristics of signals that interface to the DLPC200 by functional groups.

TERMINAL FUNCTIONS

TERMINAL		I/O TYPE(1)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
Port 1 Video Data & Control(2)				
PORT1_CLK	J2	I_3		Pixel clock
PORT1_VSYNC	N3	I_3	PORT1_CLK	Vertical Sync; weak pull-up applied
PORT1_HSYNC	P1	I_3	PORT1_CLK	Horizontal Sync; weak pull-up applied
PORT1_IVALID	P2	I_3	PORT1_CLK	Data Valid
PORT1_D0	D2	I_3	PORT1_CLK	Pixel Data - Blue 0
PORT1_D1	D3	I_3	PORT1_CLK	Pixel Data - Blue 1
PORT1_D2	F5	I_3	PORT1_CLK	Pixel Data - Blue 2
PORT1_D3	D1	I_3	PORT1_CLK	Pixel Data - Blue 3
PORT1_D4	F3	I_3	PORT1_CLK	Pixel Data - Blue 4
PORT1_D5	G4	I_3	PORT1_CLK	Pixel Data - Blue 5
PORT1_D6	F1	I_3	PORT1_CLK	Pixel Data - Blue 6
PORT1_D7	G3	I_3	PORT1_CLK	Pixel Data - Blue 7
PORT1_D8	H5	I_3	PORT1_CLK	Pixel Data – Green 0
PORT1_D9	H4	I_3	PORT1_CLK	Pixel Data – Green 1
PORT1_D10	G3	I_3	PORT1_CLK	Pixel Data – Green 2
PORT1_D11	J4	I_3	PORT1_CLK	Pixel Data – Green 3
PORT1_D12	H3	I_3	PORT1_CLK	Pixel Data – Green 4
PORT1_D13	J3	I_3	PORT1_CLK	Pixel Data – Green 5
PORT1_D14	K3	I_3	PORT1_CLK	Pixel Data – Green 6
PORT1_D15	L1	I_3	PORT1_CLK	Pixel Data – Green 7
PORT1_D16	L3	I_3	PORT1_CLK	Pixel Data - Red 0
PORT1_D17	L4	I_3	PORT1_CLK	Pixel Data - Red 1
PORT1_D18	M4	I_3	PORT1_CLK	Pixel Data - Red 2
PORT1_D19	K1	I_3	PORT1_CLK	Pixel Data - Red 3
PORT1_D20	M1	I_3	PORT1_CLK	Pixel Data - Red 4
PORT1_D21	K2	I_3	PORT1_CLK	Pixel Data - Red 5
PORT1_D22	M2	I_3	PORT1_CLK	Pixel Data - Red 6
PORT1_D23	M3	I_3	PORT1_CLK	Pixel Data - Red 7
PORT1_HPD	E15	B_2		HDMI HOTPLUG DETECT.
PORT1_SYNCDET	J22			HDMI Input Sync Detect.

(1) See IO Characteristics for more detail.
(2) 24-bit data is mapped according to RGB888 pixel format. See Figure 2.

TERMINAL FUNCTIONS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL NAME	TERMINAL NO.	I/O TYPE(1)	CLOCK SYSTEM	DESCRIPTION
Port 2 Video Data & Control(3)				
PORT2_CLK	Y2	I_1		Pixel clock
PORT2_VSYNC	AF2	I_1	PORT2_CLK	Vertical Sync; weak pull-up applied
PORT2_HSYNC	AB6	I_1	PORT2_CLK	Horizontal Sync; weak pull-up applied
PORT2_IVALID	W1	I_1	PORT2_CLK	Data Valid
PORT2_D0	Y1	I_1	PORT2_CLK	Pixel Data - Blue 0
PORT2_D1	AE1	I_1	PORT2_CLK	Pixel Data - Blue 1
PORT2_D2	U2	I_1	PORT2_CLK	Pixel Data - Blue 2
PORT2_D3	AD12	I_1	PORT2_CLK	Pixel Data - Blue 3
PORT2_D4	AB1	I_1	PORT2_CLK	Pixel Data - Blue 4
PORT2_D5	V3	I_1	PORT2_CLK	Pixel Data - Blue 5
PORT2_D6	U5	I_1	PORT2_CLK	Pixel Data - Blue 6
PORT2_D7	T3	I_1	PORT2_CLK	Pixel Data - Blue 7
PORT2_D8	AD1	I_1	PORT2_CLK	Pixel Data – Green 0
PORT2_D9	AA3	I_1	PORT2_CLK	Pixel Data – Green 1
PORT2_D10	R6	I_1	PORT2_CLK	Pixel Data – Green 2
PORT2_D11	W3	I_1	PORT2_CLK	Pixel Data – Green 3
PORT2_D12	AB5	I_1	PORT2_CLK	Pixel Data – Green 4
PORT2_D13	AD3	I_1	PORT2_CLK	Pixel Data – Green 5
PORT2_D14	AD5	I_1	PORT2_CLK	Pixel Data – Green 6
PORT2_D15	AD4	I_1	PORT2_CLK	Pixel Data – Green 7
PORT2_D16	AE5	I_1	PORT2_CLK	Pixel Data - Red 0
PORT2_D17	AC11	I_1	PORT2_CLK	Pixel Data - Red 1
PORT2_D18	AB8	I_1	PORT2_CLK	Pixel Data - Red 2
PORT2_D19	AC7	I_1	PORT2_CLK	Pixel Data - Red 3
PORT2_D20	AG4	I_1	PORT2_CLK	Pixel Data - Red 4
PORT2_D21	AE4	I_1	PORT2_CLK	Pixel Data - Red 5
PORT2_D22	AF5	I_1	PORT2_CLK	Pixel Data - Red 6
PORT2_D23	AF3	I_1	PORT2_CLK	Pixel Data - Red 7
Sync In/Sync Out				
PORT1_Trig_in	F2	I_3	PORT1_CLK	Alternate sync for port 1. Treated as Vsync; weak pull-up applied
PORT1_Sync_out	H6	O_3	Async	RESERVED FOR FUTURE USE
PORT2_Trig_in	AB7	I_1	PORT2_CLK	Alternate sync for port 2. Treated as vsync; weak pull-up applied
PORT2_Sync_out	Y3	O_1	Async	RESERVED FOR FUTURE USE

(3) 24-bit data is mapped according to RGB888 pixel format. See Figure 2.

TERMINAL FUNCTIONS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O TYPE(1)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
Control Interfaces (I_2C, USB, SPI)				
USB_CLK	A15	I_3		USB clock input (48 MHz), feeds a PLL
USB_CTRL0	B17	I_3	USB_CLK	USB I/F FIFO Programmable Level
USB_CTRL1	A26	I_3	USB_CLK	USB I/F FIFO Full Flag
USB_CTRL2	D22	I_3	USB_CLK	USB I/F FIFO Empty Flag
USB_CTRL3	C19	I_3	USB_CLK	RESERVED FOR FUTURE USE
USB_CTRL4	D16	I_3	USB_CLK	RESERVED FOR FUTURE USE
USB_CTRL5	G17	I_3	USB_CLK	RESERVED FOR FUTURE USE
USB_FD0	G16	B_3	USB_CLK	USB Interface Data BUS
USB_FD1	C26			
USB_FD2	F17			
USB_FD3	C22			
USB_FD4	E18			
USB_FD5	B18			
USB_FD6	F18			
USB_FD7	E19			
USB_FD8	B23			
USB_FD9	D25			
USB_FD10	C21			
USB_FD11	D24			
USB_FD12	B19			
USB_FD13	E25			
USB_FD14	G18			
USB_FD15	C15			
USB_PA02	D23	O_3	USB_CLK	USB I/F FIFO Output Enable for Reads
USB_PA04	G15	O_3	USB_CLK	USB I/F FIFO Address(0)
USB_PA05	A22	O_3	USB_CLK	USB I/F FIFO Address(1)
USB_PA06	A25	O_3	USB_CLK	USB I/F FIFO Packet End Trigger
USB_RDY0	C16	O_3	USB_CLK	USB I/F FIFO Read Enable
USB_RDY1	C17	O_3	USB_CLK	USB I/F FIFO Write Enable
USB_RDY2	B26	O_3	USB_CLK	RESERVED FOR FUTURE USE
I2C_SCL	C25	B_2		Master I2C Clock - 400KHz. Requires external pull-up.
I2C_SDA	D18	B_2	I2C_SCL	Master I2C Data - 400KHz. Requires external pull-up.
EDID_I2C_SCL	F8	B_2		HDMI EDID I2C Clock. 400KHz. Requires external pull-up.
EDID_I2C_SDA	D6	B_2	EDID_I2C_SCL	HDMI EDID I2C Data. 400KHz. Requires external pull-up.
SLAVE_SPI_CLK	B14	I_3		SLAVE SPI CLOCK
$\overline{\text{SLAVE\_SPI\_CS}}$	C14	I_3	SLAVE_SPI_CLK	SLAVE SPI Chip Select; weak pull-up applied
SLAVE_SPI_MISO	D14	O_3	SLAVE_SPI_CLK	SLAVE SPI Data OUT
SLAVE_SPI_MOSI	E14	I_3	SLAVE_SPI_CLK	SLAVE SPI Data IN; weak pull-up applied
$\overline{\text{SLAVE\_SPI\_SOP}}$	F21	I_3	SLAVE_SPI_CLK	RESERVED FOR FUTURE USE
$\overline{\text{SLAVE\_SPI\_ACK}}$	D20	O_3	SLAVE_SPI_CLK	SLAVE SPI data busy

TERMINAL FUNCTIONS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O TYPE(1)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
DMD Interface				
DMD_DAT_AP1	AB27	O4	DMD_DCLK_AP, DMD_DCLK_AN	DMD Data Pins. LVDS pins for Data Bus A
DMD_DAT_AN1	AB28	O4		
DMD_DAT_AP3	Y25	O4		
DMD_DAT_AN3	Y26	O4		
DMD_DAT_AP5	W25	O4		
DMD_DAT_AN5	W26	O4		
DMD_DAT_AP7	W28	O4		
DMD_DAT_AN7	W27	O4		
DMD_DAT_AP9	V27	O4		
DMD_DAT_AN9	V28	O4		
DMD_DAT_AP11	V25	O4		
DMD_DAT_AN11	V26	O4		
DMD_DAT_AP13	V23	O4		
DMD_DAT_AN13	V24	O4		
DMD_DAT_AP15	T26	O4		
DMD_DAT_AN15	U27	O4		
DMD_DCLK_AP	T25	O4		DMD Data Clock. LVDS clk for Data Bus A
DMD_DCLK_AN	U28	04		DMD Data Clock. LVDS clk for Data Bus A
DMD_SCTRL_AP	R25	O4	DMD_DCLK_AP, DMD_DCLK_AN	DMD Data Serial Control signal Bus A (LVDS)
DMD_SCTRL_AN	R26	O4		
DMD_DAT_BP1	AC24	O4	DMD_DCLK_BP, DMD_DCLK_BN	DMD Data Pins. LVDS pins for Data Bus B
DMD_DAT_BN1	AC25	O4		
DMD_DAT_BP3	AC26	O4		
DMD_DAT_BN3	AD26	O4		
DMD_DAT_BP5	AE27	O4		
DMD_DAT_BN5	AE28	O4		
DMD_DAT_BP7	AD27	O4		
DMD_DAT_BN7	AD28	O4		
DMD_DAT_BP9	Y23	O4		
DMD_DAT_BN9	Y24	O4		
DMD_DAT_BP11	AC27	O4		
DMD_DAT_BN11	AC28	O4		
DMD_DAT_BP13	AB25	O4		
DMD_DAT_BN13	AB26	O4		
DMD_DAT_BP15	AA25	O4		
DMD_DAT_BN15	AA26	O4		
DMD_DCLK_BP	U25	O4		DMD Data Clock. LVDS clk for Data Bus B
DMD_DCLK_BN	U26	04		
DMD_SCTRL_BP	T21	O4	DMD_DCLK_AP, DMD_DCLK_AN	DMD Data Serial Control signal Bus B (LVDS)
DMD_SCTRL_BN	T22	O4		
DMD_PWRDN	P26	O3	ASYNC	DMD power down (active low)
RST_IRQ	M25	I3	ASYNC	DAD interrupt active low
RST_OE	M28	O3	ASYNC	DAD output enable
RST_RST	H24	O3	ASYNC	DAD reset

TERMINAL FUNCTIONS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O TYPE[(1)]	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
RST_STROBE	G28	O3		DAD strobe
RST_SEL0	G27	O3	RST_STROBE	DAD voltage select
RST_SEL1	G26			
RST_MODE0	L24	O3	RST_STROBE	DAD mode select
RST_MODE1	L23			
RST_A0	K25	O3	RST_STROBE	DAD address
RST_A1	J26			
RST_A2	J25			
RST_A3	K26			
SCP_DMD_RST_DO	G25	O3	SCP_DMD_RST_CLK	SCP data out (write data)
SCP_DMD_RST_DI	H26	I3	SCP_DMD_RST_CLK	SCP data in (read data)
SCP_DMD_EN	L25	O3	SCP_DMD_RST_CLK	DMD SCP chip select
SCP_RST_EN	H23	O3	SCP_DMD_RST_CLK	DAD SCP chip select
SCP_DMD_RST_CLK	H25	O3		DMD/DAD SCP clock, 125 kHz
Static RAM Interface				
FLASH_CE	D12	O3	ASYNC	Flash chip enable

TERMINAL FUNCTIONS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O TYPE (1)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
FLASH_SRAM_A0	D13	O3		
FLASH_SRAM_A1	A11			
FLASH_SRAM_A2	C11			
FLASH_SRAM_A3	D11			
FLASH_SRAM_A4	A12			
FLASH_SRAM_A5	B12			
FLASH_SRAM_A6	D10			
FLASH_SRAM_A7	A10			
FLASH_SRAM_A8	B10			
FLASH_SRAM_A9	B8			
FLASH_SRAM_A10	C8			
FLASH_SRAM_A11	A7			
FLASH_SRAM_A12	B7			
FLASH_SRAM_A13	A4		FLASH_SRAM_WE	Flash/SRAM address
FLASH_SRAM_A14	D7			
FLASH_SRAM_A15	C6			
FLASH_SRAM_A16	D8			
FLASH_SRAM_A17	B6			
FLASH_SRAM_A18	C7			
FLASH_SRAM_A19	A8			
FLASH_SRAM_A20	C4			
FLASH_SRAM_A21	B3			
FLASH_SRAM_A22	A3			
FLASH_SRAM_A23	C5			
FLASH_SRAM_A24	D5			
FLASH_SRAM_A25	B4			
FLASH_SRAM_A26	D4			
FLASH_SRAM_D0	E11	B3		
FLASH_SRAM_D1	F10			
FLASH_SRAM_D2	E10			
FLASH_SRAM_D3	G9			
FLASH_SRAM_D4	E8			
FLASH_SRAM_D5	E7			
FLASH_SRAM_D6	E5			
FLASH_SRAM_D7	E4		FLASH_SRAM_WE	Flash/SRAM data
FLASH_SRAM_D8	F11			
FLASH_SRAM_D9	E12			
FLASH_SRAM_D10	F12			
FLASH_SRAM_D11	G12			
FLASH_SRAM_D12	G13			
FLASH_SRAM_D13	H13			
FLASH_SRAM_D14	F14			
FLASH_SRAM_D15	G14			

TERMINAL FUNCTIONS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O TYPE(1)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
FLASH_SRAM_OE	C10	O3		Flash output enable
FLASH_SRAM_RDY	C13	I3		Flash wait
FLASH_SRAM_RST	C12	O3		Flash reset
FLASH_SRAM_WE	A6	O3		Flash write enable
SRAM_CE	B11	O3		SRAM chip enable
SRAM_LB	D9	O3		SRAM lower byte enable
SRAM_UB	C9	O3		SRAM upper byte enable
SDRAM Interface				
MEM_CLK_P0	R2	O5		DDR2 memory, differential memory clock
MEM_CLK_N0	R1	O5		DDR2 memory, differential memory clock
MEM_CLK_P1	U3	O5		DDR2 memory, differential memory clock
MEM_CLK_N1	U4	O5		DDR2 memory, differential memory clock
MEM_CLK_P2	AC5	O5		DDR2 memory, differential memory clock
MEM_CLK_N2	AC4	O5		DDR2 memory, differential memory clock
MEM_CLK_P3	AE14	O5		DDR2 memory, differential memory clock
MEM_CLK_N3	AF14	O5		DDR2 memory, differential memory clock
MEM_CKE0	AF12	O5		
MEM_BA0	Y19	O5	MEM_CLK	
MEM_BA1	AD21	O5	MEM_CLK	
MEM_BA2	AE7	O5	MEM_CLK	
MEM_A0	AD24	O5	MEM_CLK	DDR2 memory, Multiplexed Row and Column Address. The memory in the kit is 512 Mbit in a x16 mode, 8 Meg x 16 bits x 4 banks. Only A(12:0) and BA(1:0) are currently used. A(15:13) and BA(2) are reserved for future use (RFU).
MEM_A1	AF21			
MEM_A2	AG23			
MEM_A3	AE8			
MEM_A4	AG12			
MEM_A5	AF23			
MEM_A6	AC17			
MEM_A7	AA16			
MEM_A8	AE23			
MEM_A9	AE22			
MEM_A10	AE16			
MEM_A11	AD25			
MEM_A12	AF19			
MEM_A13	AH10			
MEM_A14	AA8			
MEM_A15	AD11			
MEM_CAS	AG19	O5	MEM_CLK	Column address strobe. Active low.
MEM_RAS	AE20	O5	MEM_CLK	Row address strobe. Active low.
MEM_CS0	AF13	O5	MEM_CLK	Chip select. Active low.
MEM_WE	AG25	O5	MEM_CLK	Write enable. Active low.
MEM_ODT	AH12	O5	MEM_CLK	
MEM_DM0	W2	O5	MEM_CLK	
MEM_DM1	AE2	O5	MEM_CLK	
MEM_DM2	AH6	O5	MEM_CLK	
MEM_DM3	AF7	O5	MEM_CLK	

TERMINAL FUNCTIONS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O TYPE[1]	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
MEM_DM4	AE13	O5	MEM_CLK	
MEM_DM5	AH18	O5	MEM_CLK	
MEM_DM6	AF24	O5	MEM_CLK	
MEM_DM7	AG26	O5	MEM_CLK	
MEM_DS0	AB2	B1	MEM_CLK_P0	
MEM_DS1	AE3	B1	MEM_CLK_N0	
MEM_DS2	AD7	B1	MEM_CLK_P1	
MEM_DS3	AE10	B1	MEM_CLK_N1	
MEM_DS4	AF11	B1	MEM_CLK_P2	
MEM_DS5	AF17	B1	MEM_CLK_N2	
MEM_DS6	AE18	B1	MEM_CLK_P3	
MEM_DS7	AF26	B1	MEM_CLK_N3	
MEM_D0	R3	B1	MEM_DS0, MEM_DS1	
MEM_D1	R4	B1		
MEM_D2	T4	B1		
MEM_D3	R5	B1		
MEM_D4	U1	B1		
MEM_D5	V4	B1		
MEM_D6	V2	B1		
MEM_D7	V1	B1		
MEM_D8	U6	B1		
MEM_D9	Y4	B1		
MEM_D10	AC2	B1		
MEM_D11	AC1	B1		
MEM_D12	AC3	B1		
MEM_D13	AD2	B1		
MEM_D14	AB3	B1		
MEM_D15	AA4	B1		
MEM_D16	AE6	B1	MEM_DS2, MEM_DS3	
MEM_D17	AF4	B1		
MEM_D18	AG3	B1		
MEM_D19	AH3	B1		
MEM_D20	AF6	B1		
MEM_D21	AH4	B1		
MEM_D22	AD8	B1		
MEM_D23	AG6	B1		
MEM_D24	AB9	B1		
MEM_D25	AD10	B1		
MEM_D26	AG7	B1		
MEM_D27	AH7	B1		
MEM_D28	AC8	B1		
MEM_D29	AA10	B1		
MEM_D30	AG8	B1		
MEM_D31	AH8	B1		

TERMINAL FUNCTIONS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O TYPE(1)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
MEM_D32	AF8	B1	MEM_DS4, MEM_DS5	
MEM_D33	AE9	B1		
MEM_D34	AF10	B1		
MEM_D35	AG10	B1		
MEM_D36	AE12	B1		
MEM_D37	AE11	B1		
MEM_D38	AG11	B1		
MEM_D39	AH11	B1		
MEM_D40	AC15	B1		
MEM_D41	AF15	B1		
MEM_D42	AG17	B1		
MEM_D43	AH16	B1		
MEM_D44	AF16	B1		
MEM_D45	AB16	B1		
MEM_D46	AE17	B1		
MEM_D47	AG18	B1		
MEM_D48	AH19	B1	MEM_DS6, MEM_DS7	
MEM_D49	AD17	B1		
MEM_D50	AG21	B1		
MEM_D51	AH21	B1		
MEM_D52	AG22	B1		
MEM_D53	AH22	B1		
MEM_D54	AH23	B1		
MEM_D55	AE19	B1		
MEM_D56	AF25	B1		
MEM_D57	AF20	B1		
MEM_D58	AD18	B1		
MEM_D59	AE21	B1		
MEM_D60	AE25	B1		
MEM_D61	AH25	B1		
MEM_D62	AR22	B1		
MEM_D63	AE24	B1		
LED Driver Interface				
PWM0	C27	O_3	Async	PWM signal used to control the LED Current
PWM1	D28	O_3	Async	PWM signal used to control the LED Current
PWM2	D27	O_3	Async	PWM signal used to control the LED Current
PWM3	D26	O_3	Async	PWM signal used to control the LED Current
LED_IR_EN	E28	O_3	Async	IR LED Enable Strobe. Controlled by programmable DMD Sequence Timing (Active High)
LED_RED_EN	F28	O_3	Async	RED LED Enable Strobe. Controlled by programmable DMD Sequence Timing (Active High)
LED_GRN_EN	E27	O_3	Async	Green LED Enable Strobe. Controlled by programmable DMD Sequence Timing (Active High)
LED_BLU_EN	F27	O_3	Async	Blue LED Enable Strobe. Controlled by programmable DMD Sequence Timing (Active High)

TERMINAL FUNCTIONS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O TYPE(1)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
LED_SUBFRAME	E26	O_3	Async	Subframe signal used by LED Driver. Controlled by programmable DMD Sequence Timing (Active High)
SYNC_0	F26	O_3	Async	Extra Strobe. Controlled by programmable DMD Sequence Timing (Active High)
SYNC_1	F25	O_3	Async	Extra Strobe. Controlled by programmable DMD Sequence Timing (Active High)
SYNC_2	F24	O_3	Async	Extra Strobe. Controlled by programmable DMD Sequence Timing (Active High)
$\overline{\text{LED\_EN}}$	L28	O_3	Async	LED Driver Enable. Active low output control to external LED Drive Logic.
LED_SYNC	M21	O_3	Async	Reserved for future use; weak pull-up applied
LED_SYNCEN	C24	O_3	Async	Inverted $\overline{\text{LED\_LIT}}$ signal
$\overline{\text{LED\_LIT}}$	J28	I_3	Async	LED Driver Status
LED_SENS	K27	I_3	Async	Reserved for future use.
LED_SPI_CLK	N26	O_3	Async	LED SPI MASTER CLOCK
$\overline{\text{LED\_SPI\_CS}}$	M26	O_3	LED_SPI_CLK	LED SPI MASTER Chip Select
LED_SPI_DIR	P25	O_3	LED_SPI_CLK	LED SPI MASTER Driver Direction
LED_SPI_MISO	L27	I_3	LED_SPI_CLK	LED SPI MASTER Data IN
LED_SPI_MOSI	L26	O_3	LED_SPI_CLK	LED SPI MASTER Data OUT; weak pull-up applied
System Interfaces				
$\overline{\text{CFG\_CSO}}$	E2	O_3	CFG_DCLK	Chip Select Output for an external serial configuration device. Active low.
CFG_CLK	P3	O_3	CFG_DCLK	Configuration Serial EPROM data clock.
CFG_ASDI	N7	I_3	CFG_DCLK	Data input from an external serial configuration device. Provides configuration data for the device.
CFG_ASDO	F4	O_3	CFG_DCLK	Serial Data Output. This pin sends address and control information to the external PROM during configuration.
$\overline{\text{CFG\_STATUS}}$	M6	O_3	CFG_DCLK	Configuration status pin.
CFG_DONE	P24	O_3	CFG_DCLK	Configuration Done status pin. Signal goes high at the end of configuration.
CFG_MSEL0 CFG_MSEL1 CFG_MSEL2 CFG_MSEL3	N22 P23 M22 P22	I_3	Async	Configuration Mode Selection signals.
$\overline{\text{CFG\_CE}}$	R8	I_3	Async	Chip Enable. Active low.
$\overline{\text{CFG\_EN}}$	P4	I_3	Async	Configuration control. Configuration will start when a low to high transition is detected at this pin.
$\overline{\text{CFG\_CEO}}$	P28	O_1	Async	
REF_CLK	J27	I_3		50 MHz reference clock, 3.3V
$\overline{\text{RESET}}$	A14	I_3	Async	Device reset (active low)
PWR_GOOD	A23	I_3	Async	System power good indicator
RSVD_H10	N4	B_2		GPIO
RSVD_H11	L2	B_2		GPIO
RSVD_H12	K4	B_2		GPIO
RSVD_H6	G1	B_2		GPIO
RSVD_H5	G5	B_2		GPIO
RSVD_H4	G6	B_2		GPIO
RSVD_H2	E1	B_2		GPIO

TERMINAL FUNCTIONS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O TYPE (1)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
RSVD_H1	C2	B_2		GPIO
Reserved				
RSVD_T0	E22			These I/O can be left open/ unconnected for normal operation.
RSVD_T1	D21			
RSVD_T2	A21			
RSVD_T3	C18			
RSVD_T4	B22			
RSVD_T5	B21			
RSVD_T6	D17			
RSVD_T7	E21			
RSVD_TC	M24			
RSVD_D0	A17	I_3		RESERVED FOR FUTURE USE, do not connect
RSVD_D1	D15	O_3		RESERVED FOR FUTURE USE, do not connect
RSVD_D2	E17	I_3		RESERVED FOR FUTURE USE, do not connect
RSVD_D3	F15	O_3		RESERVED FOR FUTURE USE, do not connect
RSVD_H3	E3	I_3		RESERVED FOR FUTURE USE, can be left open, recommend grounding.
RSVD_H7	H7	I_3		RESERVED FOR FUTURE USE, can be left open, recommend grounding.
RSVD_H8	L5	I_3		RESERVED FOR FUTURE USE, can be left open, recommend grounding.
RSVD_H9	M5	I_3		RESERVED FOR FUTURE USE, can be left open, recommend grounding.
RSVD_H13	J1	I_3		RESERVED FOR FUTURE USE, can be left open, recommend grounding.
RSVD_P0	P7	I_4		RESERVED FOR FUTURE USE, do not connect
RSVD_P1	P6	O_2		RESERVED FOR FUTURE USE, do not connect
RSVD_P2	P8	I_4		RESERVED FOR FUTURE USE, do not connect
RSVD_P3	P5	I_4		RESERVED FOR FUTURE USE, do not connect
RSVD_G0	C23	O_3		RESERVED FOR FUTURE USE, do not connect
RSVD_G1	F19	O_3		RESERVED FOR FUTURE USE, do not connect
RSVD_G2	M27	O_3		RESERVED FOR FUTURE USE, do not connect
RSVD_G3	N21	O_3		RESERVED FOR FUTURE USE, do not connect
RSVD_G4	P27	O_3		RESERVED FOR FUTURE USE, do not connect
RSVD_G5	A18	O_3		RESERVED FOR FUTURE USE, do not connect
RSVD_G6	A19	O_3		RESERVED FOR FUTURE USE, do not connect
RSVD_S1	AG14			Unused input only, can be left open, recommend grounding.
RSVD_S2	AG15			Unused input only, can be left open, recommend grounding.
RSVD_S3	AH14			Unused input only, can be left open, recommend grounding.
RSVD_X11	AH15			Unused input only, can be left open, recommend grounding.
RSVD_S20	Y27			Unused input only, can be left open, recommend grounding.
RSVD_S21	Y28			Unused input only, can be left open, recommend grounding.
RSVD_X9	AA22			RESERVED FOR FUTURE USE, do not connect
RSVD_S0	AA24			RESERVED FOR FUTURE USE, do not connect
RSVD_X10	AB23			RESERVED FOR FUTURE USE, do not connect
RSVD_X6	AB24			RESERVED FOR FUTURE USE, do not connect

TERMINAL FUNCTIONS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL NAME	TERMINAL NO.	I/O TYPE (1)	CLOCK SYSTEM	DESCRIPTION
RSVD_X3	AC21			RESERVED FOR FUTURE USE, do not connect
RSVD_X15	AA17			RESERVED FOR FUTURE USE, do not connect
RSVD_X2	AE15			RESERVED FOR FUTURE USE, do not connect
RSVD_X0	AF18			RESERVED FOR FUTURE USE, do not connect
RSVD_X8	AF27			RESERVED FOR FUTURE USE, do not connect
RSVD_X4	AF9			RESERVED FOR FUTURE USE, do not connect
RSVD_S4	AH26			RESERVED FOR FUTURE USE, do not connect
RSVD_S5	B25			RESERVED FOR FUTURE USE, do not connect
RSVD_S6	C20			RESERVED FOR FUTURE USE, do not connect
RSVD_S8	D19			RESERVED FOR FUTURE USE, do not connect
RSVD_X5	E24			RESERVED FOR FUTURE USE, do not connect
RSVD_S10	F22			RESERVED FOR FUTURE USE, do not connect
RSVD_S11	K28			RESERVED FOR FUTURE USE, do not connect
RSVD_S14	N25			RESERVED FOR FUTURE USE, do not connect
RSVD_X7	R24			RESERVED FOR FUTURE USE, do not connect
RSVD_S16	R27			RESERVED FOR FUTURE USE, do not connect
RSVD_S17	R28			RESERVED FOR FUTURE USE, do not connect
RSVD_S18	U23			RESERVED FOR FUTURE USE, do not connect
RSVD_S19	U24			RESERVED FOR FUTURE USE, do not connect
Power and Ground (4)				
P1P2V		PWR	N/A	1.2 V core power
P2P5V_DPLL		PWR	N/A	2.5 V filtered power for internal PLL
P1P8V		PWR	N/A	1.8 V I/O power
P2P5V		PWR	N/A	2.5 V I/O power
P3P3V		PWR	N/A	3.3 V I/O power
GND		PWR	N/A	Common digital ground
GNDA		PWR	N/A	Common PLL ground

(4) Unused inputs should be pulled down to ground through an external resistor.

I/O CHARACTERISTICS (1)

all inputs/outputs are LVCMOS

I/O TYPE		CONDITIONS	V_{IL}(V)		V_{IH}(V)		V_{OH}(V)	V_{OL}(V)	Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
I_1	Input LVCMOS	V_{CCIO} = 1.8 V	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	2.25			V
I_2	Input LVCMOS	V_{CCIO} = 2.5 V	-0.3	0.7	1.7	V_{CCIO}+0.3			V
I_3	Input LVCMOS	V_{CCIO} = 3.3 V	-0.3	0.8	1.7	3.6			V
I_4	Input LVTTL	V_{CCIO} = 3.3 V	-0.3	0.8	1.7	3.6			V
O_1	Output LVCMOS	V_{CCIO} = 1.8 V					V_{CCIO}-0.45	0.45	V
O_2	Output LVTTL	V_{CCIO} = 3.3 V					2.4	0.45	V
O_3	Output LVCMOS	V_{CCIO} = 3.3 V					V_{CCIO}-0.2	0.2	V
O_4	Output LVDS	V_{CCIO} = 3.3 V					V_{CCIO}-0.3	0.3	V
O_5	Output SSTL-18 Class I	V_{CCIO} = 1.8 V					1.484	0.398	V

(1) Cross reference to IO assignments

I/O CHARACTERISTICS (1) (continued)

all inputs/outputs are LVCMOS

I/O TYPE		CONDITIONS	V_{IL}(V)		V_{IH}(V)		V_{OH}(V)	V_{OL}(V)	Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
B_1	Bi-directional SSTL-18 Class I	V_{CCIO} = 1.8 V		0.844	1.094		1.484	0.398	V
B_2	Bi-directional LVCMOS	V_{CCIO} = 3.3 V	-0.3	0.8	1.7	3.6	V_{CCIO}-0.2	0.2	V

POWER AND GROUND PINS

NAME	DESCRIPTION	PIN NUMBER(S)
Input Power and Ground Pins		
VCC_1P2V	1.2-V power supply for core logic	K9, K11, K13, K15, K17, K19, L10, L12, L14, L16, L18, L20, M9, M11, M13, M15, M17, M19, N10, N12, N14, N16, N18, N20, P9, P11, P13, P15, P17, P19, R10, R12, R14, R16, R18, R20, T9, T11, T13, T15, T17, T19, U10, U12, U14, U16, U18, U20, V9, V11, V13, V15, V17, V19, W10, W12, W14, W16, W18, W20
VCC_2P5V	2.5-V power supply for I/Os on bank 5	AA28, AG28, T24, T28, W24
VCC_1P8V	1.8-V power supply for I/Os on bank 2, 3, 4	AA1, AG1, T1, T5, W5 AA11, AD6, AD9, AD13, AH2, AH5, AH9, AH13 AA18, AD16, AD20, AD23, AH16, AH20, AH24, AH27
VCC_3P3V	3.3-V power supply for I/Os on bank 1, 6, 7, 8	B1, H1, K5, N1, N5 B28, H28, K24, N24, N28 A16, A20, A24, A27, E16, E20, E23, H18 A2, A5, A9, A13, E6, E9, E13, H11
VCCA	2.5V power supply for the internal PLL analog supply.	Y8, J21, J8, Y21
VCCD_PLL	1.2V power supply for the internal PLL digital supply.	Y9, J20, J9, Y20
VREF_B2	DDR2 VREF 0.9V, The SDRAM spec has guidelines on how these references should be connected. It is not just any 0.9V source on the board.	T7, T8, AB4
VREF_B3	DDR2 VREF 0.9V, The SDRAM spec has guidelines on how these references should be connected. It is not just any 0.9V source on the board.	AB13, AB11, Y10
VREF_B4	DDR2 VREF 0.9V, The SDRAM spec has guidelines on how these references should be connected. It is not just any 0.9V source on the board.	AB20, AC18, AA15
DGND	Common ground	K10, K12, K14, K16, K18, K20, L9, L11, L13, L15, L17, L19, M10, M12, M14, M16, M18, M20, N9, N11, N13, N15, N17, N19, P10, P12, P14, P16, P18, P20, R9, R11, R13, R15, R17, R19, T10, T12, T14, T16, T18, T20, U9, U11, U13, U15, U17, U19, V10, V12, V14, V16, V18, V20, W9, W11, W13, W15, W17, W19, AA2, AA27, AC6, AC9, AC13, AC16, AC20, AC23, AF1, AF28, AG2, AG5, AG9, AG13, AG16, AG20, AG24, AG27, B2, B5, B9, B13, B16, B20, B24, B27, C1, C28, F6, F9, F13, F16, F20, F23, H2, H27, J11, J18, K6, K23, N2, N6, N23, N27, T2, T6, T23, T27, W6, W23, Y11, Y18
DGND2	Analog Ground Return for the PLL (This should not be connected to the common ground GND)	H9, H20, AA9, AA20

POWER AND GROUND PINS (continued)

NAME	DESCRIPTION	PIN NUMBER(S)
NC	No Connect Pins	C3, F7, G7, G8, G10, G11, G19, G20, G21, G22, G23, G24, H8, H10, H12, H14, H15, H16, H17, H19, H21, H22, J5, J6, J7, J10, J12, J13, J14, J15, J16, J17, J19, J23, J24, K7, K8, K21, K22, L6, L7, L8, L21, L22, M7, M8, M23, N8, P21, R7, R21, R22, R23, U21, U22, V5, V6, V7, V8, V21, V22, W4, W7, W8, W21, W22, Y5, Y6, Y7, Y12, Y13, Y14, Y15, Y16, Y17, Y22, AA5, AA6, AA7, AA12, AA13, AA14, AA19, AA21, AA23, AB10, AB12, AB14, AB15, AB18, AB19, AB21, AB22, AC10, AC12, AC14, AC19, AC22, AD14, AD19, AD22, AE26

Video Input Pixel Interface

Figure 2 illustrates how pixels should be mapped to the input data bus for both port 1 and port 2.

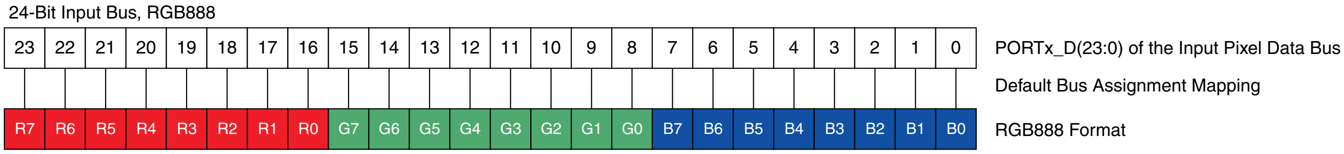


Figure 2. Pixel Mapping

IMAGE SYNC AND BLANKING REQUIREMENTS

PARAMETER		MIN	MAX	UNIT
t_{p_vsw}	Vertical Sync Width	1		clocks
t_{p_vbp}	Vertical Back Porch	14		lines
t_{p_vfp}	Vertical Front Porch	2		lines
t_{p_hsw}	Horizontal Sync Width	1		clocks
t_{p_hbp}	Horizontal Back Porch	64		clocks
t_{p_hfp}	Horizontal Front Porch	75		clocks

TIMING REQUIREMENTS

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{pclock}	Clock frequency, PORTx_CLK			80	MHz
t_{p_wh}	Pulse duration, high	45% to 55% reference points (signal)	5.6		ns
t_{p_wl}	Pulse duration, low	45% to 55% reference points (signal)	5.6		ns
t_{p_su}	Setup time, PORTx_D(23-0) valid before PORTx_CLK	See [1]	1.5		ns
t_{p_h}	Hold time, PORTx_D(23-0) valid after PORTx_CLK	See [1]	1.5		ns
t_{p_su}	Setup time, PORTx_VSYNC valid before PORTx_CLK	See [1]	1.5		ns
t_{p_h}	Hold time, PORTx_VSYNC valid after PORTx_CLK	See [1]	1.5		ns
t_{p_su}	Setup time, PORTx_HSYNC valid before PORTx_CLK	See [1]	1.5		ns
t_{p_h}	Hold time, PORTx_HSYNC valid after PORTx_CLK	See [1]	1.5		ns
t_{p_su}	Setup time, PORTx_IVALID valid before PORTx_CLK	See [1]	1.5		ns
t_{p_h}	Hold time, PORTx_IVALID valid after PORTx_CLK	See [1]	1.5		ns

(1) PCLK may be inverted from that shown in Figure 3. In that case the same specifications in the table are valid except now referenced to the falling edge of the clock. If the falling edge of PCLK is to be used, an USB or SPI command is needed to tell the DLPC200 to use the falling edge of PCLK.

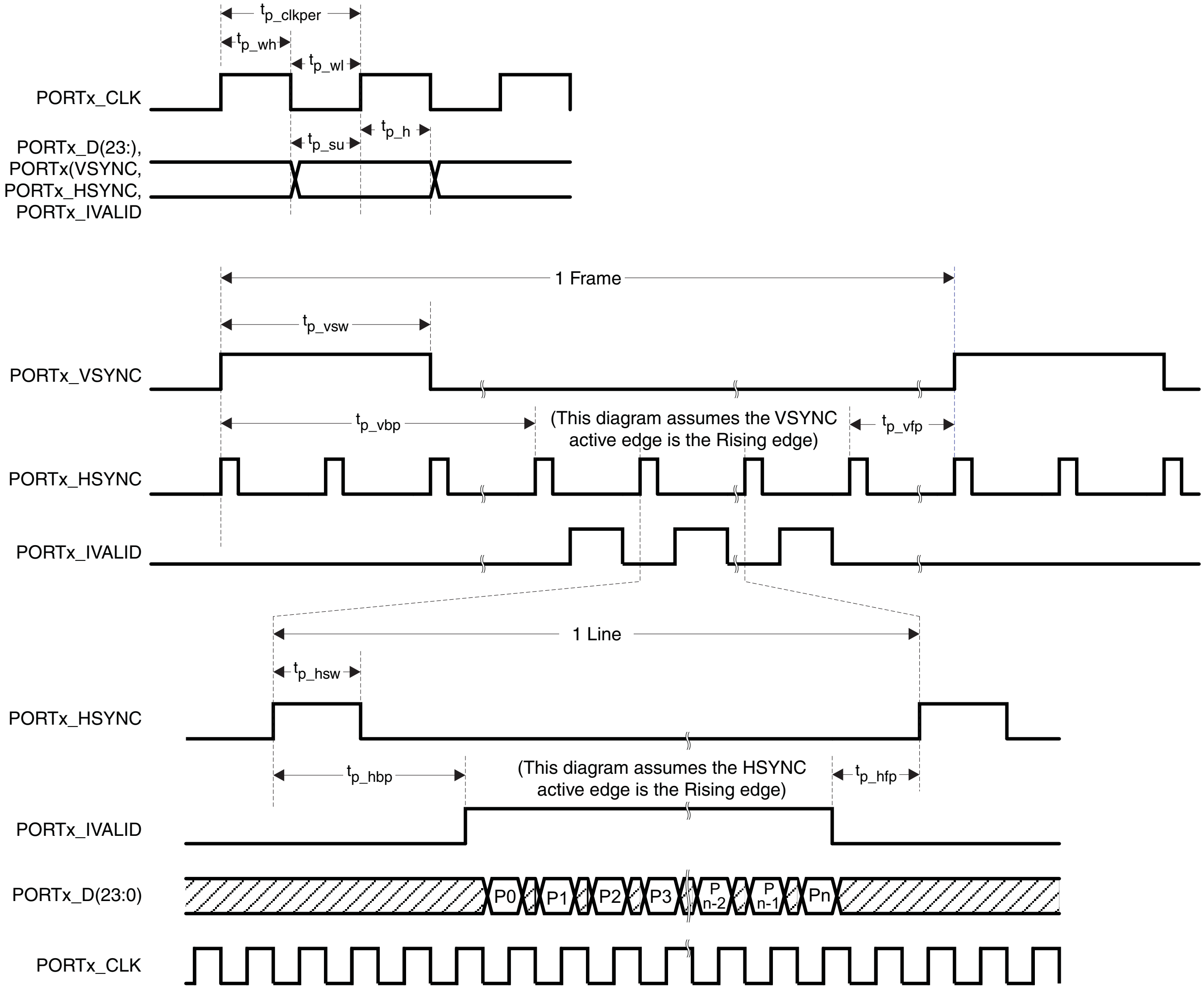


Figure 3. Input Port Interface

DLPC200 Master, I²C Interface, for Extended Display Identification Data (EDID) programming

The DLCP200 controller I²C interface is used only to program the HDMI EDID. Upon plugging in an HDMI source, the DMD resolution is compared to the HDMI output resolution programmed in the EDIDPROM. If the two do not match, then the HDMI EDID is adjusted to match the DMD resolution.

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high. After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.

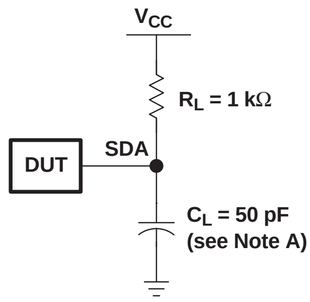
DLPC200 Master, I²C Interface, for Extended Display Identification Data (EDID) programming (continued)

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop). A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master.

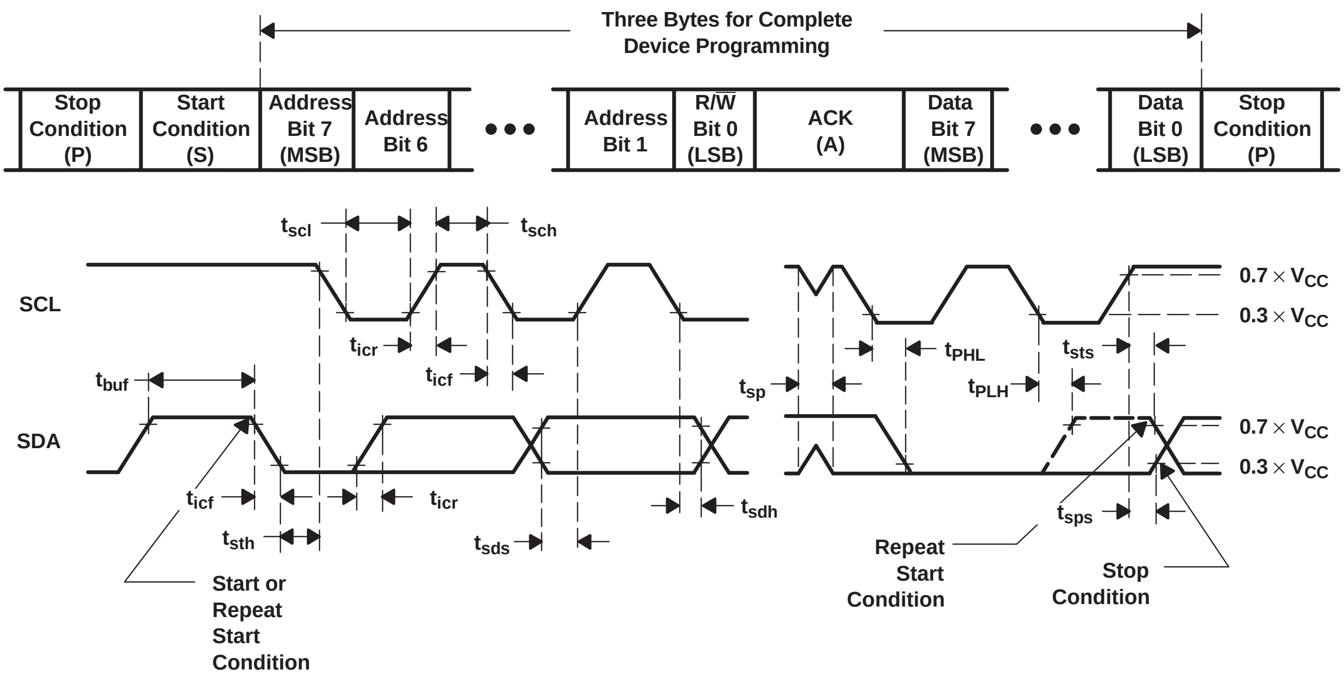
Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period. Setup and hold times must be met to ensure proper operation.

I²C INTERFACE TIMING REQUIREMENTS

PARAMETER			MIN	MAX	UNIT
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		1		ms
t_{scl}	I²C clock low time		1		ms
t_{sp}	I²C spike time			20	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		100		ns
t_{icr}	I²C input rise time		100		ns
t_{ocf}	I²C output fall time	50 pF	30	200	ns
t_{buf}	I²C bus free time between stop and start conditions		1.3		ms
t_{sts}	I²C start or repeat start condition setup		1		ms
t_{sth}	I²C start or repeat start condition hold		1		ms
t_{sph}	I²C stop condition setup		1		ms
t_{vd}	Valid-data time	SCL low to SDA output valid		1	ms
	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low		1	ms
t_{sch}	I²C bus capacitive load		0	100	pF



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

Figure 4. I^2C Interface Load Circuit and Voltage Waveforms

Recommended EDID PROM Devices

PART NUMBER	MANUFACTURER
24LC02B	Microchip Technology

USB Interface

The USB Interface consists of a single chip integrated USB 2.0 tranceiver, smart SIE, and enhance 8051 microprocessor running at 48 MHz (nominal) that support USB 2.0.

Bus Protocol

USB is a polled bus. The host controller (typically at PC) initiates all data transfers. Each transaction begins when the PC sends a packet. Communications will always be through the bulk transfer mode and 512 bytes of data are always written/read at a time. The packet consists of the following:

- Header (6 bytes)
- Data (505 bytes)
- Checksum (1 byte)

The USB device that is addressed selects itself by decoding the appropriate address fields. The direction of data transfer, either read or write, is specified in the packet header. The source of the transaction then sends a data packet or indicates it has no data to transfer. At the end of either a single packet transfer or a multi-packet transfer, the destination responds with a handshake packet indicating whether the transfer was successful.

Packet header consists of a

- CMD1 - indicates if packet is write/write response or read/read response
- CMD2 - groups major functions together
- CMD3 - provides more information about packet grouping defined in CMD2
- CMD4 - used to indicate location of data in a multi-packet transfer
- Len_MSB:Len_LSB - valid number of bytes of data transfered in packet data

Header						Data	Checksum
CMD1 1 byte	CMD2 1 byte	CMD3 1 byte	CMD4 1 byte	Len_LSB 1 byte	Len_MSB 1 byte	0-505 bytes	1 byte

Figure 5. USB Data Packet

As discussed above, the header describes whether the data transaction will be a read or write and designates the data endpoint. The data portion of the packet carries the payload and is followed by an handshaking mechanism, checksum, that reports if the data was received successfully, or if the endpoint is stalled or not available to accept data.

USB READ INTERFACE TIMING REQUIREMENTS

PARAMETER		MIN	Typ	MAX	UNIT
t_{CL}	1/CLKOUT Frequency		20.8		ns
t_{AV}	Delay from clock to valid address			10.7	ns
t_{STBL}	Clock to USB_RDY0 LOW			11	ns
t_{STBH}	Clock to USB_RDY0 HIGH			11	ns
t_{SCSL}	Clock to USB_PA02 LOW			13	ns
t_{DSU}	Data setup to clock	9.6			ns
t_{DH}	Data hold time	0			ns
t_{ACC1}	valid USB_PA04 to valid USB_FDC	43			ns

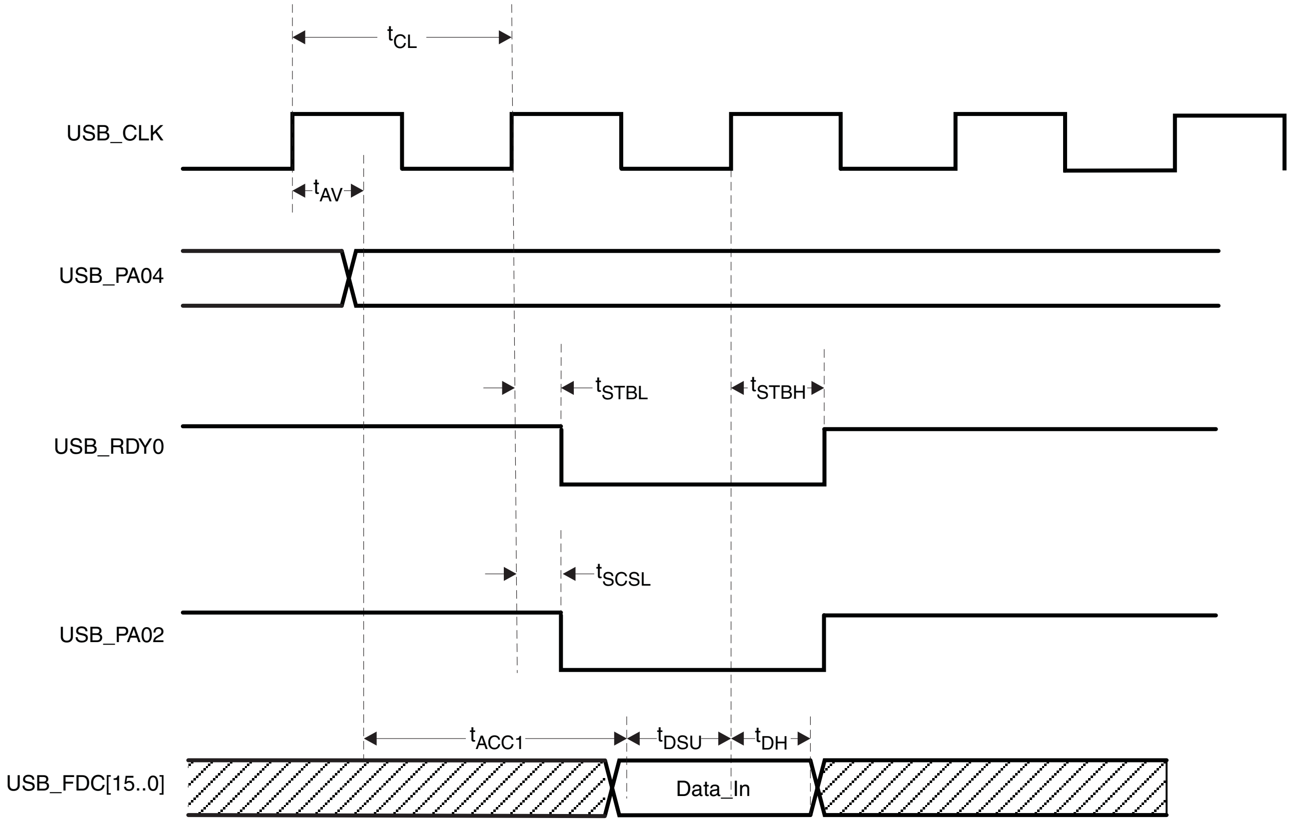


Figure 6. USB Read Timing

USB WRITE INTERFACE TIMING REQUIREMENTS

		MIN	MAX	UNIT
t_{AV}	Delay from clock to valid address	0	10.7	ns
t_{STBL}	Clock to USB_RDY1 pulse LOW	0	11.2	ns
t_{STBH}	Clock to USB_RDY1 pulse HIGH	0	11.2	ns
t_{SCSL}	Clock to USB_PA02 pulse LOW		13.0	ns
t_{ON1}	Clock to data turn-on	0	13.1	ns
t_{OFF1}	Clock to data hold time	0	13.1	ns

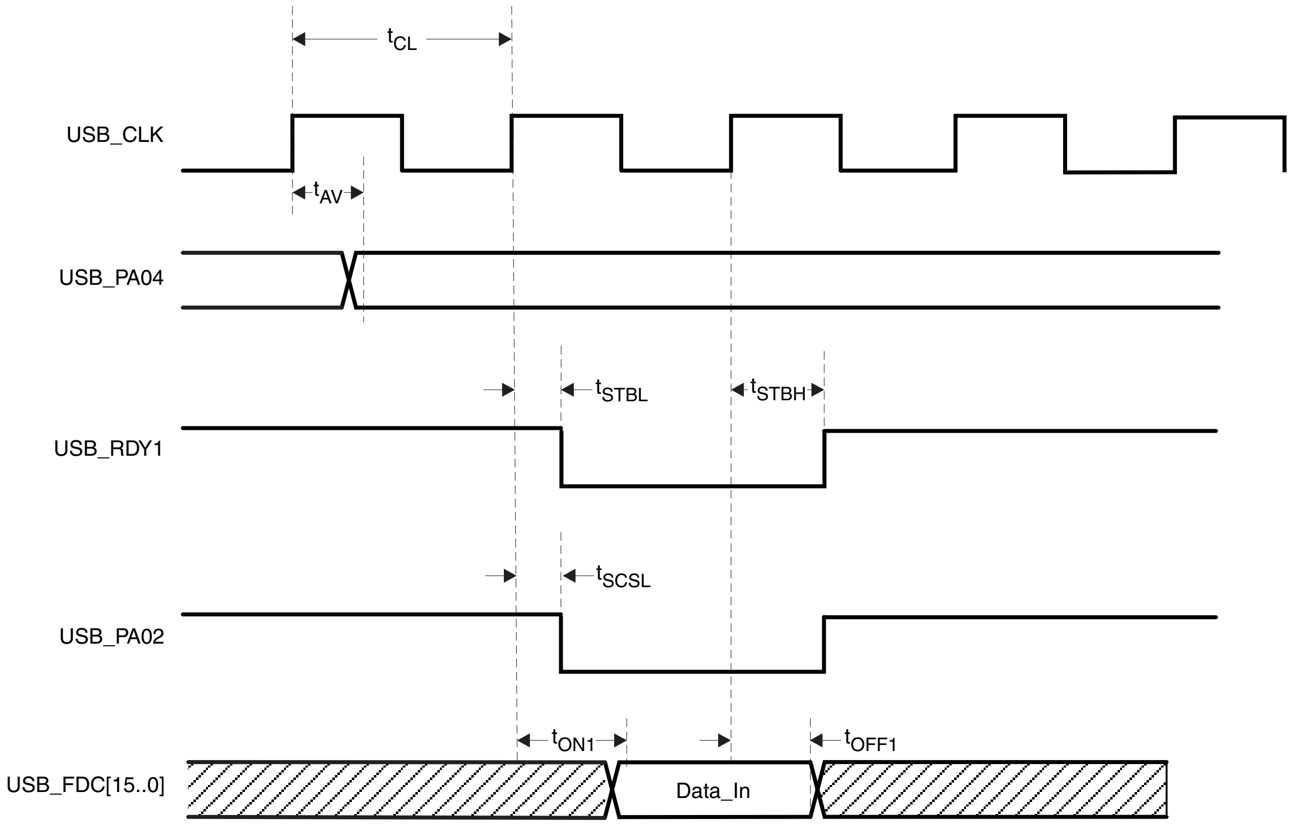


Figure 7. USB Write Timing

Recommended USB Devices

PART NUMBER	MANUFACTURER
CY7C68013A	Cypress

SPI Slave Interface

The DLCP200 controller SPI interface consists of a 5 MHz input.

The SPI bus specifies five logic signals.

- SCLK — Serial Clock (output from master)
- MOSI — Master Output, Slave Input (output from master)
- MISO — Master Input, Slave Output (output from slave)
- $\overline{SS}$ — Slave Select (active low; output from master)
- BUSY — hold off signal to indicate that the slave is processing commands and cannot accept new input

SPI Slave Interface (continued)

(output from slave)

The master pulls the slave select low. During each SPI clock cycle, a full duplex data transmission occurs:

- The master sends a bit on the MOSI line; the slave reads it from that same line
- The slave sends a bit on the MISO line; the master reads it from that same line

Transmissions involve two shift registers, one in the master and one in the slave; they are connected in a ring. Data is shifted out with the most significant bit first, while shifting a new least significant bit into the same register.

After that register has been shifted out, the master and slave have exchanged register values. If there is more data to exchange, the shift registers are loaded with new data and the process repeats. Transmissions may involve any number of clock cycles.

When there is no more data to be transmitted, the master stops toggling its clock. Transmissions consist of packet commands/responses similar to the protocol defined for the USB interface. The SPI slave supports variable length command and response packets and a master can initiate multiple such transmissions as needed.

SPI INTERFACE TIMING REQUIREMENTS

PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency, SPI_CLK		5	MHz
t_{p_clkper}	Clock period, SPI_CLK	29.994	30.006	ns
t_{p_wh}	Pulse width low, SPI_CLK	10		ns
t_{p_wl}	Pulse width high, SPI_CLK	10		ns
t_{p_su}	Setup Time – SPI_DIN valid before SPI_CLK rising edge	10		ns
t_{p_h}	Hold Time – SPI_DIN valid after SPI_CLK rising edge	5		ns

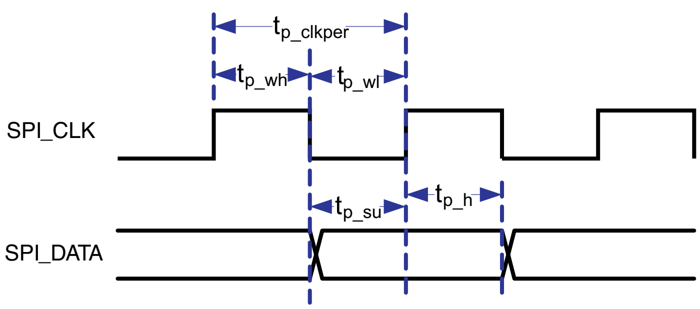


Figure 8. SPI Slave Timing

Parallel Flash Memory Interface

The Controller Parallel Flash Memory interface supports a high-speed NOR device with a 16 bit data bus and up to 1GB of memory.

To perform a synchronous burst read on array or non-array, an initial address is driven onto the address bus, and CE is asserted. $\overline{\text{WE}}$ and $\overline{\text{RST}}$ must already have been deasserted. $\overline{\text{ADV}}$ is asserted, and then deasserted to latch the address. Alternately, $\overline{\text{ADV}}$ can remain asserted throughout the burst access, in which case the address is latched on the next valid CLK edge while $\overline{\text{ADV}}$ is asserted. Once $\overline{\text{OE}}$ is asserted, the the first word is driven onto DQ[15:0] on the next valid CLK edge after initial access latency delay. Subsequent data is output on valid CLK edges following a minimum delay Tchqv.

The WAIT signal indicates data valid when the device is operating in synchronous mode (RCR.15=0). The WAIT signal is only “deasserted” when data is valid on the bus. When the device is operating in synchronous non-array read mode, such as read status, read ID, or read query, the WAIT signal is also “deasserted” when data is valid on the bus. WAIT behavior during synchronous non-array reads at the end of word line works correctly only on the first data access.

Parallel Flash Memory Interface (continued)

To perform a write operation, both $\overline{CE}$ and $\overline{WE}$ are asserted while $\overline{RST}$ and $\overline{OE}$ are deasserted. During a write operation, address and data are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. When the device is operating in write operations, WAIT is set to a deasserted state as determined by RCR.10.

PARALLEL FLASH INTERFACE TIMING REQUIREMENTS

PARAMETER		MIN	MAX	UNIT
t_{AVAV}	Read cycle time		110	ns
t_{AVQV}	Address to output valid		110	ns
t_{ELQV}	CE# low to output valid		110	ns
t_{GLQV}	OE# low to output valid		25	ns
t_{PHQV}	RST# high to output valid		150	ns
t_{GLTV}	OE# low to WAIT valid		17	ns
t_{PHWL}	RST# high recovery to WE# low	150		ns
t_{ELWL}	CE# setup to WE# low	0		ns
t_{WLWH}	WE# write pulse width low	50		ns
t_{DVWH}	Data setup to WE# high	50		ns
t_{AVWH}	Address setup to WE# high	50		ns
t_{WHEH}	CE# hold from WE# high	0		ns
t_{PWDHX}	Data hold from WE# high	0		ns
t_{WHAX}	Address hold from WE# high	0		ns

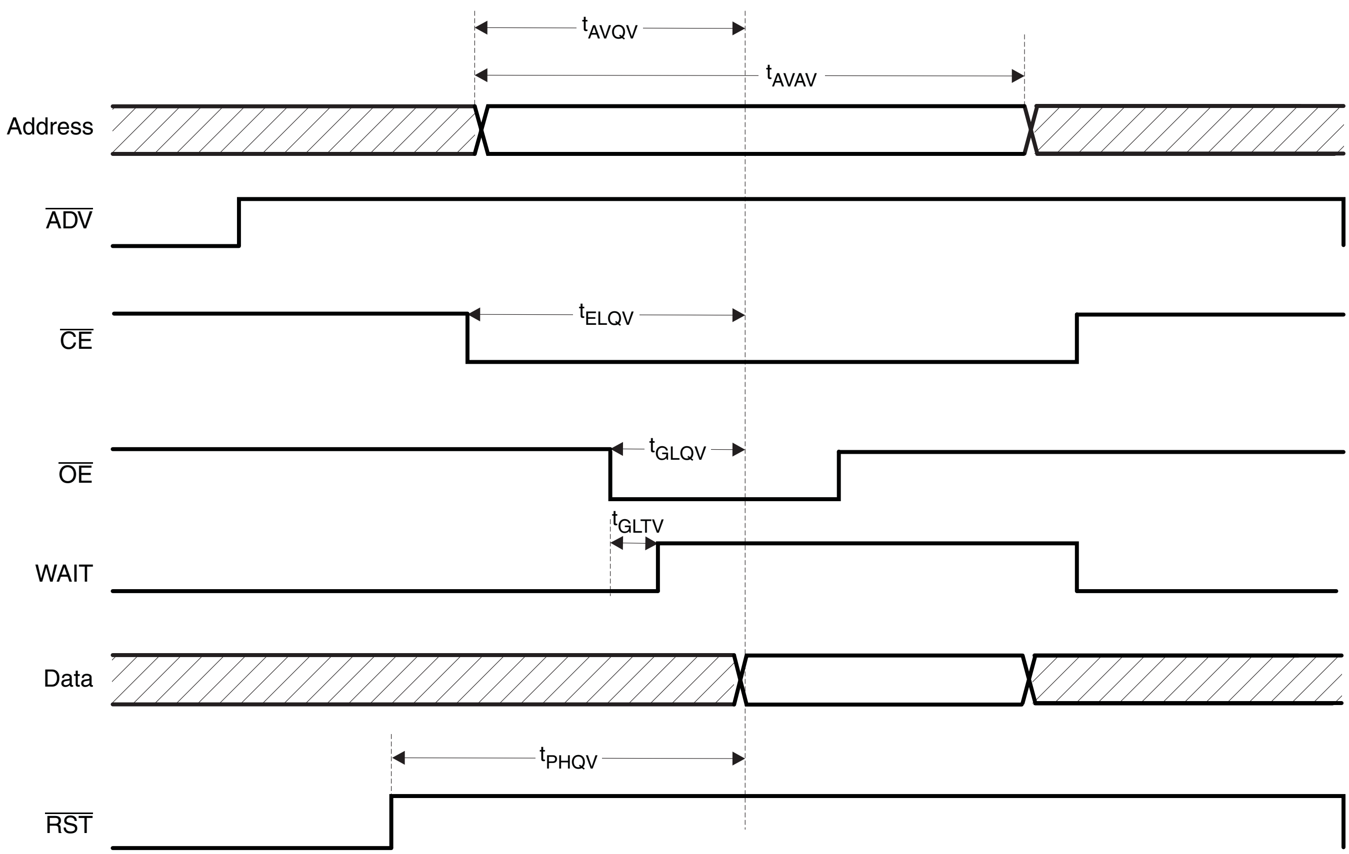


Figure 9. Parrallel Flash Read Timing

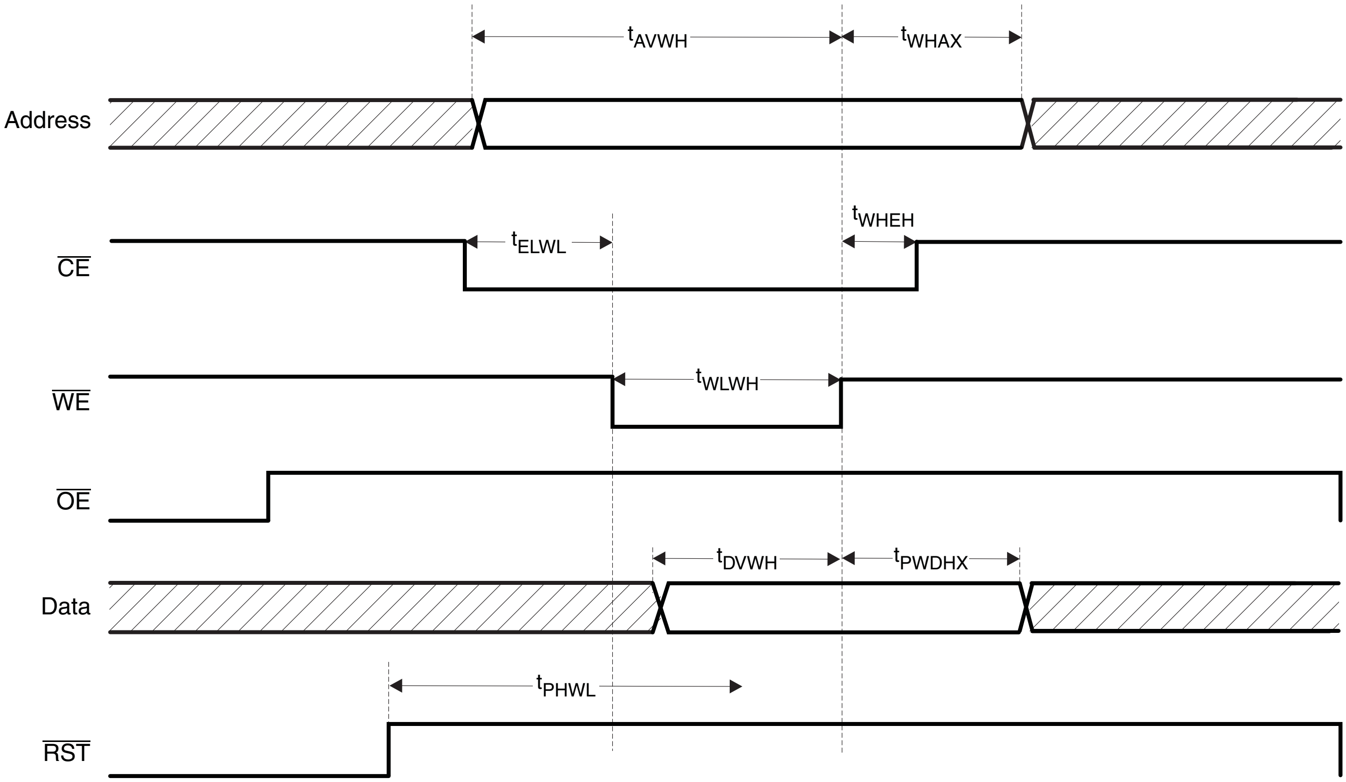


Figure 10. Parrallel Flash Write Timing

Recommended Parallel Flash Devices

PART NUMBER	MANUFACTURER	SIZE
JS28F00AP30BF	Numonyx	128 Mbit

Serial Flash Memory Interface

The DLPC200 controller flash memory interface consists of a SPI flash serial interface at 33.3 MHz (nominal).

SERIAL FLASH INTERFACE TIMING REQUIREMENTS

PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency, SPI_CLK	DC	33	MHz
t_{p_clkper}	Clock period, SPI_CLK		30.03	ns
t_{p_wh}	Pulse width low, SPI_CLK	6		ns
t_{p_wl}	Pulse width high, SPI_CLK	6		ns
t_{p_su}	Setup Time – SPI_DIN valid before SPI_CLK rising edge	2		ns
t_{p_h}	Hold Time – SPI_DIN valid after SPI_CLK rising edge	5		ns

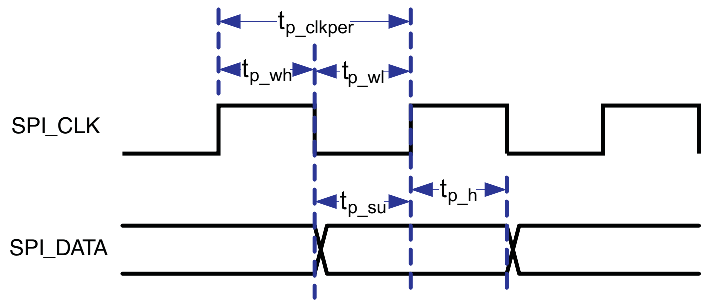


Figure 11. Flash Memory Interface Timing

Recomended Serial Flash Devices shows the Serial Flash parts that were tested by TI and found to work properly with the DLPC200.

Recommended Serial Flash Devices

PART NUMBER	MANUFACTURER	SIZE
M25P64	Numonyx	64 Mbit
W25Q64BV	Winbond	64 Mbit

STATIC RAM Interface

The DLPC200 controller Satic RAM (SRAM) interface consists of a high performance CMOS Static RAM organized as 128K words by 16 bits (2 Mbit).

STATIC RAM INTERFACE TIMING REQUIREMENTS

PARAMETER		MIN	MAX	UNIT
t_{RC}	Read cycle time	10		ns
t_{AA}	Address to data valid		10	ns
t_{OHA}	Data hold from address change	3		ns
t_{WC}	Write cycle time	10		ns
t_{SCE}	CE low to write end	7		ns
t_{AW}	Address setup to write end	7		ns
t_{HA}	Address hold from write end	0		ns
t_{SA}	Address setup to write start	0		
t_{PWE}	WE pulse width	7		
t_{SD}	Data setup to write end	5		
t_{HD}	Data hold from write end	0		

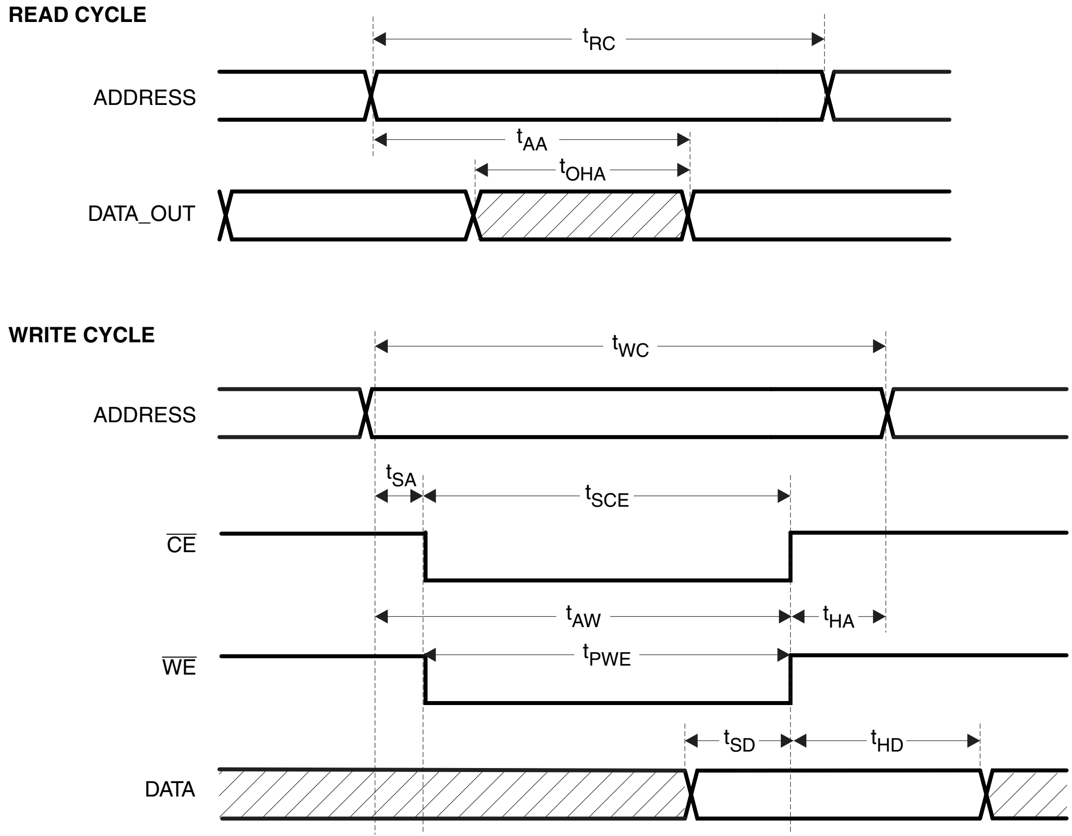


Figure 12. SRAM Interface Timing

Recomended Serial Flash Devices shows the Serial Flash parts that were tested by TI and found to work properly with the DLPC200.

Recommended Static RAM Devices

PART NUMBER	MANUFACTURER	SIZE
CY7C1011DV33	Cypress	2 Mbit

DMD Interface

The DLPC200 ASIC DMD interface consists of a 200 MHz (nominal) DDR output-only interface with LVDS signaling.

DMD INTERFACE TIMING REQUIREMENTS

PARAMETER		MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency, DCLK_A & DCLK_B		200		MHz
t_{p_clkper}	Clock period, DCLK_A & DCLK_B		5.0		ns
t_{p_wh}	Pulse width low, DCLK_A & DCLK_B		1.25		ns
t_{p_wl}	Pulse width high, DCLK_A & DCLK_B		1.25		ns
t_{skew}	Channel B relative to channel A	-1.25		1.25	ns
t_{p_su}	Output setup time – D_A(0:15) & D_B(0:15) relative to both rising and falling edges of DCLK_A & DCLK_B, respectively	0.35			ns
t_{p_h}	Output hold time – D_A(0:15) & D_B(0:15) relative to both rising and falling edges of DCLK_A & DCLK_B, respectively	0.35			ns

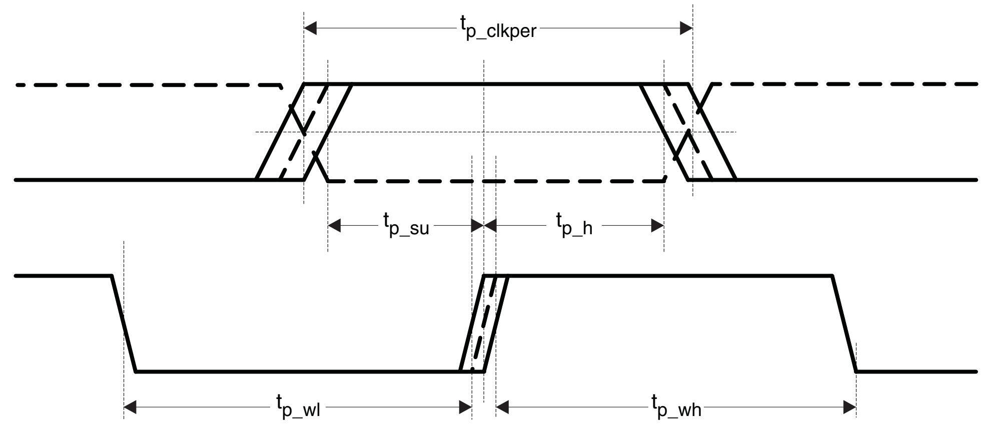


Figure 13. DMD I/F Timing

DAD Interface

The DLPC200 ASIC DAD interface consists of a 125 kMHz (nominal) serial communications port (SCP).

DAD INTERFACE TIMING REQUIREMENTS

PARAMETER		MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency		125	125	kHz
t_{p_clkper}	Clock period			8	us
t_{p_wh}	Pulse width low			4	us
t_{p_wl}	Pulse width high			4	us
t_{p_su}	SCPDI setup time	7.3			ns
t_{p_h}	SCPDI hold time	5.7			ns

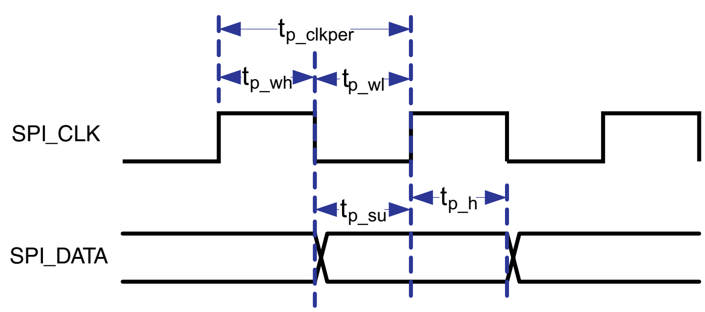


Figure 14. DAD I/F Timing

DDR2 SDR Memory Interface

The DDR2 SDRAM is a high-speed CMOS, dynamic random access memory. It is internally configured as a multibank DRAM. The Controller DDR-2 Memory interface consists of four 32 Mbit by 16-bit wide, DDR-2 interface with double data rate signaling operating at 133.33MHz (nominal). A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READ commands and by the memory controller during WRITE commands. DQS is edge-aligned with data for READ commands and center-aligned with data for WRITE commands.

The DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK#

DDR2 SDR Memory Interface (continued)

going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK. Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

DDR2 SDR MEMORY INTERFACE TIMING REQUIREMENTS

PARAMETER		MIN	MAX	UNIT
t_{CYCLE}	Cycle time reference	5.0	8.0	ns
t_{CH}	CK high pulse width[1]	2.4	4.16	ns
t_{CL}	CK low pulse width[2]	2.4	4.16	ns
t_{CMS}	Command setup	200		ps
t_{CMH}	Command hold	275		ps
t_{AS}	Address setup	400		ps
t_{AH}	Address hold	400		ps
t_{DS}	Write data setup	1.5		ns
t_{DH}	Write data hold	1.5		ns
t_{AC}	Read data access time	-450	450	ps
t_{OH}	Read data hold time		340	ps
t_{LZ}	Read data low impedance time	-900	450	ps
t_{HZ}	Read data high impedance time		450	ps

(1) Output setup/ hold numbers already account for controller clock jitter. Only routing skew and memory setup/ hold need be considered in system timing analysis.
(2) Output setup/ hold numbers already account for controller clock jitter. Only routing skew and memory setup/ hold need be considered in system timing analysis.

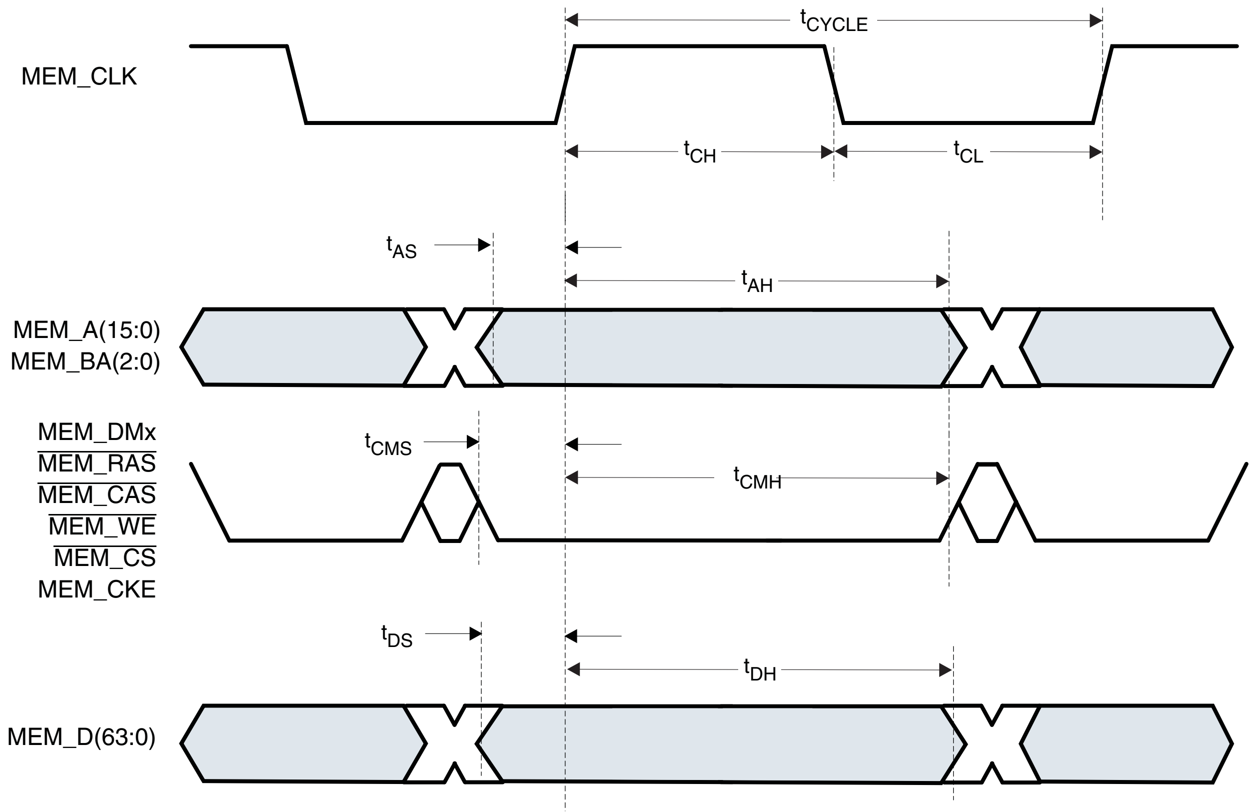


Figure 15. SDR Memory I/F Write Timing

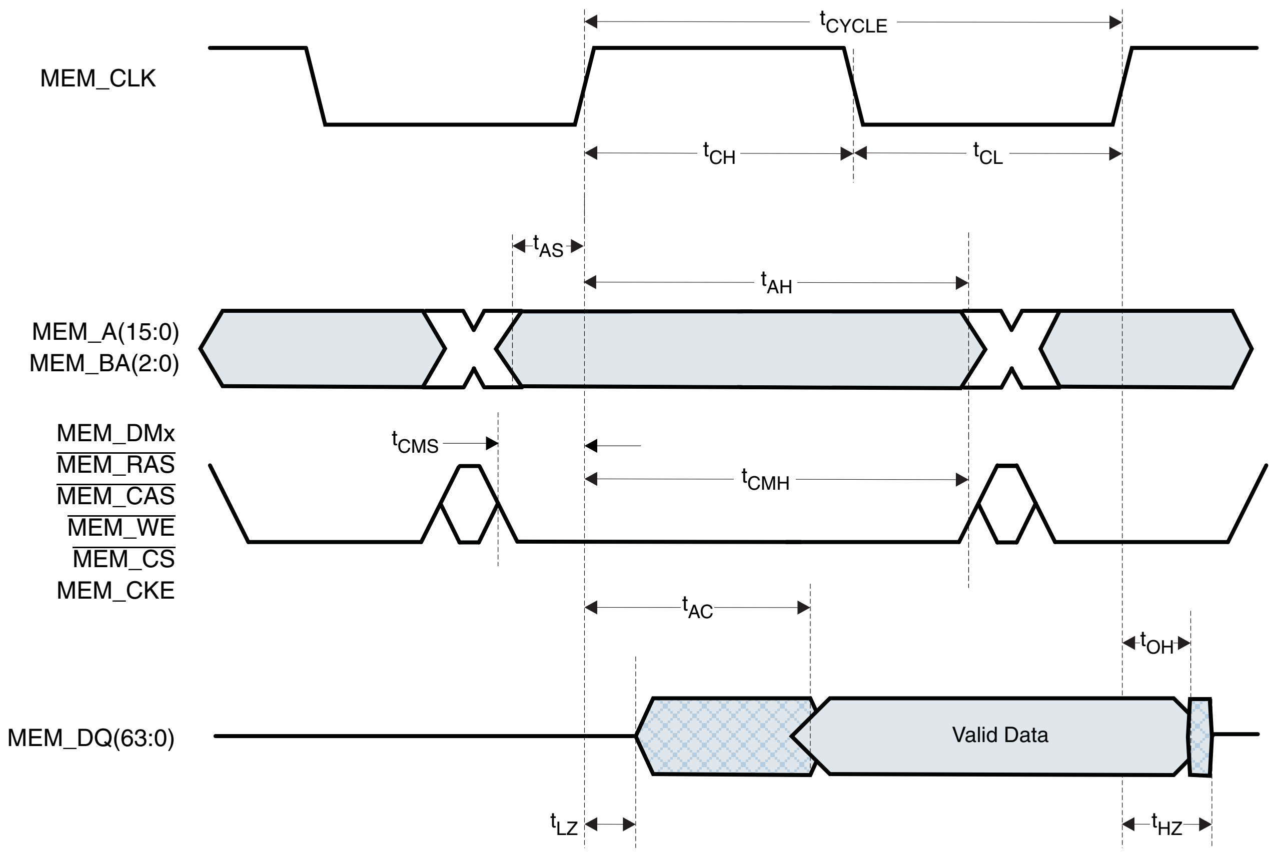


Figure 16. SDR Memory I/F Read Timing

SDRAM Memory

The DLPC200 requires an external DDR2 SDR SDRAM. The DLPC200 supports the use of four 512 Mbit SDRAMs. The requirements for the SDRAMs are:

- SDRAM type: DDR2
- Speed: 133 MHz minimum
- 16-bit interface size: 32 Mbit
- Supply voltage: 1.8 V

Supported SDRAM Devices shows the SDRAM parts that have been tested by TI and found to work properly with the DLPC200.

Recommended SDRAM Devices

PART NUMBER	MANUFACTURER	SIZE
MT47H32M16R	Micron	512 Mbit

POWER UP REQUIREMENTS

Details about the chip power up requirements are included in the DLPZ004 Chipset datasheet. For the DLPC200, there is a 50 MHz reference clock that must meet the specifications listed in the table below. Additionally, at power up, the 3.3 V supply must be stable for 2 seconds before the global reset ($\overline{RESET}$) occurs and then PWR_GOOD occurs within 20 msec.

Table 2. Reference Clock Oscillator Requirements

PART NUMBER	FREQUENCY STABILITY	FREQUENCY	SUPPLY VOLTAGE
ASV-50.000MHZ-E-J-T	±20 ppm (0.002% or ±0.001 MHz)	50 MHz	3.3 V

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	VALUE	UNIT
V_{CC12}	Supply voltage range (2)		–0.5 V to 1.80	V
V_{CCIO18}			–0.5 V to 3.90	
V_{CCA25_DPLL}			–0.5 V to 3.75	
V_{CCD_PLL1-4}			-0.5 V to 1.80	
V_I	Input voltage range(3)	1.8 V, 2.5 V, 3.3 V	–0.5 V to 3.95	V
T_J	Operating junction temperature range		–40°C to 125	°C
T_{stg}	Storage temperature range		–65°C to 150	°C
HBM	Electrostatic discharge voltage using the Human Body Model		± 2000	V
CD	Electrostatic discharge voltage using the Charged Device Model		± 500	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND, and at the device not at the power supply.
(3) Applies to external input and bidirectional buffers.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
V_{CC12}	1.2-V supply voltage, core logic		1.15	1.2	1.25	V
V_{CC18}	1.5-V supply voltage, HSTL output buffers		1.71	1.8	1.89	V
V_{CCA25_DPLL}	2.5-V analog voltage for PLL regulator		2.375	2.5	2.625	V
V_{CCD_PLL1-4}	1.2-V supply voltage, for PLL		1.15	1.2	1.25	V
V_I	Input voltage		–0.5		3.6	V
V_O	Output voltage		0		V_{CCIO}	V
t_{Ramp}	Power supply ramp time		50 us		3 ms	-
T_J	Operating junction temperature(1)		0		70	°C
R_C	Case-to-ambient thermal resistance	T_A = ambient temperature P = Power			[(T_J – T_A) / P] - 3.3	°C/W

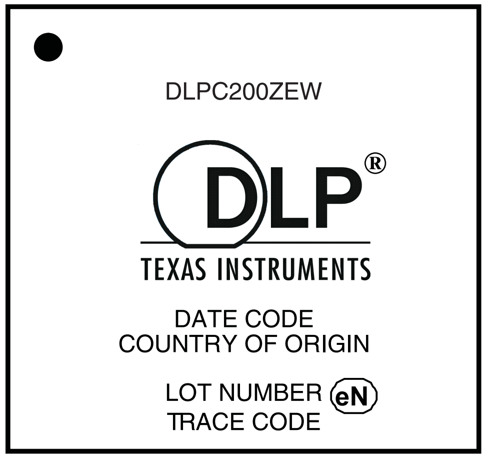
(1) Heat sink not required for 0 to 55, but for 55 to 70, low profile (15 mm) heat sink recommended

Thermal Considerations

The underlying thermal limitation for the DLPC200 is that the maximum operating junction temperature (T_J) not be exceeded (see Recommended Operating Conditions). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC200 and power dissipation of surrounding components. The DLPC200's package is designed primarily to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

Device Marking

Device marking should be as shown below.



Marking Key:

- Line 1 : TI Reference Number
- Line 2 : Device Name
- Line 3 : DLP® logo
- Line 4 : Date Code
- Line 5 : Country of Origin
- Line 6 : Assembly Lot Number
- Line 7 : Trace Code

TI Internal: Drawing #2511315

Revision History

REVISION	SECTION(S)	COMMENT
*	All	Initial release
A	Update junction temperature and notate need for heat sink	Update to Recommended Operating Conditions
	Added new section for power up requirements	Added section for power up requirements
	Added reference for TI internal drawing number	Added TI interal drawing number
	updated parameter names to match figure	Update to Image sync and blanking requirements table
	Removed unused types, updated values	Update to I/O Characteristics table
	Added/changed pin names, updated descriptions	Update to Terminal Functions table

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
DLPC200ZEW	ACTIVE	BGA	ZEW	780	1	TBD	POST-PLATE	Level-3-260C-168 HR	Purchase Samples
DLPC200ZEWT	ACTIVE	BGA	ZEW	780	10	TBD	Call TI	Level-3-260C-168 HR	Purchase Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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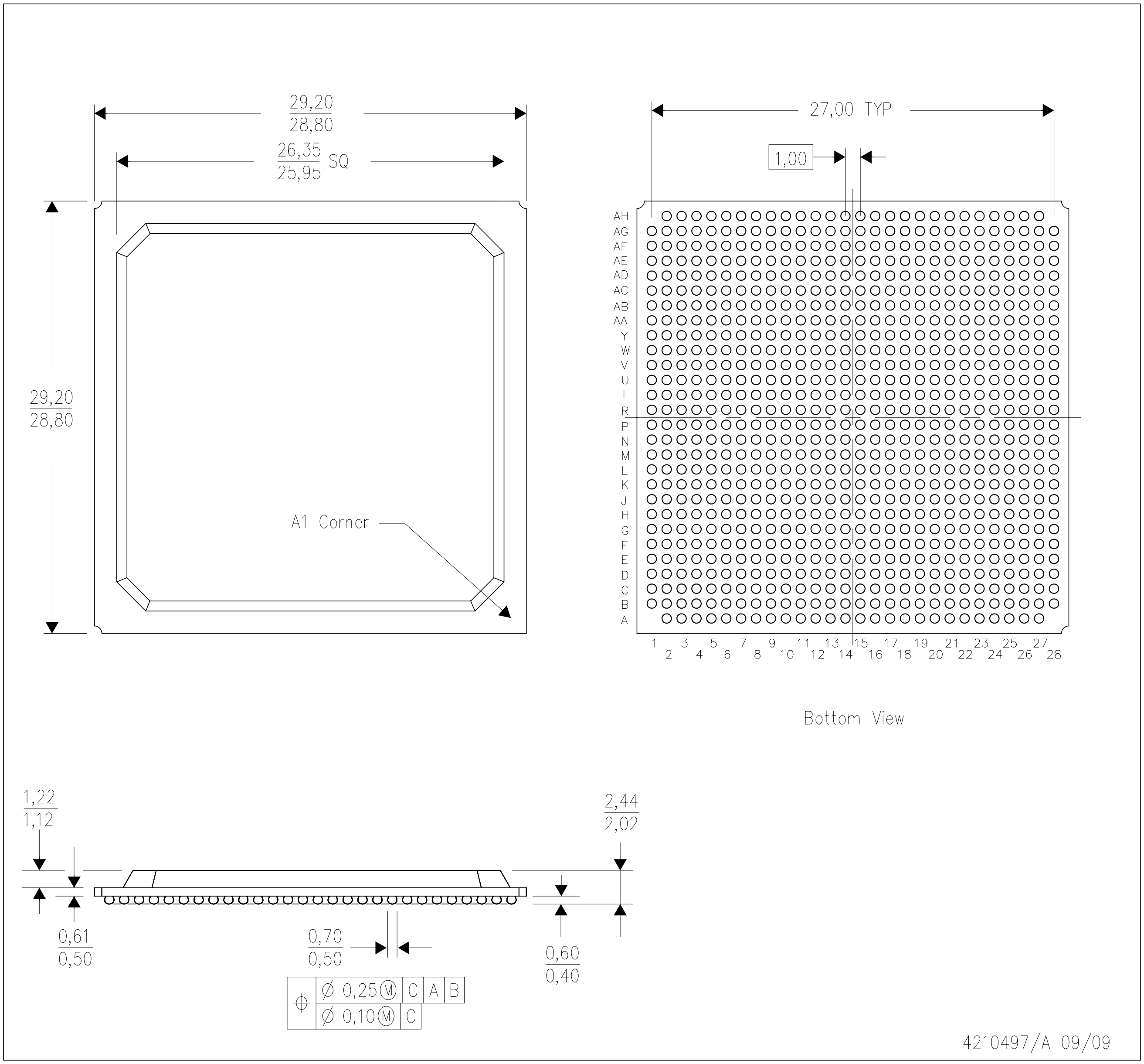
ZEW (S-PBGA-N780) PLASTIC BALL GRID ARRAY



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS–034, Variation: AAM–1.

D. This package is Pb–free.

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