19-3033; Rev 1; 4/04

MAXIM

VRM 9.0/VRM 9.1, Dual-Phase, Parallelable, Average-Current-Mode Controller

General Description

The MAX5037A dual-phase, PWM controller provides high-output-current capability in a compact package with a minimum number of external components. The MAX5037A utilizes a dual-phase, average-current-mode control that enables optimal use of low $R_{DS(ON)}$ MOSFETs, eliminating the need for external heatsinks even when delivering high output currents.

Differential sensing enables accurate control of the output voltage, while adaptive voltage positioning provides optimum transient response. An internal regulator enables operation with either +5V or +12V input voltage without the need for additional voltage sources. The high switching frequency, up to 500kHz per phase, and dual-phase operation allow the use of low output inductor values and input capacitor values. This accommodates the use of PC board-embedded planar magnetics achieving superior reliability, current sharing, thermal management, compact size, and low system cost.

The MAX5037A also features a clock input (CLKIN) for synchronization to an external clock, and a clock output (CLKOUT) with programmable phase delay (relative to CLKIN) for paralleling multiple phases. The MAX5037A also limits the reverse current in case the bus voltage becomes higher than the regulated output voltage.

The MAX5037A operates over the extended temperature range (-40°C to +85°C) and is available in 44-pin MQFP or thin QFN packages. Refer to the MAX5038A/MAX5041A and MAX5065/MAX5067 data sheets for either a fixed output voltage controller or an adjustable output voltage controller in an SSOP or thin QFN package.

Applications

Servers and Workstations

Point-of-Load High-Current/High-Density Telecom DC-DC Regulators

Networking Systems

Large-Memory Arrays

RAID Systems

High-End Desktop Computers

Features

- **+4.75V to +5.5V or +8V to +28V Input Voltage Range**
- **Up to 60A Output Current**
- **Internal Voltage Regulator for a +12V or +24V Power Bus**
- **Internal 5-Bit DAC VID Control (VRM 9.0/VRM 9.1 Compliant, 0.8% Accuracy)**
- **Programmable Adaptive Output Voltage Positioning**
- **True Differential Remote Output Sensing**
- **Out-of-Phase Controllers Reduce Input Capacitance Requirement and Distribute Power Dissipation**
- **Average-Current-Mode Control**
  - **Superior Current Sharing Between Individual Phases and Paralleled Modules**
  - **Accurate Current Limit Eliminates MOSFET and Inductor Derating**
- **Limits Reverse-Current Sinking in Paralleled Modules**
- **Integrated High-Output-Current Gate Drivers**
- **Selectable Fixed Frequency 250kHz or 500kHz per Phase (Up to 1MHz for Two Phases)**
- **External Frequency Synchronization from 125kHz to 600kHz**
- **Internal PLL with Clock Output for Paralleling Multiple DC-DC Converters**
- **Power-Good Output**
- **Phase Failure Detector**
- **Overvoltage and Thermal Protection**
- **44-Pin MQFP or Thin QFN Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5037AEMH	-40°C to +85°C	44 MQFP
MAX5037AETH	-40°C to +85°C	44 Thin QFN

Pin Configuration appears at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

IN to SGND .....-0.3V to +30V
BST_ to SGND ..... -0.3V to +35V
DH_ to LX_ .....-0.3V to [($V_{BST\_}$ - $V_{LX\_}$) + 0.3V]
DL_ to PGND .....-0.3V to (V_{DD} + 0.3V)
BST_ to LX_ .....-0.3V to +6V
V_{CC} to SGND .....-0.3V to +6V
V_{DD} to PGND .....-0.3V to +6V
SGND to PGND .....-0.3V to +0.3V
All Other Pins to SGND.....-0.3V to (V_{CC} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
44-Pin MQFP (derate 12.7mW/°C above +70°C).....1013mW
44-Pin Thin QFN (derate 27.0mW/°C above +70°C).....2162.2mW
Package Thermal Resistance, θ_{JC} (Thin QFN only).....+2°C/W
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{DD} = +5V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS						
Input Voltage Range	V_{IN}		8		28	V
		Short IN and V_{CC} together for 5V input operation	4.75		5.5	
Quiescent Supply Current	I_Q	EN = V_{CC} or SGND, VID inputs unconnected		4	6	mA
Efficiency	η	I_{LOAD} = 52A (26A per phase)		90		%
STARTUP/INTERNAL REGULATOR						
V_{CC} Undervoltage Lockout	UVLO	V_{CC} rising	4.0	4.15	4.5	V
V_{CC} Undervoltage Lockout Hysteresis				200		mV
V_{CC} Output Accuracy		V_{IN} = 8V to 28V, I_{SOURCE} = 0 to 80mA	4.85	5.1	5.30	V
V_{OUT}/ADAPTIVE VOLTAGE POSITIONING (AVP)						
Nominal Output Voltage Accuracy (VID Setting)		R_{REG} = R_F = 100kΩ, R_{IN} = 1kΩ, no load, Figure 3	-0.8		+0.8	%
		V_{IN} = V_{CC} = 4.75V to 5.5V, or V_{IN} = 8V to 28V, R_{REG} = R_F = 100kΩ, R_{IN} = 1kΩ, no load, Figure 3	-1		+1	
Maximum REG Loading	I_{REG_MAX}		50			µA
REG Accuracy (Voltage Positioning)	d (ΔV_{OUT})	T_A = 0°C to +85°C	-3		+3	%
		T_A = -40°C to +85°C	-5		+5	
Maximum CNTR Loading	I_{CNTR_MAX}		50			µA
Center Voltage Set-Point Accuracy (Note 2)	d (ΔV_{CNTR})	T_A = 0°C to +85°C	-3		+3	%
		T_A = -40°C to +85°C	-5		+5	
MOSFET DRIVERS						
Output Driver Impedance	R_{ON}	Low or high output		1	3	Ω
Output Driver Peak Source/Sink Current	$I_{DH\_}$, $I_{DL\_}$			4		A

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{DD} = +5V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Nonoverlap Time	t_{NO}	$C_{DH\_/DL\_}$ = 5nF		60		ns
OSCILLATOR AND PLL						
Switching Frequency	f_{SW}	CLKIN = SGND	238	250	262	kHz
		CLKIN = V_{CC}	475	500	525	
PLL Lock Range	f_{PLL}		125		600	kHz
PLL Locking Time	t_{PLL}			200		µs
CLKOUT Phase Shift (at f_{SW} = 125kHz)	ϕ_{CLKOUT}	PHASE = V_{CC}	115	120	125	Degrees
		PHASE = unconnected	85	90	95	
		PHASE = SGND	55	60	65	
CLKIN Input Pulldown Current	I_{CLKIN}		3	5	7	µA
CLKIN High Threshold	V_{CLKINH}		2.4			V
CLKIN Low Threshold	V_{CLKINL}				0.8	V
CLKIN High Pulse Width	t_{CLKIN}		200			ns
PHASE High Threshold	V_{PHASEH}		4			V
PHASE Low Threshold	V_{PHASEL}				1	V
PHASE Input Bias Current	$I_{PHASEBIAS}$		-50		+50	µA
CLKOUT Output Low Level	$V_{CLKOUTL}$	I_{SINK} = 2mA (Note 3)			100	mV
CLKOUT Output High Level	$V_{CLKOUTH}$	I_{SOURCE} = 2mA (Note 3)	4.5			V
CURRENT LIMIT						
Average Current-Limit Threshold	V_{CL}	CSP_ to CSN_	45	48	51	mV
Reverse Current-Limit Threshold	V_{CLR}	CSP_ to CSN_	-3.9		-0.2	mV
Cycle-by-Cycle Current Limit	V_{CLPK}	CSP_ to CSN_ (Note 3)	90	112	130	mV
Cycle-by-Cycle Overload Response Time	t_R	$V_{CSP\_}$ to $V_{CSN\_}$ = +150mV		260		ns
CURRENT-SENSE AMPLIFIER						
CSP_ to CSN_ Input Resistance	$R_{CS\_}$			4		kΩ
Common-Mode Range	$V_{CMR(CS)}$		-0.3		+3.6	V
Input Offset Voltage	$V_{OS(CS)}$		-1		+1	mV
Amplifier Gain	$A_{V(CS)}$			18		V/V
3dB Bandwidth	f_{3dB}			4		MHz
CURRENT-ERROR AMPLIFIER (TRANSCONDUCTANCE AMPLIFIER)						
Transconductance	gm_{ca}			550		µS
Open-Loop Gain	$A_{VOL(CE)}$	No load		50		dB
DIFFERENTIAL VOLTAGE AMPLIFIER (DIFF)						
Common-Mode Voltage Range	$V_{CMR(DIFF)}$		-0.3		+1.0	V
DIFF Output Voltage	V_{CM}	V_{SENSE+} = V_{SENSE-} = 0		0.6		V
Input Offset Voltage	$V_{OS(DIFF)}$		-2		+2	mV
Amplifier Gain	$A_{V(DIFF)}$		0.997	1	1.003	V/V
3dB Bandwidth	f_{3dB}	C_{DIFF} = 20pF		3		MHz
Minimum Output Current Drive	$I_{OUT(DIFF)}$		1.0			mA

VRM 9.0/VRM 9.1, Dual-Phase, Parallelable, Average-Current-Mode Controller

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{DD} = +5V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SENSE+ to SENSE- Input Resistance	$R_{VS\_}$		50	100		kΩ
VOLTAGE-ERROR AMPLIFIER (EAOUT)						
Open-Loop Gain	$A_{VOL(EA)}$			70		dB
Unity-Gain Bandwidth	f_{UGEA}			3		MHz
EAN Input Bias Current	$I_{B(EA)}$	CNTR and REG = open, V_{EAN} = 2.0V	-100		+100	nA
Error-Amplifier Output Clamping Voltage	$V_{CLAMP(EA)}$	With respect to V_{CM}	810		918	mV
POWER-GOOD, PHASE FAILURE DETECTION, OVERVOLTAGE PROTECTION, AND THERMAL SHUTDOWN						
PGOOD Trip Level	V_{OV}	PGOOD goes low when V_{OUT} is outside of this window	+6	+8	+10	% V_O (VID)
	V_{UV}		-12.5	-10	-8.5	
PGOOD Output Low Level	V_{PGLO}	I_{SINK} = 4mA			0.20	V
PGOOD Output Leakage Current	I_{PG}	PGOOD = V_{CC}			1	µA
Phase Failure Trip Threshold	V_{PH}	PGOOD goes low when CLP_ is higher than V_{PH}		2.0		V
OVPIN Trip Threshold	OVP_{TH}	Above VID programmed output voltage	+10	+13	+16	% V_O (VID)
OVPOUT Source/Sink Current	I_{OVPOUT}	V_{OVPOUT} = 2.5V	15	20		mA
OVPIN Input Resistance	R_{OVPIN}		190	280	370	kΩ
Thermal Shutdown	T_{SHDN}			150		°C
Thermal-Shutdown Hysteresis				8		°C
LOGIC INPUTS FOR VID						
Logic-Input Pullup Resistors	R_{VID}		8	12	20	kΩ
Logic-Input Low Voltage	V_{IL}				0.8	V
Logic-Input High Voltage	V_{IH}		1.7			V
VID Internal Pullup Voltage	V_{VID}	All VID_ inputs unconnected	2.8	2.9	3.2	V
EN INPUT						
EN Input Low Voltage	V_{ENL}				1	V
EN Input High Voltage	V_{ENH}		3			V
EN Pullup Current	I_{EN}		4.5	5	5.5	µA

Note 1: Specifications from -40°C to 0°C are guaranteed by characterization but not production tested.

Note 2: CNTR voltage accuracy is defined as the center of the adaptive voltage-positioning window (see *Adaptive Voltage Positioning* section).

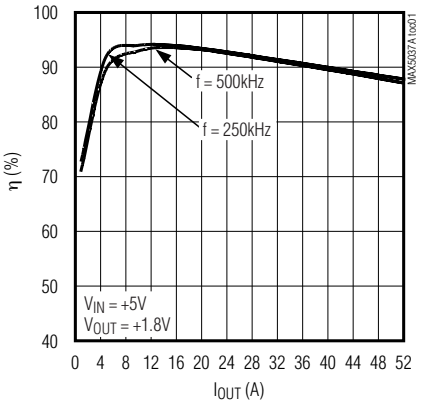
Note 3: Guaranteed by design. Not production tested.

Note 4: See *Peak-Current Comparator* section.

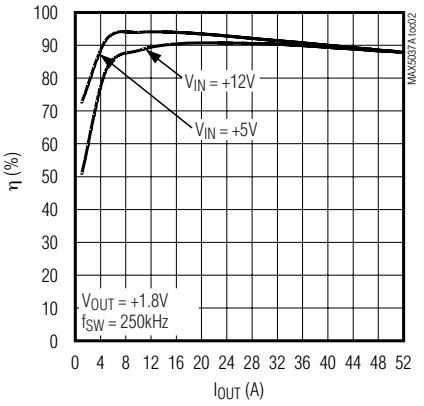
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

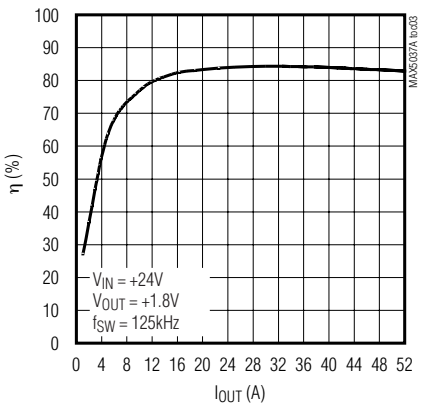
EFFICIENCY vs. OUTPUT CURRENT AND INTERNAL OSCILLATOR FREQUENCY



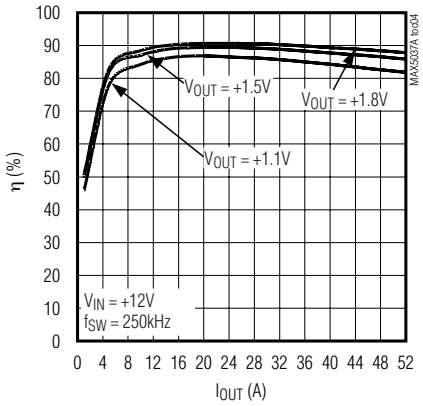
EFFICIENCY vs. OUTPUT CURRENT AND INPUT VOLTAGE



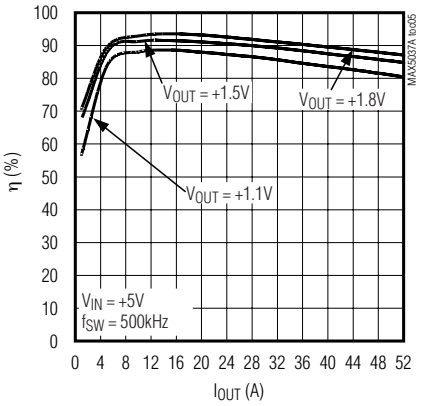
EFFICIENCY vs. OUTPUT CURRENT



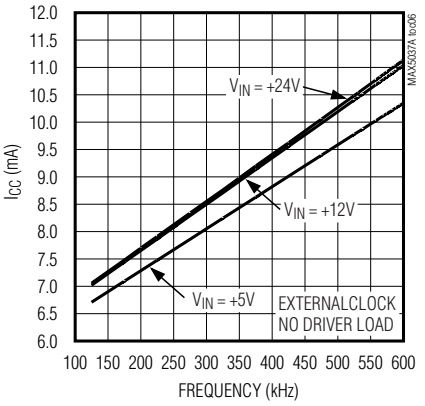
EFFICIENCY vs. OUTPUT CURRENT AND OUTPUT VOLTAGE



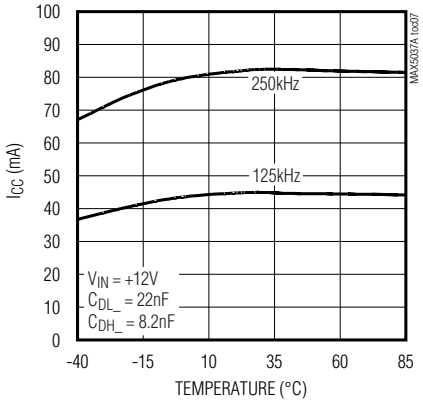
EFFICIENCY vs. OUTPUT CURRENT AND OUTPUT VOLTAGE



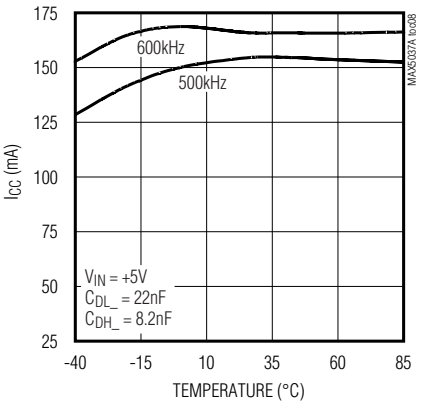
SUPPLY CURRENT vs. FREQUENCY AND INPUT VOLTAGE



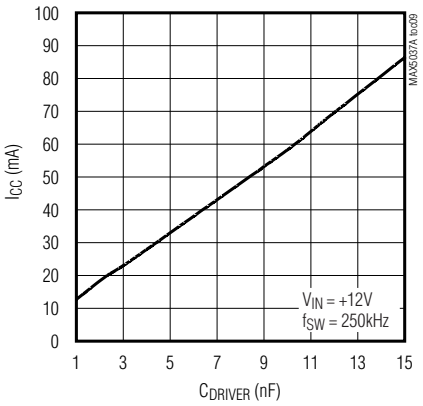
SUPPLY CURRENT vs. TEMPERATURE AND FREQUENCY



SUPPLY CURRENT vs. TEMPERATURE AND FREQUENCY



SUPPLY CURRENT vs. LOAD CAPACITANCE PER DRIVER

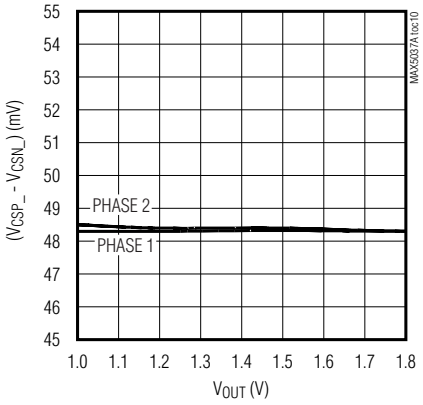


VRM 9.0/VRM 9.1, Dual-Phase, Parallelable, Average-Current-Mode Controller

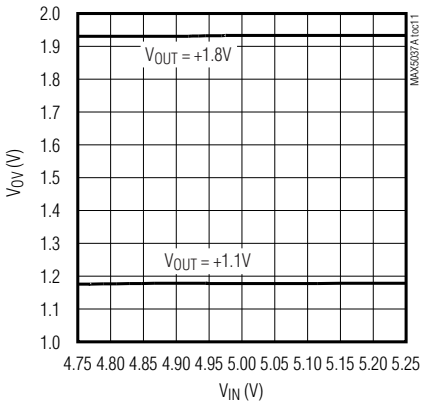
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

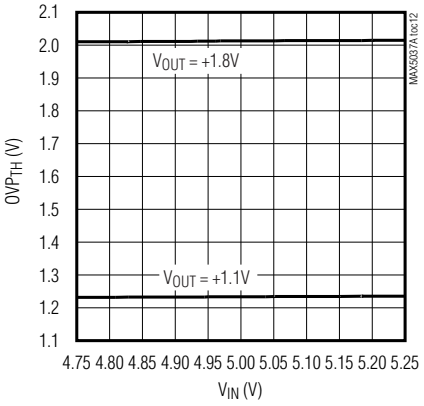
CURRENT-SENSE THRESHOLD vs. OUTPUT VOLTAGE



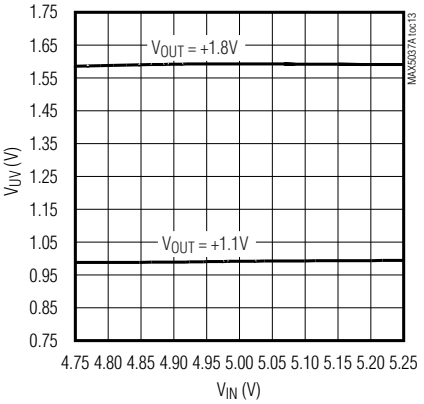
OVERVOLTAGE THRESHOLD (PGOOD) vs. INPUT VOLTAGE



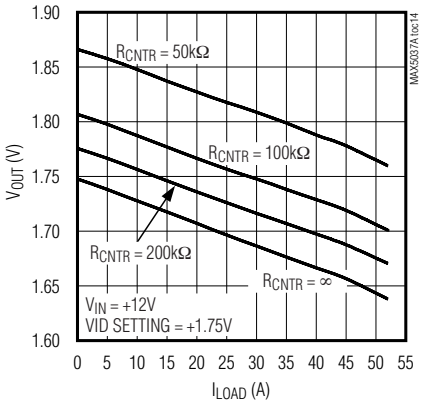
OVERVOLTAGE THRESHOLD (OVPOUT) vs. INPUT VOLTAGE



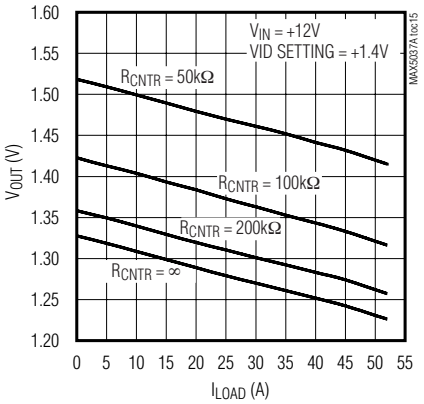
UNDERVOLTAGE THRESHOLD (PGOOD) vs. INPUT VOLTAGE



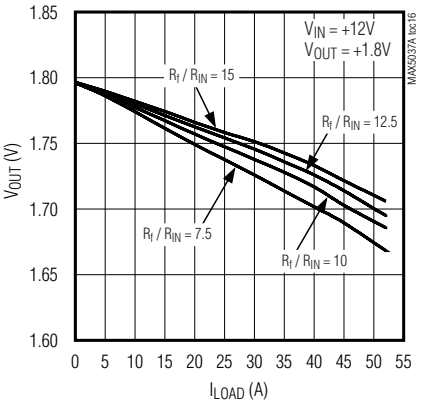
OUTPUT VOLTAGE vs. I_{LOAD} AND R_{CNTR}



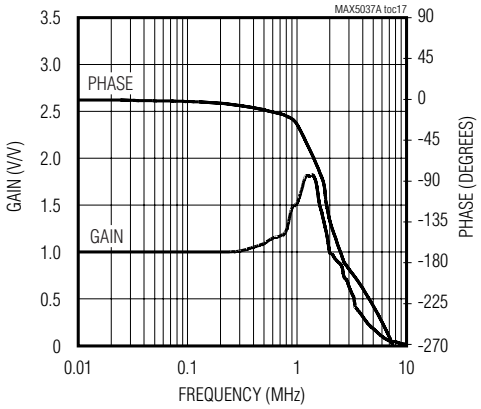
OUTPUT VOLTAGE vs. I_{LOAD} AND R_{CNTR}



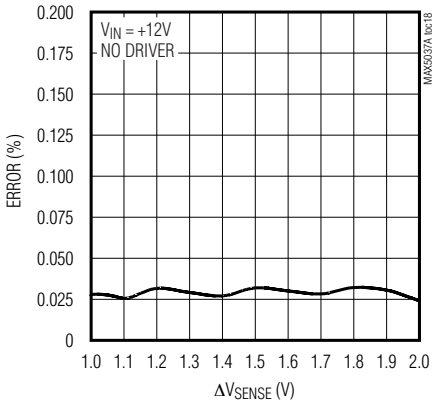
OUTPUT VOLTAGE vs. OUTPUT CURRENT AND ERROR AMP GAIN (R_F / R_{IN})



DIFFERENTIAL AMPLIFIER BANDWIDTH



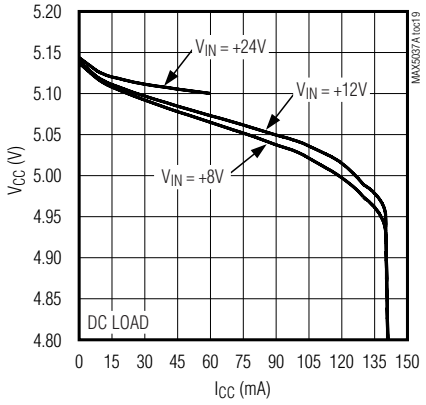
DIFF OUTPUT ERROR vs. SENSE+ TO SENSE- VOLTAGE



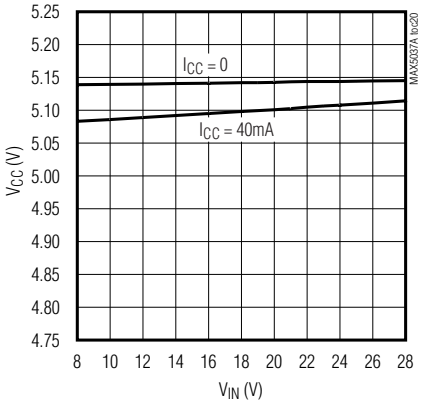
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

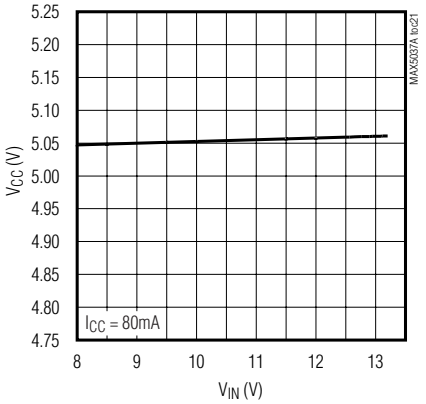
V_{CC} LOAD REGULATION vs. INPUT VOLTAGE



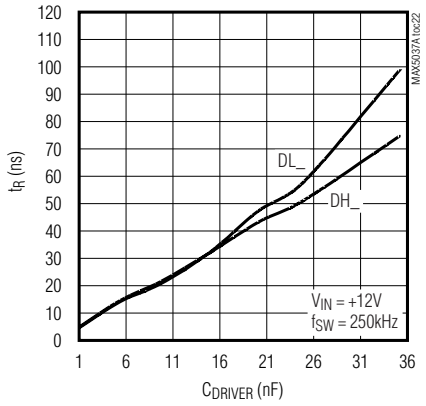
V_{CC} LINE REGULATION



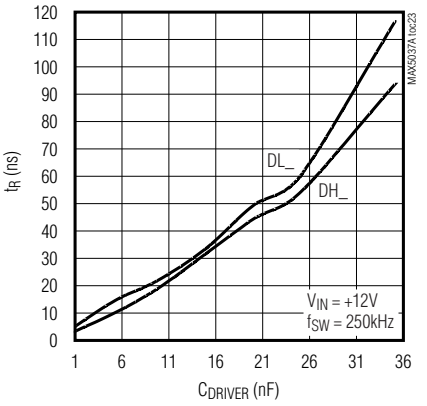
V_{CC} LINE REGULATION



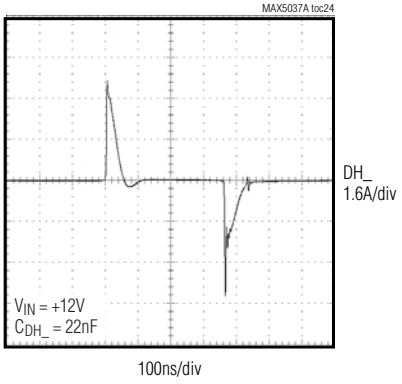
DRIVER RISE TIME vs. DRIVER LOAD CAPACITANCE



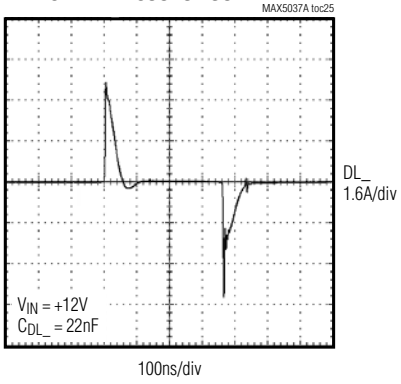
DRIVER FALL TIME vs. DRIVER LOAD CAPACITANCE



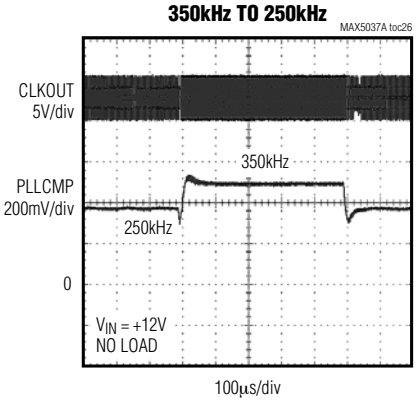
HIGH-SIDE DRIVER (DH_) SINK AND SOURCE CURRENT



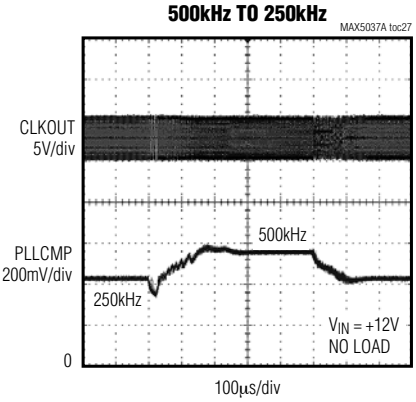
LOW-SIDE DRIVER (DL_) SINK AND SOURCE CURRENT



PLL LOCKING TIME 250kHz TO 350kHz AND 350kHz TO 250kHz



PLL LOCKING TIME 250kHz TO 500kHz AND 500kHz TO 250kHz

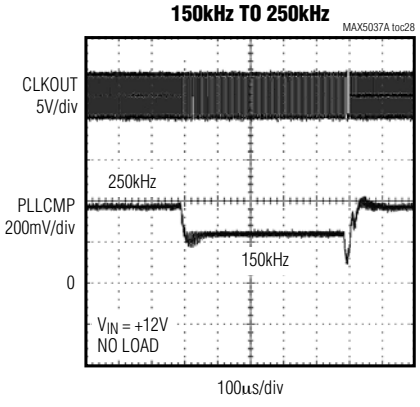


VRM 9.0/VRM 9.1, Dual-Phase, Parallelable, Average-Current-Mode Controller

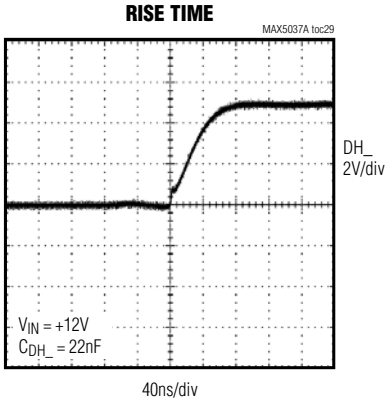
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

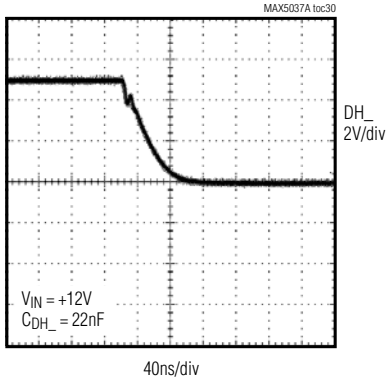
PLL LOCKING TIME 250kHz TO 150kHz AND 150kHz TO 250kHz



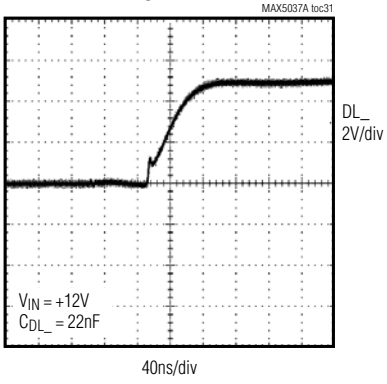
HIGH-SIDE DRIVER (DH_) RISE TIME



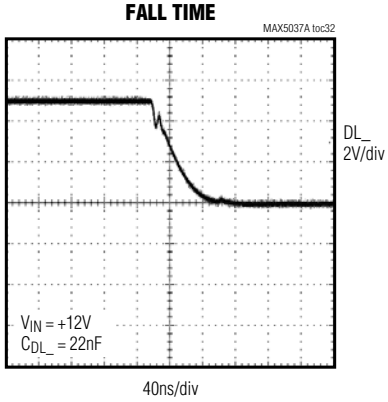
HIGH-SIDE DRIVER (DH_) FALL TIME



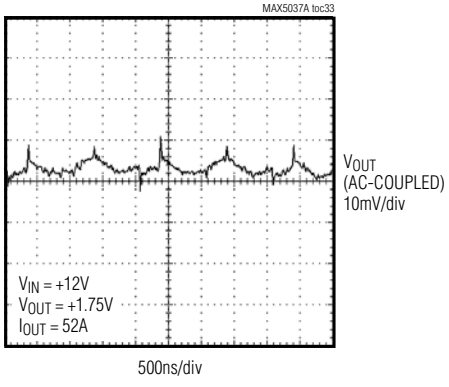
LOW-SIDE DRIVER (DL_) RISE TIME



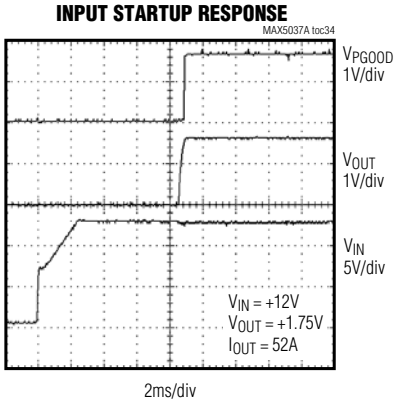
LOW-SIDE DRIVER (DL_) FALL TIME



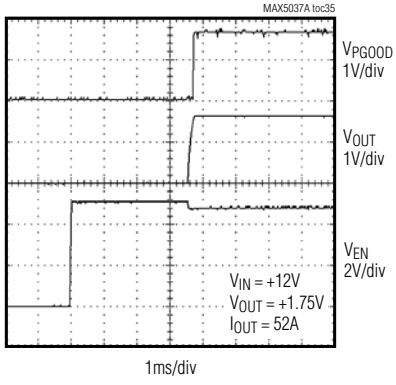
OUTPUT RIPPLE



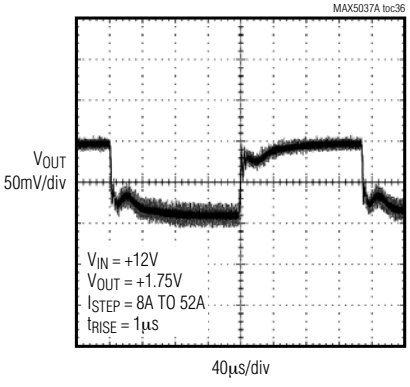
INPUT STARTUP RESPONSE



ENABLE STARTUP RESPONSE



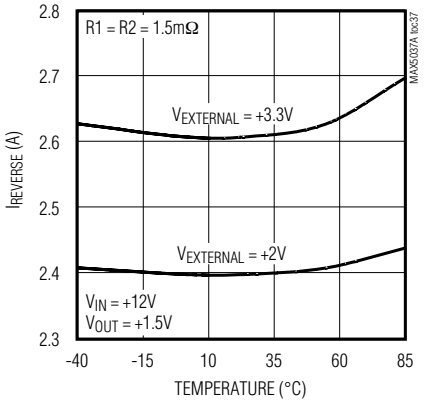
LOAD-TRANSIENT RESPONSE



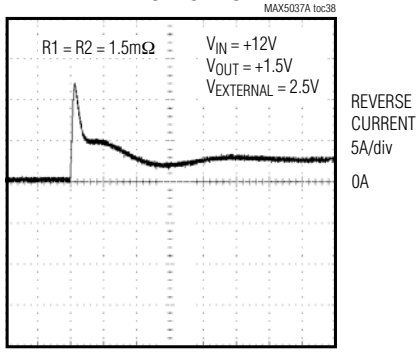
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

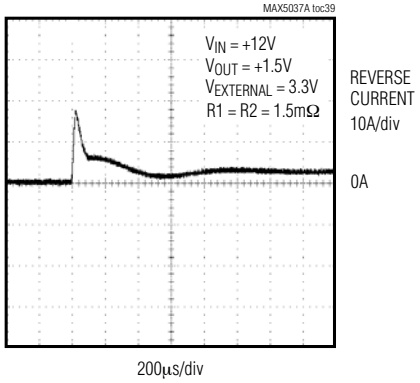
REVERSE-CURRENT SINK vs. TEMPERATURE



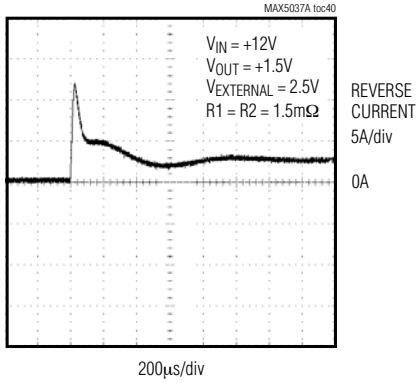
REVERSE-CURRENT SINK AT INPUT TURN-ON



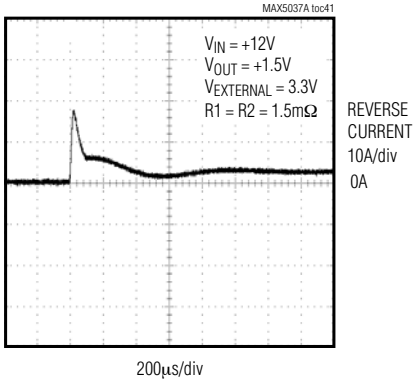
REVERSE-CURRENT SINK AT INPUT TURN-ON



REVERSE-CURRENT SINK AT ENABLE TURN-ON



REVERSE-CURRENT SINK AT ENABLE TURN-ON



VRM 9.0/VRM 9.1, Dual-Phase, Parallelable, Average-Current-Mode Controller

Pin Description

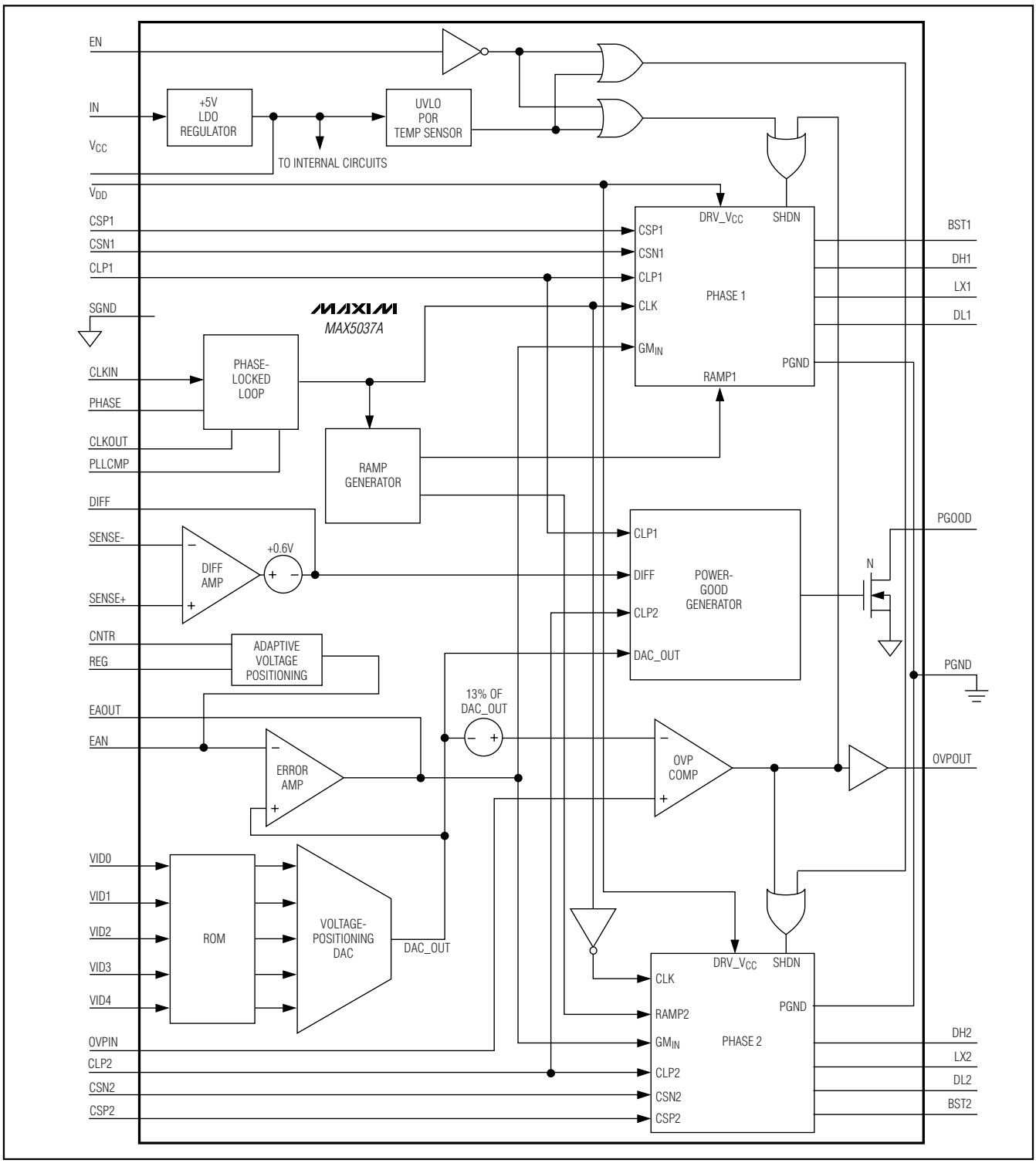
PIN	NAME	FUNCTION
1–4, 44	VID3–VID0, VID4	DAC Code Inputs. VID0 is the LSB and VID4 is the MSB for the internal 5-bit DAC (Table 1). Connect to SGND for logic low or leave open circuit for logic high. These inputs have 12kΩ internal pullup resistors to an internal 3V regulator.
5, 20, 35	SGND	Signal Ground. Ground connection for the internal circuitry. QFN package exposed pad connected to SGND.
6	OVPIN	Overvoltage Protection Circuit Input. Connect DIFF to OVPIN. When OVPIN exceeds +13% above the VID programmed output voltage, OVPOUT latches DH_ low and DL_ high. Toggle EN low to high or recycle the power to reset the latch.
7, 43	CLP1, CLP2	Current-Error Amplifier Output. Compensate the current loop by connecting an R-C network to ground.
8	OVPOUT	Overvoltage Protection Output. Use the OVPOUT active-high, push-pull output to trigger a safety device such as an SCR.
9	PGOOD	Power-Good Output. The open-drain, active-low PGOOD output goes low when the VID programmed output voltage falls out of regulation or a phase failure is detected. The power-good window comparator thresholds are +8% and -10% of the VID programmed output voltage. Forcing EN low also forces PGOOD low.
10	SENSE+	Differential Output Voltage-Sensing Positive Input. Used to sense a remote load. Connect SENSE+ to V_{OUT+} at the load. The device regulates the difference between SENSE+ and SENSE- according to the programmed VID code and adaptive voltage positioning.
11	SENSE-	Differential Output Voltage-Sensing Negative Input. Used to sense a remote load. Connect SENSE- to V_{OUT-} or PGND at the load.
12	DIFF	Differential Remote-Sense Amplifier Output. DIFF is the output of a precision unity-gain amplifier.
13	EAN	Voltage-Error Amplifier Inverting Input. Receives the output of the differential remote-sense amplifier. Referenced to SGND.
14	EAOUT	Voltage-Error Amplifier Output. Connect to an external, gain-setting feedback resistor. The error amplifier gain determines the output voltage load regulation for adaptive voltage positioning.
15	REG	REG Input. A resistor on REG applies the same voltage-positioning window at different VRM voltage settings. For a no-load output voltage (V_{CORE}) equal to VID, set $R_{REG} = R_F$, where the R_F is the feedback resistor of the voltage-error amplifier. V_{REG} internally regulates to the programmed VID output voltage.
16, 39	CSP1, CSP2	Current-Sense Differential Amplifier Positive Input. Senses the inductor current. The differential voltage between CSP_ and CSN_ is amplified internally by the current-sense amplifier gain of 18.
17, 40	CSN1, CSN2	Current-Sense Differential Amplifier Negative Input. Together with CSP_, senses the inductor current.
18	CNTR	Adaptive Voltage Center Position Input. Connect a resistor between CNTR and SGND to program the center of the adaptive V_{OUT} position. V_{CNTR} regulates to +1.22V.
19	EN	Output Enable. A logic low shuts down the power drivers. EN has an internal 5µA pullup current.
21, 33, 37	N.C.	No Connection. Not internally connected.
22, 34	BST1, BST2	Boost Flying-Capacitor Connection. Reservoir capacitor connection for the high-side FET driver supply. Connect a 0.47µF ceramic capacitor between BST_ and LX_.
23, 32	DH1, DH2	High-Side Gate-Driver Output. Drives the gate of the high-side MOSFET.

Pin Description (continued)

PIN	NAME	FUNCTION
24, 31	LX1, LX2	Inductor Connection. Source connection for the high-side MOSFETs. Also serves as the return terminal for the high-side driver.
25, 30	DL1, DL2	Low-Side Gate-Driver Output. Synchronous MOSFET gate drivers for the two phases.
26	V_{DD}	Supply Voltage for Low-Side and High-Side Drivers. V_{CC} powers V_{DD}. Connect a parallel combination of 0.1µF and 1µF ceramic capacitors to PGND and a 1Ω resistor to V_{CC} to filter out the high peak currents of the driver from the internal circuitry.
27	V_{CC}	Internal 5V Regulator Output. V_{CC} is derived internally from the IN voltage. Bypass to SGND with 4.7µF and 0.1µF ceramic capacitors.
28	IN	Supply Voltage Connection. Connect IN to V_{CC} for a 5V system.
29	PGND	Power Ground. Connect PGND, low-side synchronous MOSFET's source, and V_{DD} bypass capacitor returns together.
36	CLKOUT	Oscillator Output. CLKOUT is phase shifted from CLKIN by the amount specified by PHASE. Use CLKOUT to parallel additional MAX5037s.
38	CLKIN	CMOS Logic Clock Input. Drive the internal oscillator with a frequency range between 125kHz and 600kHz. Connect to V_{CC} or SGND. Connect CLKIN to SGND to set the internal oscillator to 250kHz or connect to V_{CC} to set the internal oscillator to 500kHz. CLKIN has an internal 5µA pulldown current.
41	PHASE	Phase Shift Setting Input. Drive PHASE high for 120°, leave PHASE unconnected for 90°, and force PHASE low for 60° of phase shift between the rising edges of CLKOUT and CLKIN/DH1.
42	PLLCMP	External Loop-Compensation Input. Connect compensation network for the phase-locked loop (see *Phase-Locked Loop* section).

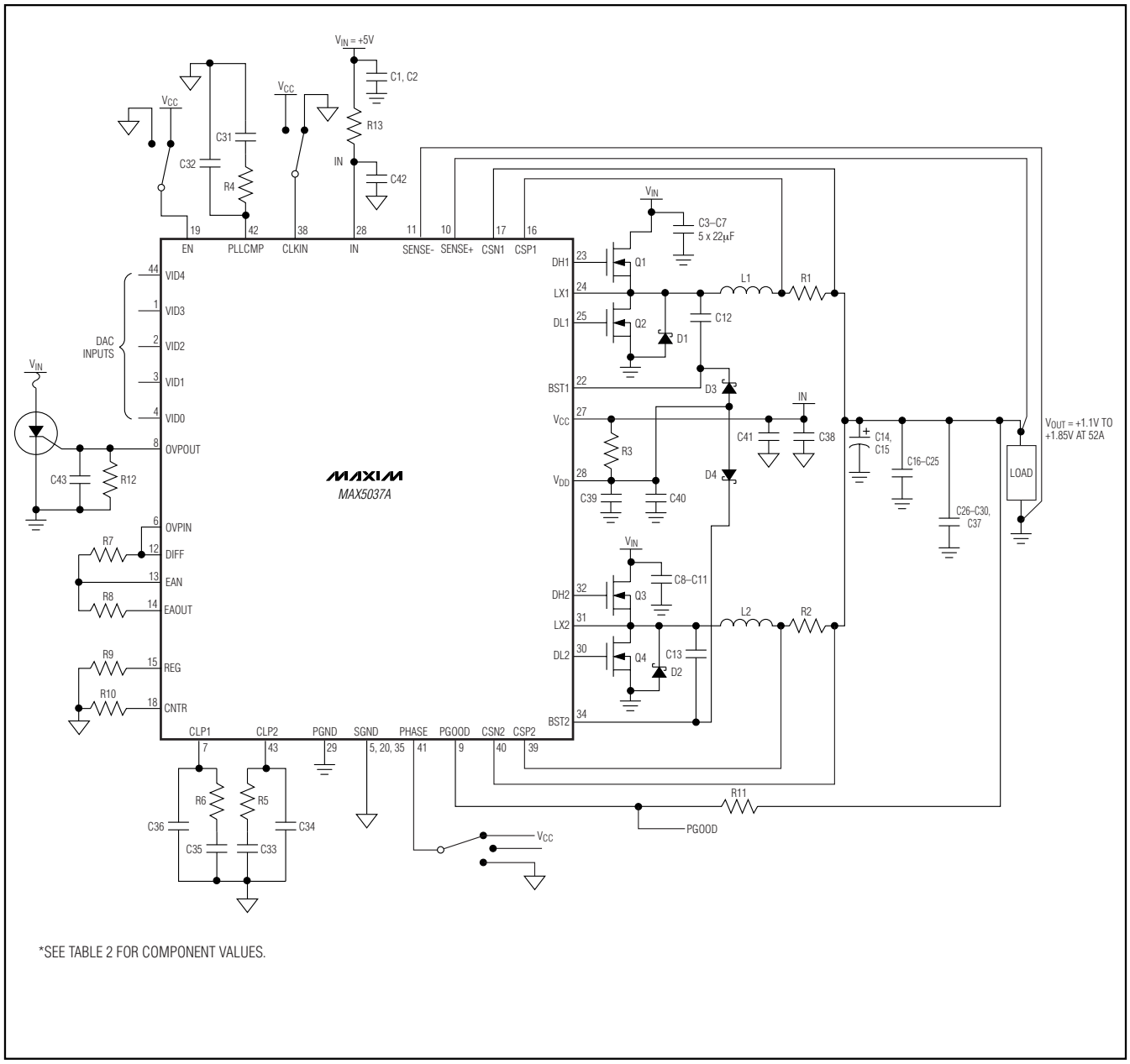
VRM 9.0/VRM 9.1, Dual-Phase, Parallelable, Average-Current-Mode Controller

Functional Diagram



Detailed Description

The MAX5037A (Figures 1 and 2) average-current-mode PWM controller drives two out-of-phase buck converter channels. Average-current-mode control improves current sharing between the channels while minimizing component derating and size. Parallel multiple MAX5037A regulators to increase the output current capacity. For maximum ripple rejection at the input, set the phase shift between phases to 90° for two paralleled converters, or 60° for three paralleled converters. The paralleling capability of the MAX5037A improves design flexibility in applications requiring upgrades (higher load). The programmable output voltage utilizes VID codes compliant with Intel's VRM 9.0/VRM 9.1 specifications.

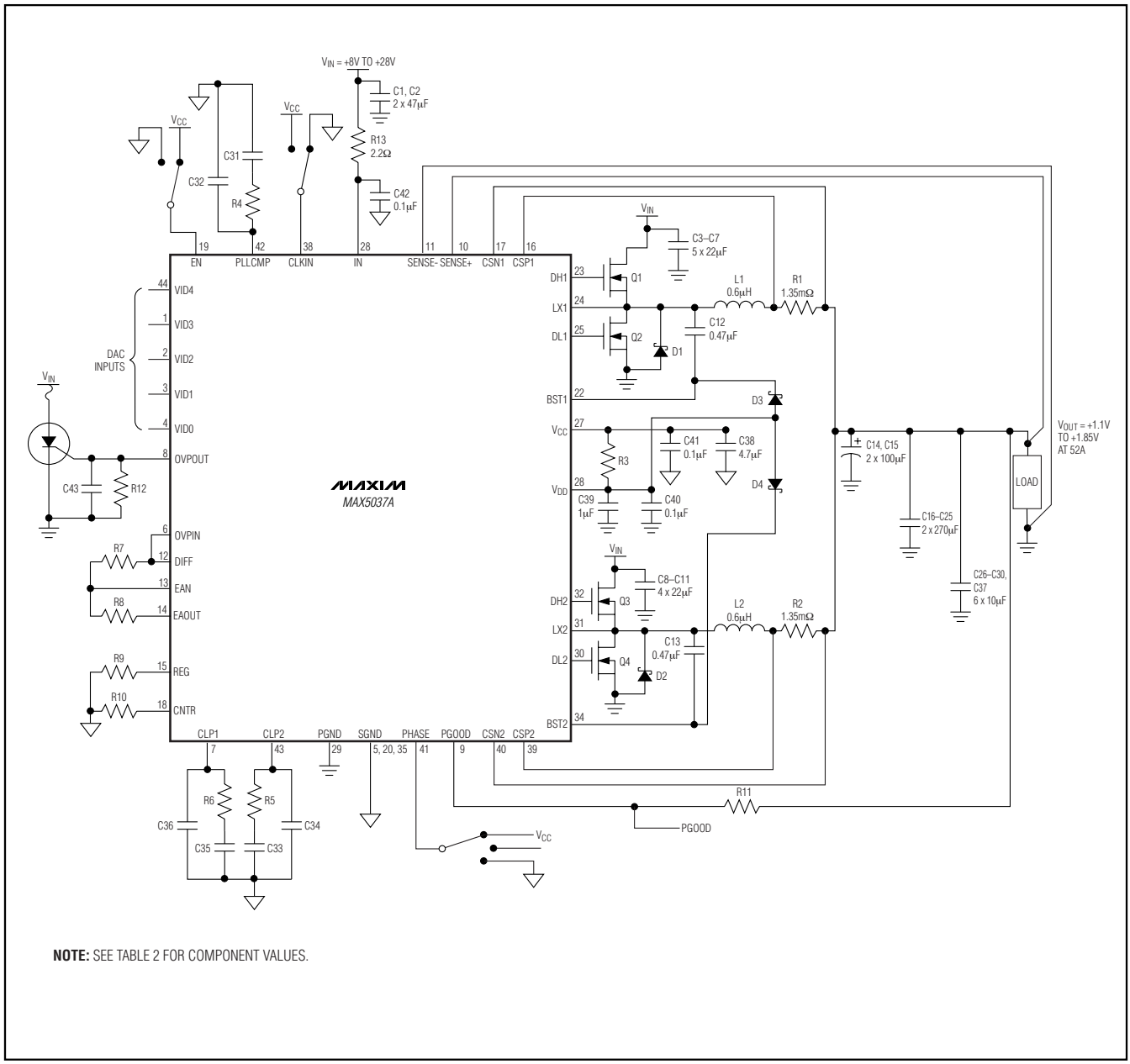


*SEE TABLE 2 FOR COMPONENT VALUES.

Figure 1. Typical VRM Application Circuit, V_{IN} = +5V

VRM 9.0/VRM 9.1, Dual-Phase, Parallelable, Average-Current-Mode Controller

Dual-phase converters with an out-of-phase locking arrangement reduce the input and output capacitor ripple current, effectively multiplying the switching frequency by the number of phases. Each phase of the MAX5037A consists of an inner average current loop controlled by a common outer-loop voltage-error amplifier (VEA). The combined action of the two inner current loops and the output voltage loop corrects the output voltage errors and forces the phase currents to be equal.



NOTE: SEE TABLE 2 FOR COMPONENT VALUES.

Figure 2. Typical VRM Application Circuit, V_{IN} = +8V to +28V

V_{IN}, V_{CC}, and V_{DD}

The MAX5037A accepts an input voltage range of +4.75V to +5.5V or +8V to +28V. All internal control circuitry operates from an internally regulated nominal voltage of 5V. For input voltages of +8V or greater, the internal V_{CC} regulator steps the voltage down to +5V. The V_{CC} output voltage is a regulated 5V output capable of sourcing up to 80mA. Bypass V_{CC} to SGND with 4.7µF and 0.1µF low-ESR ceramic capacitors in parallel for high-frequency noise rejection and stable operation (Figure 1).

V_{CC} powers all internal circuitry. V_{DD} is derived externally from V_{CC} and provides power to the high-side and low-side MOSFET drivers. V_{DD} is internally connected to the power source of the low-side MOSFET drivers. Use V_{DD} to charge the boost capacitors that provide power to the high-side MOSFET drivers. Connect the V_{CC} regulator output to V_{DD} through an R-C lowpass filter. Use a 1Ω (R3) resistor and a parallel combination of 1µF and 0.1µF ceramic capacitors to filter out the high peak currents of the MOSFET drivers from the sensitive internal circuitry.

Calculate power dissipation in the MAX5037A as a product of the input voltage and the total V_{CC} regulator output current (I_{CC}). I_{CC} includes quiescent current (I_Q) and gate drive current (I_{DD}):

$$P_D = V_{IN} \times I_{CC} \quad (1)$$

$$I_{CC} = I_Q + f_{SW} \times (Q_{G1} + Q_{G2} + Q_{G3} + Q_{G4}) \quad (2)$$

where, Q_{G1}, Q_{G2}, Q_{G3}, and Q_{G4} are the total gate charge of the low-side and high-side external MOSFETs, I_Q is 4mA (typ), and f_{SW} is the switching frequency of each individual phase.

For applications utilizing a +5V input voltage, disable the V_{CC} regulator by connecting IN and V_{CC} together.

Undervoltage Lockout (UVLO)/Soft-Start

The MAX5037A includes an undervoltage lockout with hysteresis and a power-on reset circuit for converter turn-on and monotonic rise of the output voltage. The UVLO circuit monitors the V_{CC} regulator output while actively holding down the power-good (PGOOD) output. The UVLO threshold is internally set between +4.0V and +4.5V with a 200mV hysteresis. Hysteresis at UVLO eliminates "chattering" during startup.

Most of the internal circuitry, including the oscillator, turns on when the input voltage reaches +4V. The MAX5037A draws up to 4mA of current before the input voltage reaches the UVLO threshold.

The compensation network at the current-error amplifier, CLP1 and CLP2, provides an inherent soft-start to the VRM power supply. It includes a parallel combination of capacitors (C34, C36) and resistors (R5, R6) in series with other capacitors (C33, C35) (see Figure 1). The voltage at CLP_ limits the maximum current available to charge output capacitors. The capacitor on CLP_ in conjunction with the finite output-drive current of the current-error amplifier yields a finite rise time for the output current and thus the output voltage.

Internal Oscillator

The internal oscillator generates the 180° out-of-phase clock signals required by the pulse-width modulation (PWM) circuits. The oscillator also generates the $2V_{P-P}$ voltage ramp signals necessary for the PWM comparators. Connect CLKIN to SGND to set the internal oscillator frequency to 250kHz or connect CLKIN to V_{CC} to set the internal oscillator to 500kHz.

CLKIN is a CMOS logic clock for the phase-locked loop (PLL). When driven externally, the internal oscillator locks to the signal at CLKIN. A rising edge at CLKIN starts the ON cycle of the PWM. Ensure that the external clock pulse width is at least 200ns. CLKOUT provides a phase-shifted output with respect to the rising edge of the signal at CLKIN. PHASE sets the amount of phase shift at CLKOUT. Connect PHASE to V_{CC} for 120° of phase shift, leave PHASE unconnected for 90° of phase shift, or connect PHASE to SGND for 60° of phase shift with respect to CLKIN.

The MAX5037A requires compensation on PLLCMP even when operating from the internal oscillator. The device requires an active PLL in order to generate the proper clock signal required for PWM operation.

Control Loop

The MAX5037A uses an average-current-mode control scheme to regulate the output voltage (Figure 3). The main control loop consists of an inner current loop and an outer voltage loop. The inner loop controls the output currents (I_{PHASE1} and I_{PHASE2}), while the outer loop controls the output voltage. The inner current loop absorbs the inductor pole reducing the order of the outer voltage loop to that of a single-pole system.

VRM 9.0/VRM 9.1, Dual-Phase, Parallelable, Average-Current-Mode Controller

The current loop consists of a current-sense resistor, R_S (an RC lowpass filter in the case of lossless inductor current sensing), a current-sense amplifier (CA_), a current-error amplifier (CEA_), an oscillator providing the carrier ramp, and a PWM comparator (CPWM_). The precision CA_ amplifies the sense voltage across R_S by a factor of 18. The inverting input to the CEA_ senses the output of the CA_. The output of the CEA_ is the difference between the voltage-error amplifier output (EAOUT) and the amplified voltage from the CA_. The RC compensation network connected to CLP1 and CLP2 provides external frequency compensation for the respective CEA_. The start of every clock cycle enables the high-side drivers and initiates a PWM ON cycle. Comparator CPWM_ compares the output voltage from the CEA_ with a 0 to 2V ramp from the oscillator. The PWM ON cycle terminates when the ramp voltage exceeds the error voltage.

The outer voltage control loop consists of the differential amplifier (DIFF AMP), adaptive voltage-positioning (AVP) block, digital-to-analog converter (DAC), and voltage-error amplifier (VEA). The unity-gain differential amplifier provides true differential remote sensing of the output voltage. The differential amplifier output and the AVP connect to the inverting input (EAN) of the VEA. The noninverting input of VEA is internally connected to the DAC output. The VEA controls the two inner current loops (Figure 3). Use a resistive feedback network to set the gain of the VEA as required by the adaptive voltage-positioning circuit.

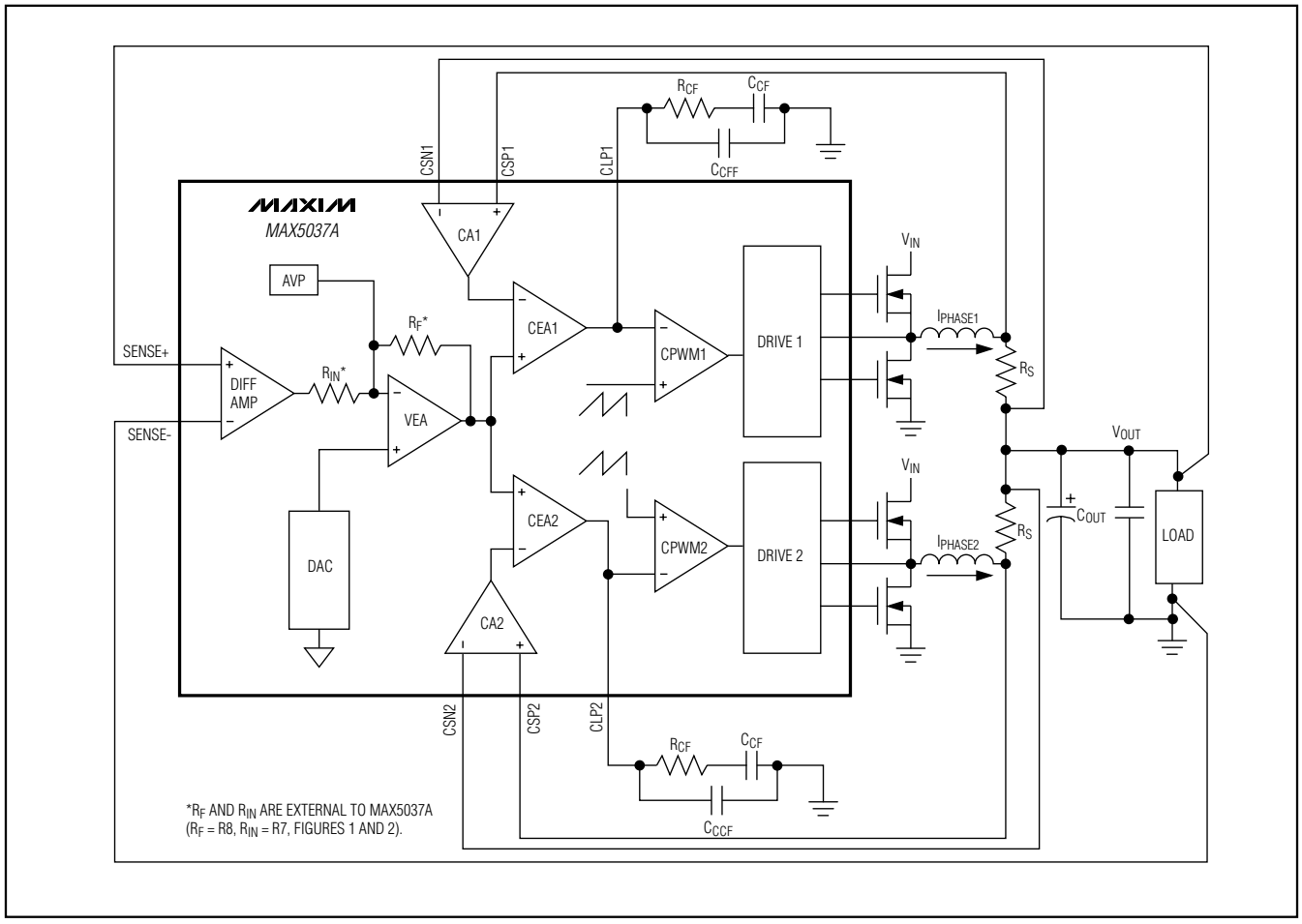


Figure 3. MAX5037A Control Loop

Current-Sense Amplifier

The differential current-sense amplifier (CA_) provides a DC gain of 18. The maximum input offset voltage of the current-sense amplifier is 1mV and the common-mode voltage range is -0.3V to +3.6V. The current-sense amplifier senses the voltage across a current-sense resistor.

Peak-Current Comparator

The peak-current comparator provides a path for fast cycle-by-cycle current limit during extreme fault conditions such as an output inductor malfunction (Figure 4). Note that the average current-limit threshold of 48mV still limits the output current during short-circuit conditions. So to prevent inductor saturation, select an output inductor with a saturation current specification greater than the average current limit. Proper inductor selection ensures that only extreme conditions trip the peak-current comparator, such as a broken output inductor. The 112mV voltage threshold for triggering the peak-current limit is twice the full-scale average current-limit voltage threshold. The peak-current comparator has a delay of only 260ns.

Current-Error Amplifier

Each phase of the MAX5037A has a dedicated transconductance current-error amplifier (CEA_) with a typical g_m of 550µS and 320µA output sink and source current capability. The CEA_ outputs, CLP1 and CLP2, serve as the inverting input to the PWM comparator. CLP1 and CLP2 are externally accessible to provide frequency compensation for the inner current loops (Figure 3). Compensate CEA_ such that the inductor current down slope, which becomes the up slope to the inverting input of the PWM comparator, is less than the slope of the internally generated voltage ramp (see the *Compensation* section).

PWM Comparator and R-S Flip-Flop

The PWM comparator (CPWM) sets the duty cycle for each cycle by comparing the current-error amplifier output to a $2V_{P-P}$ ramp. At the start of each clock cycle, an R-S flip-flop resets and the high-side driver (DH_) turns on. The comparator sets the flip-flop as soon as the ramp voltage exceeds the CLP_ voltage, thus terminating the ON cycle (Figure 4).

Differential Amplifier

The unity-gain differential amplifier (DIFF AMP) facilitates the output voltage remote sensing at the load (Figure 3). It provides true differential output voltage sensing while rejecting the common-mode voltage errors due to high-current ground paths. Sensing the output voltage directly at the load provides accurate load voltage sensing in high-current environments. The VEA provides the difference between the differential amplifier output (DIFF) and the desired VID programmed output voltage. The differential amplifier has a unity-gain bandwidth of 3MHz. The difference between SENSE+ and SENSE- regulates to the programmed VID output voltage.

Connect SENSE+ to an external resistor-divider network at the output voltage to use the MAX5037A for output voltages higher than those allowed by the VID codes.

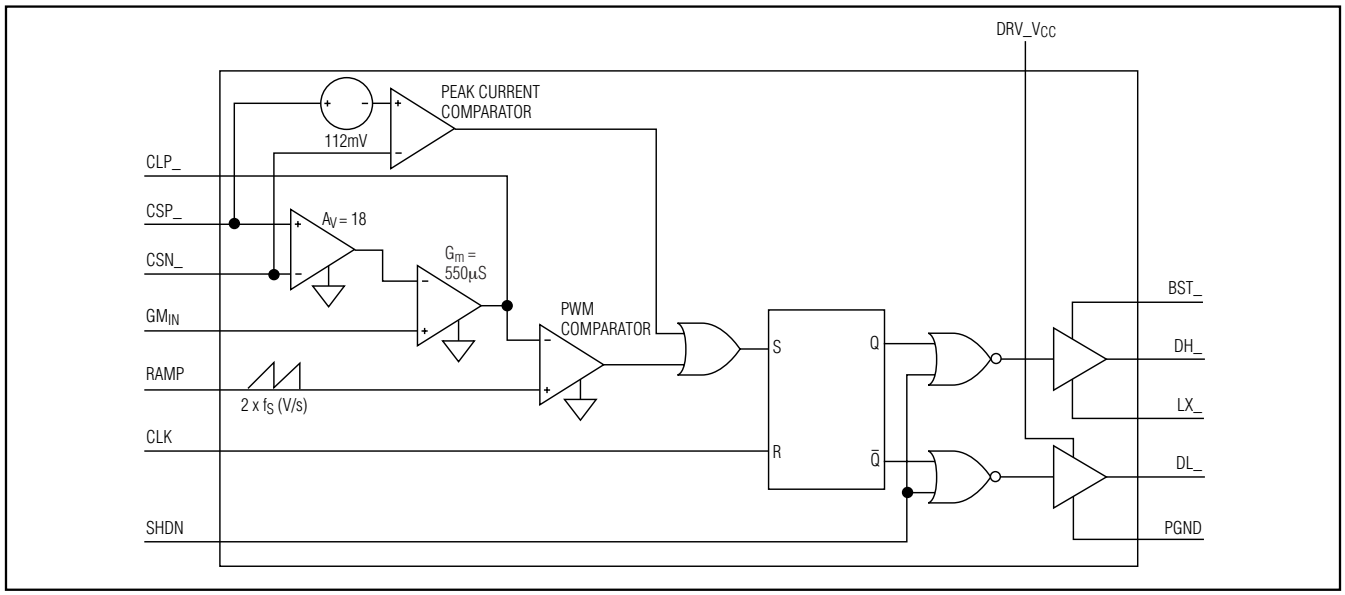


Figure 4. Phase Circuit (Phase 1/Phase 2)

VRM 9.0/VRM 9.1, Dual-Phase, Parallelable, Average-Current-Mode Controller

Voltage-Error Amplifier

The VEA sets the gain of the voltage control loop. The VEA determines the error between the differential amplifier output and the reference voltage generated from the DAC.

The VEA output clamps to 0.9V relative to V_{CM} (0.6V), thus limiting the average maximum current from individual phases. The maximum average current-limit threshold for each phase is equal to the maximum clamp voltage of the VEA divided by the gain (18) of the current-sense amplifier. This results in accurate settings for the average maximum current for each phase. Set the VEA gain using R_F and R_{IN} for the amount of output voltage positioning required within the rated current range as discussed in the *Adaptive Voltage Positioning* section (Figure 3).

Adaptive Voltage Positioning

Powering new generation processors requires new techniques to reduce cost, size, and power dissipation. Voltage positioning reduces the total number of output capacitors to meet a given transient response requirement. Setting the no-load output voltage slightly higher than the output voltage during nominally loaded conditions allows a larger downward voltage excursion when the output current suddenly increases. Regulating at a lower output voltage under a heavy load allows a larger upward voltage excursion when the output current suddenly decreases. A larger allowed voltage step excursion reduces the required number of output capacitors or allows for the use of higher ESR capacitors.

Voltage positioning and the ability to operate with the multiple reference voltages may require the output to regulate away from a center value. Define the center value as the voltage where the output equals the VID reference voltage at one half the maximum output current (Figure 5).

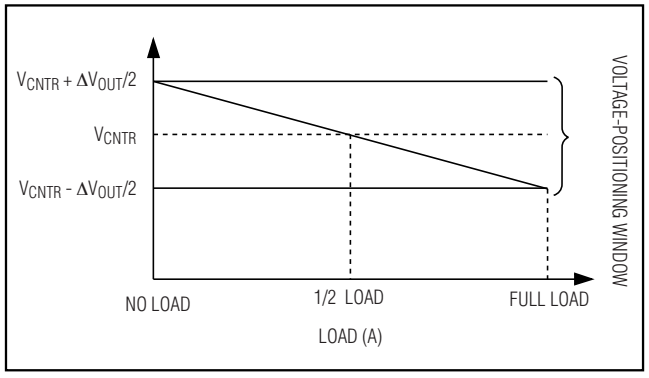


Figure 5. Defining the Voltage-Positioning Window

Set the voltage-positioning window (ΔV_{OUT}) using the resistive feedback of the VEA. See the *Adaptive Voltage-Positioning Design Procedure* section and use the following equation to calculate the voltage-positioning window:

$$\Delta V_{OUT} = I_{OUT} \times R_{IN} / (2 \times G_C \times R_F) \quad (3)$$

$$G_C = \frac{0.05}{R_S} \quad (4)$$

where R_{IN} and R_F are the input and feedback resistors of the VEA, G_C is the current-loop transconductance, and R_S is the current-sense resistor or, if using lossless inductor current sensing, the DC resistance of the inductor.

The voltage at CNTR (V_{CNTR}) regulates to 1.2V (Figure 6). The current set by the resistor R_{CNTR} is mirrored at the inverting input of the VEA, centering the output voltage-positioning window on the VID programmed output voltage. Set the center of the output voltage with a resistor from CNTR to SGND in the following manner:

$$R_{CNTR} = \frac{V_{CNTR} \times R_{IN}}{I_{OUT}\left(\frac{R_{IN}}{2R_F G_C}\right) + (V_{OUT} - VID)} \quad (5)$$

where V_{OUT} is a required value of output voltage at the corresponding I_{OUT}. I_{OUT} can be any value from no load to full load.

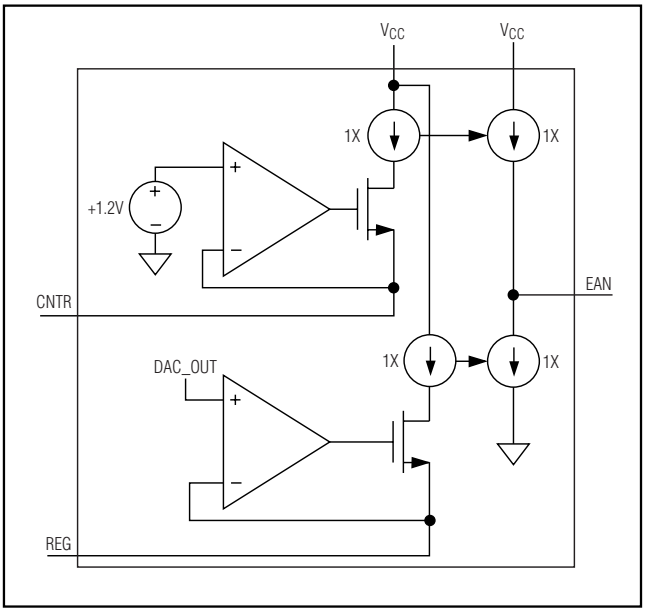


Figure 6. Adaptive Voltage-Positioning Circuit

Applying the voltage-positioning window at different VRM voltage settings requires that $R_{REG} = R_F$. The voltage on REG internally regulates to the programmed VID output voltage. Choose R_{REG} to limit the current at REG to 50µA. For example, for a VID setting of 1.85V, calculate the minimum allowed R_{REG} as R_{REG} = 1.85V/50µA = 37kΩ. To use larger values of R_{REG} while maintaining the required gain of the VEA, use larger values for R_{IN}.

In the case of a VID voltage setting equal to $V_{COREMAX}$ at I_{OUT} = 0 (no load), $R_{CNTR} = \infty$ from the above equation (Figure 7). For systems requiring $V_{COREMAX}$ as an absolute maximum voltage when I_{OUT} = 0 (no load), calculate R_{REG} using following the equation:

$$R_{REG} = \frac{R_{IN} \times R_F}{R_{IN} + R_F\left(1 - \frac{V_{COREMAX}}{VID}\right)} \quad (6)$$

DAC Inputs (VID0–VID4)

The DAC programs the output voltage. The DAC typically receives a digital code, alternatively, the VID inputs are hardwired to SGND or left open circuit. VID0–VID4 logic can be changed while the MAX5037A is active, initiating a transition to a new output voltage level. Change VID0–VID4 together, avoiding greater than 1µs skew between bits. Otherwise, incorrect DAC readings may cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. For any low-going VID step of 100mV or more, the OVP can trip because the OVP trip reference changes instantaneously with the VID code, but the converter output does not follow immediately. The converter output drops at a rate depending on the output capacitor, inductor load, and the closed-loop bandwidth of the converter. Do not exceed a maximum VID step size of 75mV.

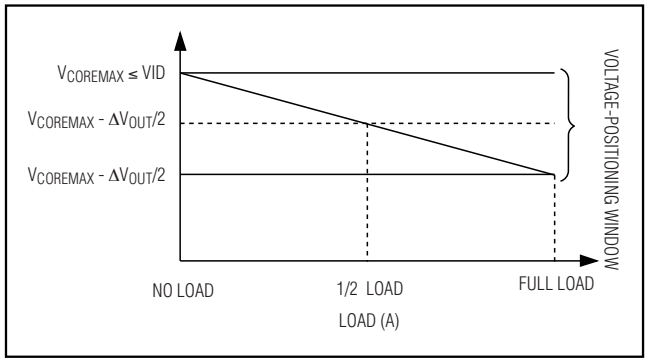


Figure 7. Limiting the Voltage-Positioning Window

The available DAC codes and resulting output voltages (Table 1) comply with Intel's VRM 9.0 specification. Internal pullup resistors connect the VID inputs to a nominal internal 3V supply. Force the VID inputs below 0.8V for logic low or leave unconnected for logic high. Output voltage accuracy with respect to the programmed VID voltage is ±0.8% over the -40°C to +85°C temperature range.

Table 1. Output Voltage vs. DAC Codes

VID INPUTS (0 = CONNECTED TO SGND, 1 = OPEN CIRCUIT)					OUTPUT VOLTAGE (V)
VID4	VID3	VID2	VID1	VID0	V_{OUT}
1	1	1	1	1	Output off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

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Phase-Locked Loop: Operation and Compensation

The phase-locked loop (PLL) synchronizes the internal oscillator to the external frequency source when driving CLKIN. Connecting CLKIN to V_{CC} or SGND forces the PWM frequency to default to the internal oscillator frequency of 500kHz or 250kHz, respectively. The PLL uses a conventional architecture consisting of a phase detector and a charge pump capable of providing 20µA of output current. Connect an external series combination capacitor (C31) and resistor (R4) and a parallel capacitor (C32) from PLLCMP to SGND to provide frequency compensation for the PLL (Figure 1). The pole-zero pair compensation provides a zero at f_Z defined by 1 / [R4 x (C31 + C32)] and a pole at f_P defined by 1 / (R4 x C32). Use the following typical values for compensating the PLL: R4 = 7.5kΩ, C31 = 4.7nF, C32 = 470pF. When changing the PLL frequency, expect a finite locking time of approximately 200µs.

The MAX5037A requires compensation on PLLCMP even when operating from the internal oscillator. The device requires an active-phase-locked loop in order to generate the proper internally shifted clock available at CLKOUT.

MOSFET Gate Drivers (DH_, DL_)

The high-side (DH_) and low-side (DL_) drivers drive the gates of external N-channel MOSFETs (Figure 1). The drivers' high-peak sink and source current capability provides ample drive for the fast rise and fall times of the switching MOSFETs. Faster rise and fall times result in reduced cross-conduction losses. For modern CPU applications where the duty cycle is less than 50%, choose high-side MOSFETs (Q1 and Q3) with a moderate $R_{DS(ON)}$ and very low gate charge. Choose low-side MOSFETs (Q2 and Q4) with very low $R_{DS(ON)}$ and moderate gate charge.

The driver block also includes a logic circuit that provides an adaptive nonoverlap time to prevent shoot-through currents during transition. The typical nonoverlap time is 60ns between the high-side and low-side MOSFETs.

BST_

V_{DD} powers the low- and high-side MOSFET drivers. The high-side drivers derive their power through a bootstrap capacitor and V_{DD} supplies power internally to the low-side drivers. Connect a 0.47µF low-ESR ceramic capacitor between BST_ and LX_. Bypass V_{DD} to PGND with 1µF and 0.1µF low-ESR ceramic capacitors. Reduce the PC board area formed by these capacitors, the rectifier diodes between V_{DD} and the boost capacitor, the MAX5037A, and the switching MOSFETs.

Protection

The MAX5037A includes output overvoltage protection (OVP), undervoltage protection (UVP), phase failure, and overload protection to prevent damage to the powered electronic circuits.

Overvoltage Protection (OVP)

The OVP comparator compares the OVPIN input to the overvoltage threshold. The overvoltage threshold is typically +13% above the programmed VID output voltage. A detected overvoltage event latches the comparator output forcing the power stage into the OVP state. In the OVP state, the high-side MOSFETs turn off and the low-side MOSFETs latch on. Use the OVPOUT high-current-output driver to turn on an external crowbar SCR. When the crowbar SCR turns on, a fuse must blow or the source current for the MAX5037A regulator must be limited to prevent further damage to the external circuitry. Connect the SCR close to the input source and after the fuse. Use an SCR large enough to handle the peak I^2t energy due to the input and output capacitors discharging and the current sourced by the power source output. Connect DIFF to OVPIN for differential output sensing and overvoltage protection. Add an RC delay to reduce the sensitivity of overvoltage circuit and avoid nuisance tripping of the converter (Figure 8).

For any low-going VID step of 75mV or more, the OVP can trip because the OVP trip reference changes instantaneously with the VID code, but the converter output does not follow immediately. The converter output drops at a rate depending on the output capacitor, inductor load, and the closed-loop bandwidth of the converter.

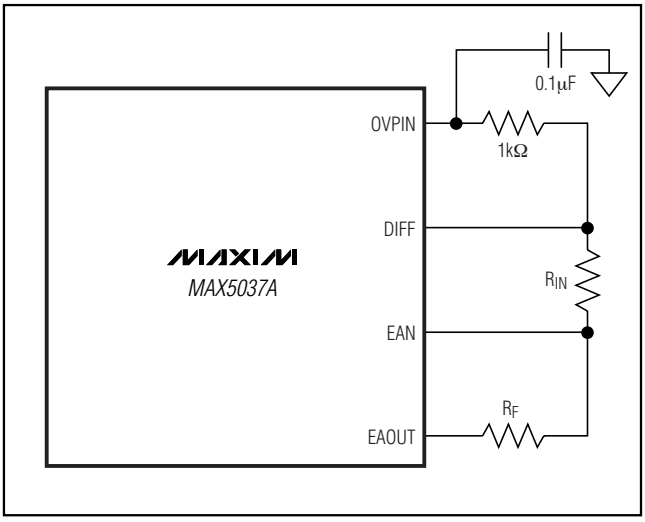

Figure 8. OVP Input Delay

Power-Good Generator (PGOOD)

The PGOOD output is high if all of the following conditions are met (Figure 9):

1) The output is within 90% to 108% of the programmed output voltage.
2) Both phases are providing current.
3) EN is HIGH.

A window comparator compares the differential amplifier output (DIFF) against 1.08 times the programmed VID output voltage for overvoltage and 0.90 times the programmed VID output voltage for undervoltage monitoring. The phase failure comparator detects a phase failure by comparing the current-error amplifier output (CLP_) with a 2.0V reference.

Use a 10kΩ pullup resistor from PGOOD to a voltage source less than or equal to V_{CC}. An output voltage outside the comparator window or a phase failure condition forces the open-drain output low. The open-drain MOSFET sinks 4mA of current while maintaining less than 0.2V at the PGOOD output.

Phase Failure Detector

Output current contributions from the two phases are within ±10% of each other. Proper current sharing reduces the necessity to overcompensate the external components. However, an undetected failure of one phase driver causes the other phase driver to run continuously as it tries to provide the entire current requirement to the load. Eventually, the stressed operational phase driver fails.

During normal operating conditions, the voltage level on CLP_ is within the peak-to-peak voltage levels of the PWM ramp. If one of the phases fails, the control loop raises the CLP_ voltage above its operating range. To determine a phase failure, the phase failure detection circuit (Figure 9) monitors the output of the current amplifiers (CLP1 and CLP2) and compares them to a 2.0V reference. If the voltage levels on CLP1 or CLP2 are above the reference level for more than 1250 clock cycles, the phase failure circuit forces PGOOD low.

Overload Conditions

Average current-mode control has the ability to limit the average current sourced by the converter during a fault condition. When a fault condition occurs, the VEA output clamps to 0.9V with respect to the common-mode voltage (V_{CM} = 0.6V) and is compared with the output of the current-sense amplifiers (CA1 and CA2) (see Figure 3). The current-sense amplifier's gain of 18 limits the maximum current in the inductor or sense resistor to $I_{LIMIT} = 50mV/R_S$.

Parallel Operation

For applications requiring large output current, parallel up to three MAX5037As (six phases) to triple the available output current. The paralleled converters operating at the same switching frequency but different phases keep the capacitor ripple RMS currents to a minimum. Three parallel MAX5037A converters deliver up to 180A of output current. To set the phase shift of the on-board PLL, leave PHASE unconnected for 90° of phase shift (two paralleled converters), or connect PHASE to SGND for 60° of phase shift (three converters in parallel). Designate one converter as master and the remaining converters as slaves. Connect the master and slave controllers in a daisy-chain configuration as shown in Figure 10. Connect CLKOUT from the master controller to CLKIN of the first slaved controller, and CLKOUT from the first slaved controller to CLKIN of the second slaved controller. Choose the appropriate phase shift for minimum ripple currents at the input and output capacitors. The master controller senses the output differential voltage through SENSE+ and SENSE- and generates the DIFF voltage. Disable the voltage sensing of the slaved controllers by leaving DIFF unconnected (floating). Figure 11 shows a detailed typical parallel application circuit using two MAX5037As. This circuit provides four phases at an input voltage of 12V and an output voltage range of 1.1V to 1.85V at 104A.

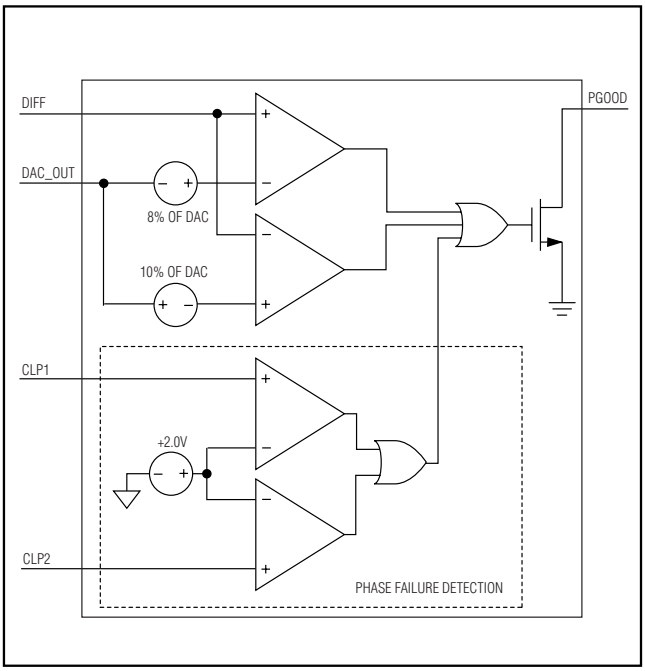

Figure 9. Power-Good Generator

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Applications Information

Each MAX5037A circuit drives two 180° out-of-phase channels. Parallel two or three MAX5037A circuits to achieve four- or six-phase operation, respectively. Figure 1 shows the typical application circuit for two-phase operation. The design criteria for a two-phase converter includes frequency selection, inductor value, input/output capacitance, switching MOSFETs, sense resistors, and the compensation network. Follow the same procedure for the four- and six-phase converter design, except for the input and output capacitance. The input and output capacitance requirement varies depending on the operating duty cycle.

The examples discussed in this data sheet pertain to a typical VRM application with the following specifications:

V_{IN} = +12V

V_{OUT} = +1.1V to +1.85V

$I_{OUT(MAX)}$ = 52A

$V_{COREMAX}$ = VID Programmed Output Voltage at No Load

AVP (ΔV_{OUT}) = 120mV

f_{SW} = 250kHz

Peak-to-Peak Inductor Current (ΔI_L) = 10A

Table 2 shows a list of recommended external components (Figure 1) and Table 3 provides component supplier information.

Table 2. Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2	2	47µF, 16V X5R input-filter capacitors, TDK C5750X5R1C476M
C3–C11	9	22µF, 16V input-filter capacitors, TDK C4532X5R1C226M
C12, C13	2	0.47µF, 16V capacitors, TDK C1608X5R1A474K
C14, C15	2	100µF, 6.3V output-filter capacitors, Murata GRM44-1X5R107K6.3
C16–C25	10	270µF, 2V output-filter capacitors, Panasonic EEFUE0D271R
C26–C30, C37	6	10µF, 6.3V output-filter capacitors, TDK C2012X5R0J106M
C31	1	4700pF, 16V X7R capacitor, Vishay-Siliconix VJ0603Y471JXJ
C32, C34, C36	3	470pF, 16V capacitors, Murata GRM1885C1H471JAB01
C33, C35, C43	3	0.01µF, 50V X7R capacitors, Murata GRM188R71H103KA01
C38	1	4.7µF, 16V X5R capacitor, Murata GRM40-034X5R475k6.3
C39	1	1.0µF, 10V Y5V capacitor, Murata GRM188F51A105
C40, C41, C42	3	0.1µF, 16V X7R capacitors, Murata GRM188R71C104KA01
D1, D2	2	Schottky diodes, ON-Semiconductor MBRS340T3
D3, D4	2	Schottky diodes, ON-Semiconductor MBR0520LT1
L1, L2	2	0.6µH, 27A inductors, Panasonic ETQP1H0R6BFX
Q1, Q3	2	Upper power MOSFETs, Vishay-Siliconix Si7860DP
Q2, Q4	2	Lower power MOSFETs, Vishay-Siliconix Si7886DP
R1, R2	4	Current-sense resistors, use two 2.70mΩ resistors in parallel, Panasonic ERJM1WSF2M7U
R3, R13	1	2.2Ω ±1% resistor
R4	1	7.5kΩ ±1% resistor
R5, R6	2	1kΩ ±1% resistors
R7	1	4.99kΩ ±1% resistor
R8, R9	2	37.4kΩ ±1% resistors
R11	1	10kΩ ±1% resistor
R12	1	10Ω ±1% resistor

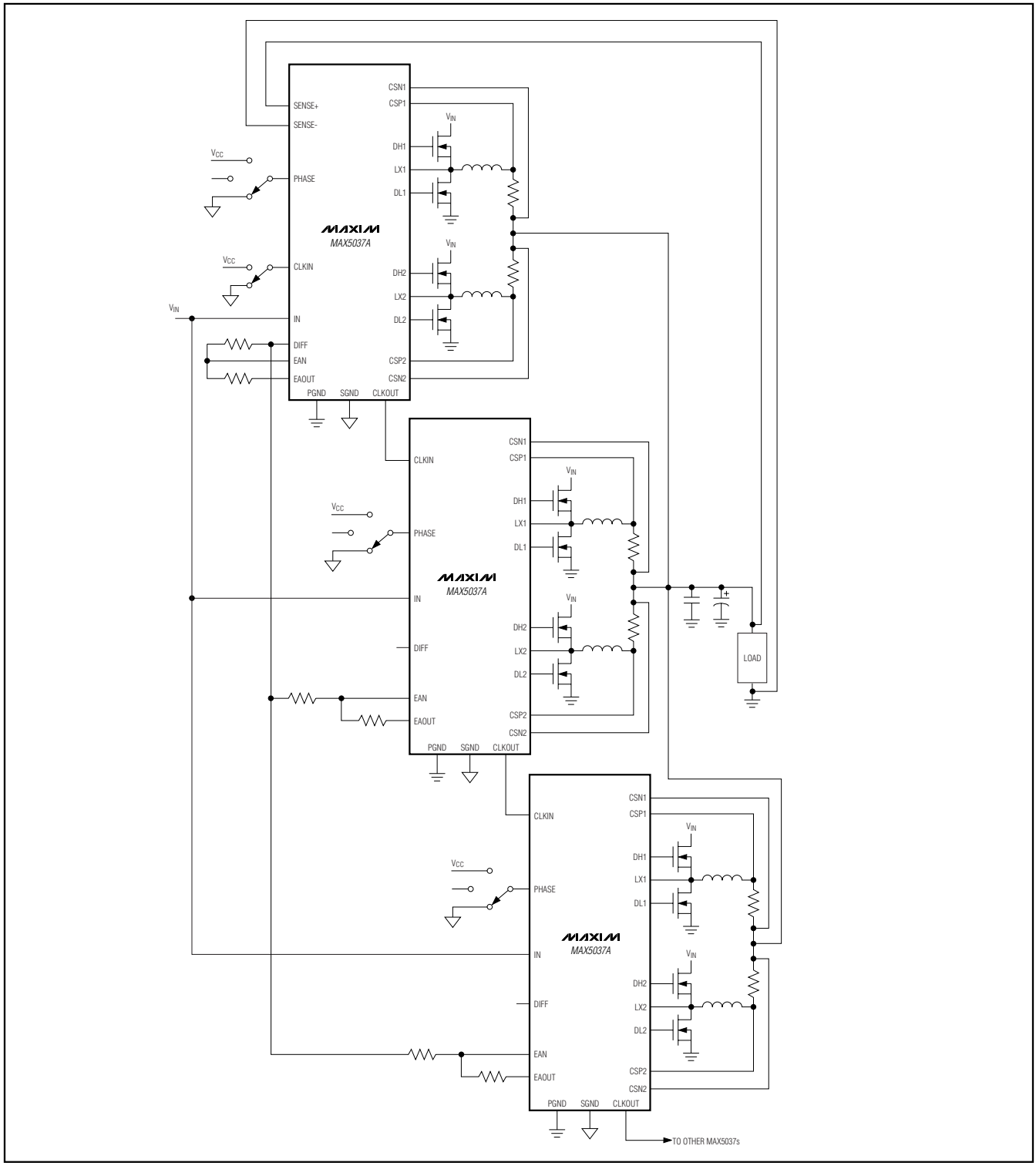

Figure 10. Parallel Configuration of Multiple MAX5037As

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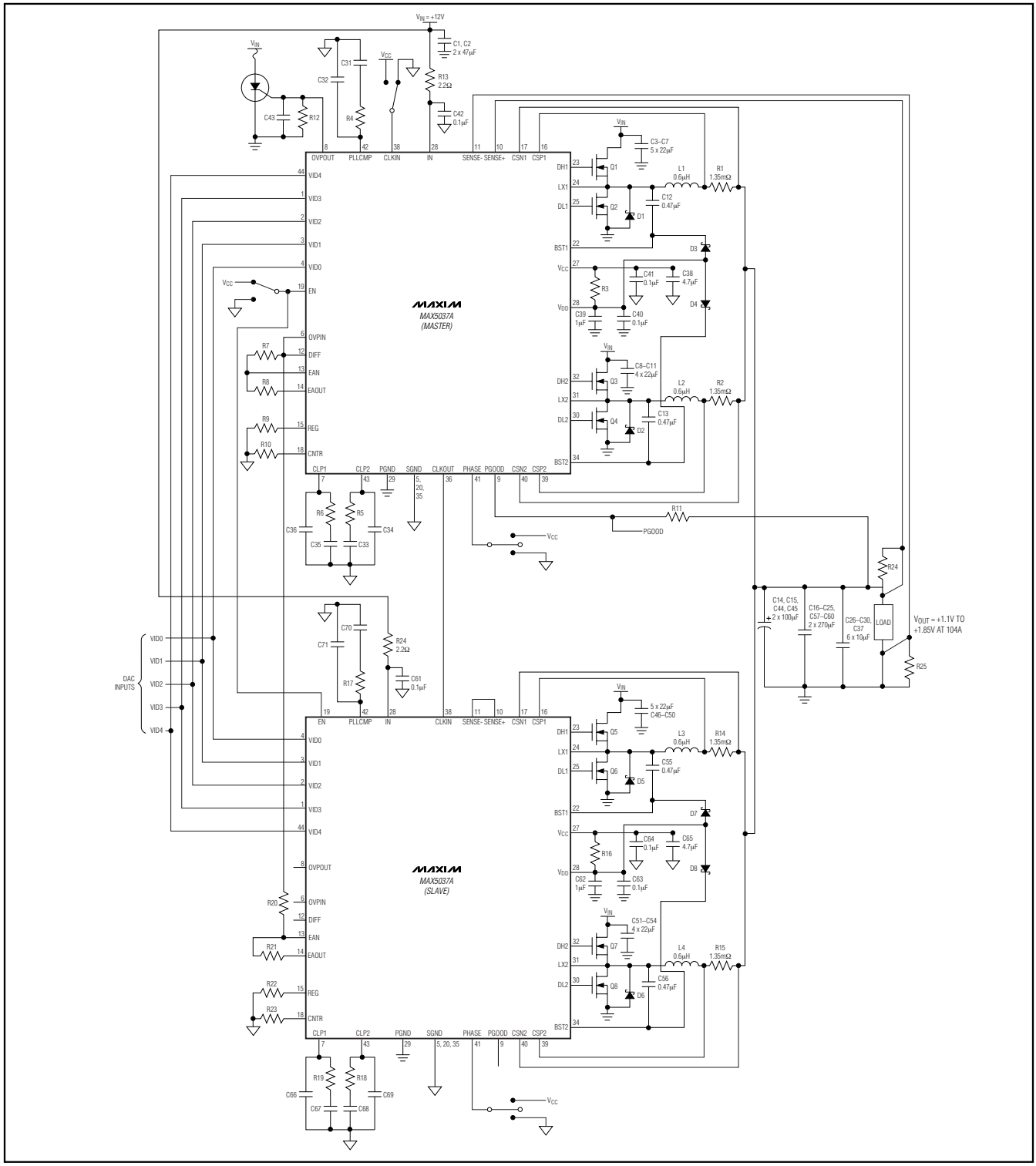

Figure 11. Four-Phase Parallel Application Circuit (V_{IN} = +12V, V_{OUT} = +1.1V to +1.85V at 104A)

Table 3. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Murata	770-436-1300	770-436-3030	www.murata.com
ON Semiconductor	602-244-6600	602-244-3345	www.on-semi.com
Panasonic	714-373-7939	714-373-7183	www.panasonic.com
TDK	847-803-6100	847-390-4405	www.tcs.tdk.com
Vishay-Siliconix	1-800-551-6933	619-474-8920	www.vishay.com

Number of Phases

Selecting the number of phases for a voltage regulator depends mainly on the ratio of input-to-output voltage (operating duty cycle). Optimum output-ripple cancellation depends on the right combination of operating duty cycle and the number of phases. Use the following equation as a starting point to choose the number of phases:

$$N_{PH} \approx K/D \quad (7)$$

where K = 1, 2, or 3 and the duty cycle $D = V_{OUT}/V_{IN}$.

Choose K to make N_{PH} an integer number. For example, converting V_{IN} = +12V to V_{OUT} = +1.75V yields better ripple cancellation in the six-phase converter than in the four-phase converter. Ensure that the output load justifies the greater number of components for multiphase conversion. Generally, limiting the maximum output current to 25A per phase yields the most cost-effective solution. The maximum ripple cancellation occurs when $N_{PH} = K/D$.

Single-phase conversion requires greater size and power dissipation for external components such as the switching MOSFETs and the inductor. Multiphase conversion eliminates the heatsink by distributing the power dissipation in the external components. The multiple phases operating at given phase shifts effectively increase the switching frequency seen by the input/output capacitors, reducing the input/output capacitance requirement for the same ripple performance. The lower inductance value improves the large-signal response of the converter during a transient load at the output. Consider all these issues when determining the number of phases necessary for the voltage regulator application.

Adaptive Voltage-Positioning Design Procedure

The following steps outline the procedure for setting the adaptive voltage positioning:

1) Choose the voltage-error amplifier input (EAN) resistor $R_{IN} > 5k\Omega$.
2) Determine a reasonable amount of excursion from the desired output voltage that the system can tolerate and use as an estimate for the voltage-positioning window, ΔV_{OUT} (see Figures 5 and 7).
3) Calculate R_F from equations 22 and 23. Use equation 3 to verify that ΔV_{OUT} remains within tolerable limits.
4) Calculate the centering resistor, R_{CNTR}, from equation 5. R_{CNTR} sets the center of the adaptive voltage positioning such that at 1/2 full-load current, the output voltage is the desired VID programmed output voltage (Figure 5). Do not use values less than 24kΩ for R_{CNTR}.
5) Choose the regulation resistor, R_{REG}, to have the same value as the feedback resistor, R_F ($R_{REG} = R_F$). R_{REG} maintains the adaptive voltage-positioning window at all VID output voltage settings. Do not use values less than 37kΩ for R_{REG}.

Inductor Selection

The switching frequency per phase, peak-to-peak ripple current in each phase, and allowable ripple at the output determine the inductance value.

Selecting higher switching frequencies reduces the inductance requirement, but at the cost of lower efficiency. The charge/discharge cycle of the gate and drain capacitances in the switching MOSFETs create switching losses. The situation worsens at higher input voltages, since switching losses are proportional to the square of input voltage. Use 500kHz per phase for V_{IN} = +5V, 250kHz or less per phase for $V_{IN} \geq$ +12V.

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Although lower switching frequencies per phase increase the peak-to-peak inductor ripple current (ΔI_L), the ripple cancellation in the multiphase topology reduces the RMS ripple current of the input and output capacitor.

Use the following equation to determine the minimum inductance value:

$$L_{MIN} = \frac{(V_{INMAX} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times \Delta I_L} \quad (8)$$

Choose ΔI_L equal to about 40% of the output current per phase. Since ΔI_L affects the output ripple voltage, the inductance value may need minor adjustment after choosing the output capacitors for full-rated efficiency.

Choose inductors from the standard high-current, surface-mount inductor series available from various manufacturers. Particular applications may require custom-made inductors. Use high-frequency core material for custom inductors. High ΔI_L causes large peak-to-peak flux excursion increasing the core losses at higher frequencies. The high-frequency operation coupled with high ΔI_L, reduces the required minimum inductance making possible even the use of planar inductors. The advantages of using planar magnetics include low-profile design, excellent current sharing between phases due to the tight control of parasitics, and low cost.

For example, calculate the minimum inductance at $V_{IN(MAX)}$ = +13.2V, V_{OUT} = +1.75V, ΔI_L = 10A, and f_{SW} = 250kHz:

$$L_{MIN} = \frac{(13.2 - 1.75) \times 1.75}{13.2 \times 250k \times 10} = 0.6\mu H \quad (9)$$

The MAX5037A average current-mode control feature limits the maximum peak-inductor current and prevents the inductor from saturating. Choose an inductor with a saturating current greater than the worst-case peak inductor current. Use the following equation to determine the worst-case inductor current for each phase:

$$I_{L\_PEAK} = \frac{0.051}{R_{SENSE}} + \frac{\Delta I_L}{2} \quad (10)$$

where R_{SENSE} is the sense resistor in each phase.

Switching MOSFETs

When choosing a MOSFET for voltage regulators, consider the total gate charge, $R_{DS(ON)}$, power dissipation, and package thermal impedance. The product of the gate charge and on-resistance of the MOSFET is a figure of merit, with a lower number signifying better performance. Choose MOSFETs optimized for high-frequency switching applications.

The average current from the MAX5037A gate-drive output is proportional to the total capacitance it drives from DH1, DH2, DL1, and DL2. The power dissipated in the MAX5037A is proportional to the input voltage and the average drive current. See the *V_{IN}, V_{CC}, and V_{DD}* section to determine the maximum total gate charge allowed from all the driver outputs combined.

The gate charge and drain capacitance (CV^2) loss, the cross-conduction loss in the upper MOSFET due to finite rise/fall time, and the I^2R loss due to RMS current in the MOSFET $R_{DS(ON)}$ account for the total losses in the MOSFET. Estimate the power loss ($PD_{MOS\_}$) in the high-side and low-side MOSFETs using the following equations:

$$PD_{MOS-HI} = (Q_G \times V_{DD} \times f_{SW}) + \left(\frac{V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}}{4}\right) + 1.4R_{DS(ON)} \times I^2_{RMS-HI} \quad (11)$$

where Q_G, $R_{DS(ON)}$, t_R, and t_F are the upper switching MOSFET's total gate charge, on-resistance at +25°C, rise time, and fall time, respectively:

$$I_{RMS-HI} = \sqrt{\left(I^2_{DC} + I^2_{PK} + I_{DC} \times I_{PK}\right) \times \frac{D}{3}} \quad (12)$$

where $D = V_{OUT}/V_{IN}$, $I_{DC} = (I_{OUT} - \Delta I_L)/2$ and $I_{PK} = (I_{OUT} + \Delta I_L)/2$.

$$PD_{MOS-LO} = (Q_G \times V_{DD} \times f_{SW}) + \left(\frac{2 \times C_{OSS} \times V_{IN}{}^2 \times f_{SW}}{3}\right) + 1.4R_{DS(ON)} \times I^2_{RMS-LO} \quad (13)$$

$$I_{RMS-LO} = \sqrt{\left(I^2_{DC} + I^2_{PK} + I_{DC} \times I_{PK}\right) \times \frac{(1-D)}{3}} \quad (14)$$

where C_{OSS} is the MOSFET drain-to-source capacitance.

For example, from the typical VRM specifications in the *Applications Information* section with V_{OUT} = +1.75V, the high-side and low-side MOSFET RMS currents are 9.9A and 24.1A, respectively. Ensure that the thermal impedance of the MOSFET package keeps the junction temperature at least +25°C below the absolute maximum rating. Use the following equation to calculate maximum junction temperature:

$$T_J = PD_{MOS} \times \theta_{J-A} + T_A \quad (15)$$

Input Capacitors

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflected back to the source dictate the capacitance requirement. Increasing the number of phases increases the effective switching frequency and lowers the peak-to-average current ratio, yielding a lower input capacitance requirement.

The input ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contributions from the ESR and capacitor discharge are equal to 30% and 70%, respectively. Calculate the input capacitance and ESR required for a specified ripple using the following equations:

$$ESR_{IN} = \frac{(\Delta V_{ESR})}{\left(\frac{I_{OUT}}{N} + \frac{\Delta I_L}{2}\right)} \quad (16)$$

$$C_{IN} = \frac{\frac{I_{OUT}}{N} \times D(1-D)}{\Delta V_Q \times f_{SW}} \quad (17)$$

where I_{OUT} is the total output current of the multiphase converter and N is the number of phases.

For example, at V_{OUT} = 1.75V, the ESR and input capacitance are calculated for the input peak-to-peak ripple of 100mV or less yielding an ESR and capacitance value of 1mΩ and 200µF.

Output Capacitors

The worst-case peak-to-peak and capacitor RMS ripple current, the allowable peak-to-peak output ripple voltage, and the maximum deviation of the output voltage during step loads determine the capacitance and the ESR requirements for the output capacitors.

In multiphase converter design, the ripple currents from the individual phases cancel each other and lower the ripple current. The degree of ripple cancellation depends on the operating duty cycle and the number of phases. Choose the right equation from Table 4 to calculate the peak-to-peak output ripple for a given duty cycle of two-, four-, and six-phase converters. The maximum ripple cancellation occurs when N_{PH} = K / D.

The allowable deviation of the output voltage during the fast-transient load dictates the output capacitance and ESR. The output capacitors supply the load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter. The resistive drop across the capacitor ESR and capacitor discharge causes a voltage drop during a step load. Use a combination of SP polymer and ceramic capacitors for better transient load and ripple/noise performance.

Table 4. Peak-to-Peak Output Ripple Current Calculations

NO. OF PHASES (N)	DUTY CYCLE (D) (%)	EQUATION FOR ΔI_{P-P}
2	< 50	$\Delta I = \frac{V_O(1-2D)}{L \times f_{SW}}$
2	> 50	$\Delta I = \frac{(V_{IN}-V_O)(2D-1)}{L \times f_{SW}}$
4	0 to 25	$\Delta I = \frac{V_O(1-4D)}{L \times f_{SW}}$
4	25 to 50	$\Delta I = \frac{V_O(1-2D)(4D-1)}{2 \times D \times L \times f_{SW}}$
4	> 50	$\Delta I = \frac{V_O(2D-1)(3-4D)}{D \times L \times f_{SW}}$
6	< 17	$\Delta I = \frac{V_O(1-6D)}{L \times f_{SW}}$

VRM 9.0/VRM 9.1, Dual-Phase, Parallelable, Average-Current-Mode Controller

Keep the maximum output voltage deviation less than or equal to the adaptive voltage-positioning window (ΔV_{OUT}). Assume 50% contribution each from the output capacitance discharge and the ESR drop. Use the following equations to calculate the required ESR and capacitance value:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}} \quad (18)$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q} \quad (19)$$

where I_{STEP} is the load step and $t_{RESPONSE}$ is the response time of the controller. Controller response time depends on the control-loop bandwidth.

Current Limit

The average current-mode control technique of the MAX5037A accurately limits the maximum output current per phase. The MAX5037A senses the voltage across the sense resistor and limits the peak inductor current (I_{L-PK}) accordingly. The ON cycle terminates when the current-sense voltage reaches 45mV (min). Use the following equation to calculate maximum current-sense resistor value:

$$R_{SENSE} = \frac{0.045}{\frac{I_{OUT}}{N}} \quad (20)$$

$$PD_R = \frac{2.5 \times 10^{-3}}{R_{SENSE}} \quad (21)$$

where PD_R is the power dissipation in sense resistors. Select 5% lower value of R_{SENSE} to compensate for any parasitics associated with the PC board. Also, select a noninductive resistor with the appropriate wattage rating.

Reverse Current Limit

The MAX5037A limits the reverse current in the case that V_{BUS} is higher than the preset output voltage setting.

Calculate the maximum reverse current based on V_{CLR}, the reverse current-limit threshold, and the current-sense resistor:

$$I_{REVERSE} = \frac{2 \times V_{CLR}}{R_{SENSE}}$$

Compensation

The main control loop consists of an inner current loop and an outer voltage loop. The MAX5037A uses an average current-mode control scheme to regulate the output voltage (Figure 3). I_{PHASE1} and I_{PHASE2} are the inner average current loops. The VEA output provides the controlling voltage for these current sources. The inner current loop absorbs the inductor pole reducing the order of the outer voltage loop to that of a single-pole system.

A resistive feedback network around the VEA provides the best possible response, since there are no capacitors to charge and discharge during large-signal excursions. The required amount of adaptive voltage positioning (ΔV_{OUT}) determines the VEA gain. Use the following equation to calculate the value for R_F when using adaptive voltage positioning:

$$R_F = \frac{I_{OUT} \times R_{IN}}{N \times G_C \times \Delta V_{OUT}} \quad (22)$$

$$G_C = \frac{0.05}{R_S} \quad (23)$$

where G_C is the current-source transconductance and N is the number of phases.

When designing the current-control loop ensure that the inductor downslope (when it becomes an upslope at the CEA output) does not exceed the ramp slope. This is a necessary condition to avoid subharmonic oscillations similar to those in peak current-mode control with insufficient slope compensation. Use the following equation to calculate the resistor R_{CF}:

$$R_{CF} \le \frac{2 \times f_{SW} \times L \times 10^2}{V_{OUT} \times R_{SENSE}} \quad (24)$$

For example, the maximum R_{CF} is 12kΩ for R_{SENSE} = 1.35mΩ.

C_{CF} provides a low-frequency pole while R_{CF} provides a midband zero. Place a zero at f_Z to obtain a phase bump at the crossover frequency. Place a high-frequency pole (f_P) at least a decade away from the crossover frequency to reduce the influence of the switching noise and achieve maximum phase margin. Use the following equations to calculate C_{CF} and C_{CFF}:

$$C_{CF} = \frac{1}{2 \times \pi \times f_Z \times R_{CF}} \quad (25)$$

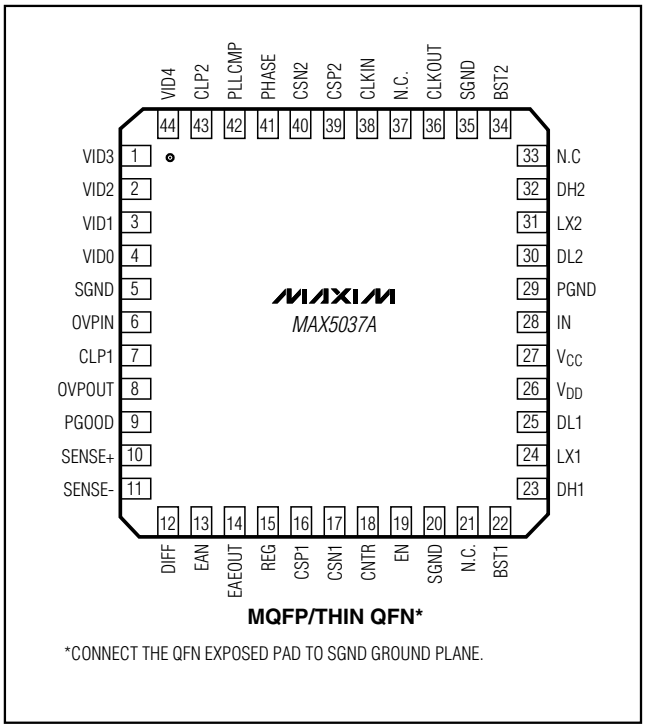
$$C_{CFF} = \frac{1}{2 \times \pi \times f_P \times R_{CF}} \quad (26)$$

PC Board Layout

Use the following guidelines to lay out the switching voltage regulator.

1) Place the V_{IN}, $V_{CC,}$ and V_{DD} bypass capacitors close to the MAX5037A.
2) Minimize the area and length of the high-current loops from the input capacitor, upper switching MOSFET, inductor, and output capacitor back to the input capacitor negative terminal.
3) Keep short the current loop formed by the lower switching MOSFET, inductor, and output capacitor.
4) Place the Schottky diodes close to the lower MOSFETs and on the same side of the PC board.
5) Keep the SGND and PGND isolated and connect them at one single point close to the negative terminal of the input filter capacitor.
6) Run the current-sense lines CS+ and CS- very close to each other to minimize the loop area. Similarly, run the remote voltage sense lines SENSE+ and SENSE- close to each other. Do not cross these critical signal lines through power circuitry. Sense the current right at the pads of the current-sense resistors.
7) Avoid long traces between the V_{DD} bypass capacitors, driver output of the MAX5037A, MOSFET gates, and PGND. Minimize the loop formed by the V_{DD} bypass capacitors, bootstrap diode, bootstrap capacitor, MAX5037A, and upper MOSFET gate.
8) Place the bank of output capacitors close to the load.
9) Distribute the power components evenly across the board for proper heat dissipation.
10) Provide enough copper area at and around the switching MOSFETs, inductor, and sense resistors to aid in thermal dissipation.
11) Use 4oz copper to keep the trace inductance and resistance to a minimum. Thin copper PC boards can compromise efficiency since high currents are involved in the application. Also, thicker copper conducts heat more effectively, thereby reducing thermal impedance.

Pin Configuration



MQFP/THIN QFN*

*CONNECT THE QFN EXPOSED PAD TO SGND GROUND PLANE.

Chip Information

TRANSISTOR COUNT: 5431

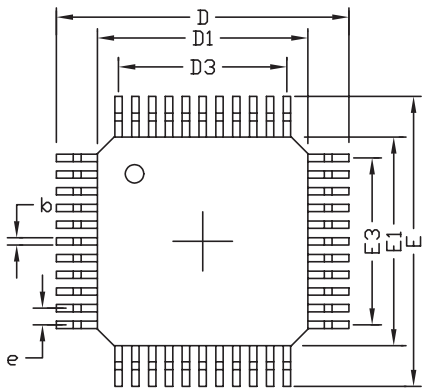
PROCESS: BiCMOS

VRM 9.0/VRM 9.1, Dual-Phase, Parallelable, Average-Current-Mode Controller

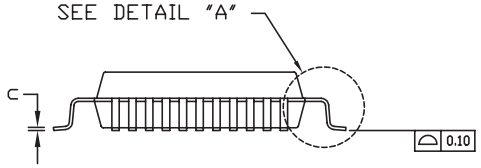
Package Information

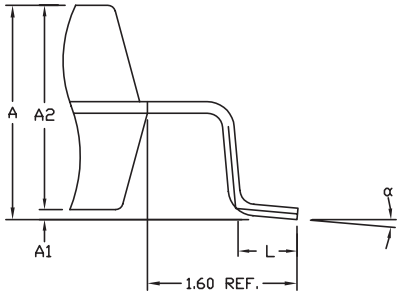
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

MQFP44.EPS



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	--	2.45	--	0.096
A1	0.000	0.250	0.000	0.010
A2	1.800	2.200	0.071	0.087
b	0.290	0.450	0.011	0.018
c	0.110	0.230	0.004	0.009
D	12.954	13.462	0.510	0.530
D1	9.906	10.109	0.390	0.398
D3	8.000 REF		0.315 REF	
E	12.954	13.462	0.510	0.530
E1	9.906	10.109	0.390	0.398
E3	8.000 REF		0.315 REF	
e	0.800 REF		0.031 REF	
L	0.730	1.030	0.029	0.041
α	-0	+7	+0	+7





DETAIL "A"

NOTES:

1. D1&E1 DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.25mm(.010").
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC MS-022-AB.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

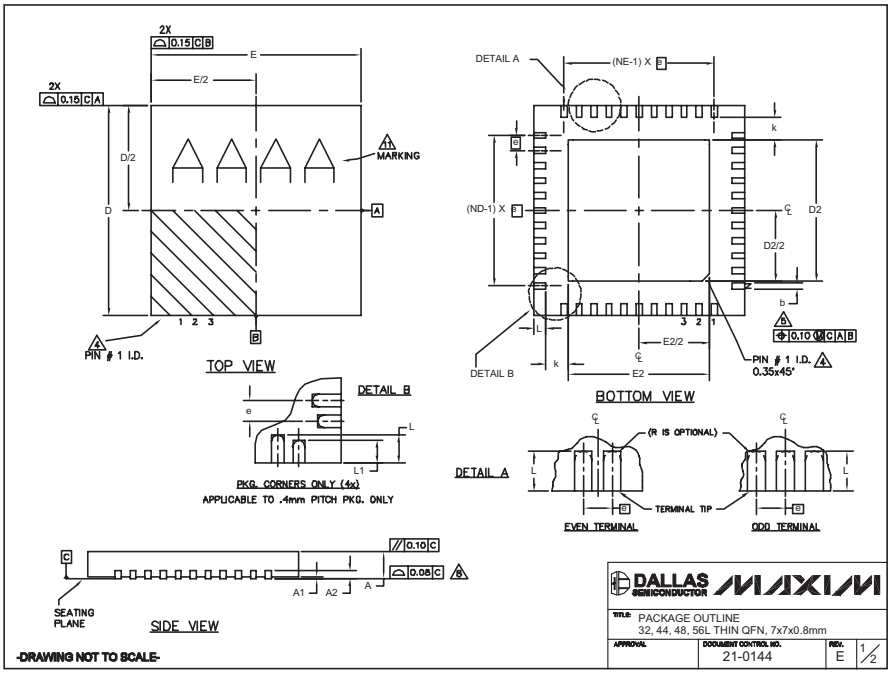
TITLE: PACKAGE OUTLINE 44L MQFP, 1.60 LEAD FORM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0826	D	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32, 44, 48L QFN.EPS



COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.40	0.50	0.60
L1	–	–	–	–	–	–	–	–	–	–	–	–	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C	DOWN BONDS ALLOWED
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–	YES
T3277-3	–	4.55	4.70	4.85	4.55	4.70	4.85	–	NO
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4877-1**	13,24,37,48	4.20	4.30	4.40	4.20	4.30	4.40	–	NO
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–	YES
T4877-4	–	5.46	5.60	5.63	5.45	5.60	5.63	–	YES
T4877-5	–	2.40	2.50	2.60	2.40	2.50	2.60	–	NO
T4877-6	–	5.45	5.60	5.63	5.45	5.60	5.63	–	NO
T4877-7	–	4.95	5.10	5.25	4.95	5.10	5.25	–	YES
T5677-1	–	5.20	5.30	5.40	5.20	5.30	5.40	–	YES

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877-1/-3/-4/-5/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE 32, 44, 48, 56L THIN QFN, 7x7x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0144
REV. E
2/2