Excelics SEMICONDUCTOR

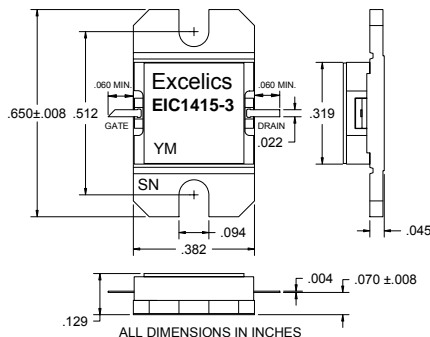# EIC1415-3

14.40 – 15.35GHz 3-Watt Internally Matched Power FET

FEATURES

- **14.40-15.35 GHz Bandwidth**
- **Input/Output Impedance Matched to 50 Ohms**
- **+34.5 dBm Output Power at 1dB Compression**
- **6.0 dB Power Gain at 1dB Compression**
- **25% Power Added Efficiency**
- **-42 dBc IM3 at Po = 23.5 dBm SCL**
- **Hermetic Metal Flange Package**
- **100% Tested for DC, RF, and R_{TH}**

ALL DIMENSIONS IN INCHES

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Caution! ESD sensitive device.

SYMBOL	PARAMETERS/TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
P_{1dB}	Output Power at 1dB Compression f = 14.40-15.35GHz V_{DS} = 10 V, I_{DSQ} ≈ 800mA	33.5	34.5		dBm
G_{1dB}	Gain at 1dB Compression f = 14.40-15.35GHz V_{DS} = 10 V, I_{DSQ} ≈ 800mA	5.0	6.0		dB
ΔG	Gain Flatness f = 14.40-15.35GHz V_{DS} = 10 V, I_{DSQ} ≈ 800mA			±0.6	dB
PAE	Power Added Efficiency at 1dB Compression V_{DS} = 10 V, I_{DSQ} ≈ 800mA f = 14.40-15.35GHz		25		%
Id_{1dB}	Drain Current at 1dB Compression f = 14.40-15.35GHz		900	1100	mA
IM3	Output 3rd Order Intermodulation Distortion Δf = 10 MHz 2-Tone Test; Pout = 23.5 dBm S.C.L[2] V_{DS} = 10 V, I_{DSQ} ≈ 65% IDSS f = 15.35GHz	-38	-42*		dBc
I_{DSS}	Saturated Drain Current V_{DS} = 3 V, V_{GS} = 0 V		1400	1800	mA
V_P	Pinch-off Voltage V_{DS} = 3 V, I_{DS} = 15 mA		-2.5	-4.0	V
R_{TH}	Thermal Resistance[3]		8.0	9.0	°C/W

Notes:
1. Tested with 100 Ohm gate resistor.   2. S.C.L. = Single Carrier Level.   3. Overall Rth depends on case mounting.
* These devices are available screened for IM3 performance. Please contact factory with your requirement.

ABSOLUTE MAXIMUM RATINGS FOR CONTINUOUS OPERATION[1,2]

SYMBOL	CHARACTERISTIC	VALUE
V_{DS}	Drain to Source Voltage	10 V
V_{GS}	Gate to Source Voltage	-4.5 V
I_{DS}	Drain Current	IDSS
I_{GSF}	Forward Gate Current	30 mA
P_{IN}	Input Power	@ 3dB compression
P_T	Total Power Dissipation	14 W
T_{CH}	Channel Temperature	150°C
T_{STG}	Storage Temperature	-65/+150°C

Notes:
1. Operating the device beyond any of the above ratings may result in permanent damage or reduction of MTTF.
2. Bias conditions must also satisfy the following equation $P_T < (T_{CH} - T_{PKG})/R_{TH}$; where T_{PKG} = temperature of package, and $P_T = (V_{DS} * I_{DS}) – (P_{OUT} – P_{IN})$.

Specifications are subject to change without notice.
Excelics Semiconductor, Inc. 310 De Guigne Drive, Sunnyvale, CA 94085   page 1 of 1
Phone: 408-737-1711 Fax: 408-737-1868 Web: www.excelics.com   Revised December 2004