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September 21, 2010

FN7393.2

18-Channel TFT-LCD Reference Voltage Generator

The EL5525 is designed to produce the reference voltages required in TFT-LCD applications. Each output is programmed to the required voltage with 10 bits of resolution. Reference pins determine the high and low voltages of the output range, which are capable of swinging to either supply rail. Programming of each output is performed using the serial interface. A serial out pin enables daisy chaining of multiple devices.

A number of the EL5525 can be stacked for applications requiring more than 18 outputs. The reference inputs can be tied to the rails, enabling each part to output the full voltage range, or alternatively, they can be connected to external resistors to split the output range and enable finer resolutions of the outputs.

The EL5525 has 18 outputs and comes in a 38-pin HTSSOP package. It is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. NUMBER
EL5525IREZ*	5525IREZ	-40 to +85	38-Pin HTSSOP	MDP0048
EL5525IREZ-T7*	5525IREZ	-40 to +85	38-Pin HTSSOP	MDP0048
EL5525IREZ-T13*	5525IREZ	-40 to +85	38-Pin HTSSOP	MDP0048

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

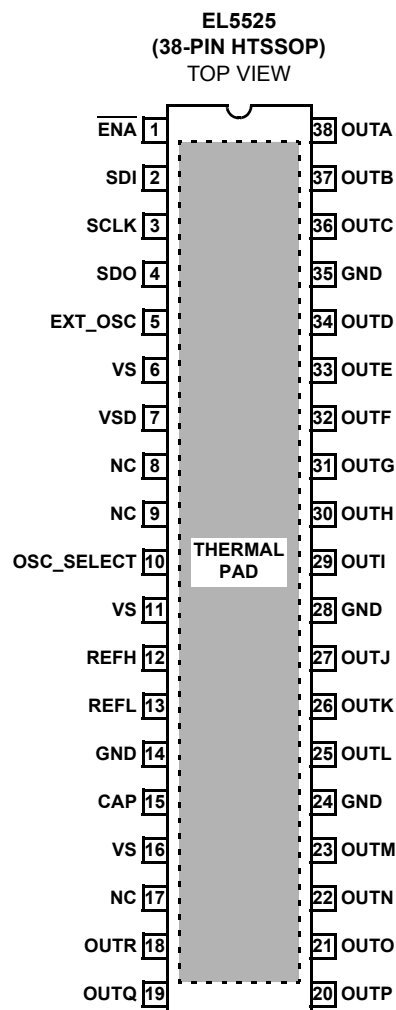
Features

- 18-channel Reference Outputs
- Accuracy of $\pm 0.1\%$
- Supply Voltage of 4.5V to 16.5V
- Digital Supply 3.3V to 5V
- Low Supply Current of 15mA
- Rail-to-Rail Capability
- Internal Thermal Protection
- Pb-Free Available (RoHS Compliant)

Applications

- TFT-LCD Drive Circuits
- Reference Voltage Generators

Pinout



Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$)

Supply Voltage

Between V_S and GND 4.5V(min) to 18V(max)Between V_{SD} and GND 3V(min) to V_S and +7(max)

Maximum Continuous Output Current 30mA

Thermal Information

Maximum Die Temperature +125°C

Storage Temperature -65°C to +150°C

Pb-Free Reflow Profile. see link below
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>**Operating Conditions**

Ambient Operating Temperature -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_S = 15\text{V}$, $V_{SD} = 5\text{V}$, $V_{REFH} = 13\text{V}$, $V_{REFL} = 2\text{V}$, $R_L = 1.5\text{k}\Omega$ and $C_L = 200\text{pF}$ to 0V, $T_A = +25^\circ\text{C}$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_S	Supply Current	No load		15	18	mA
I_{SD}	Digital Supply Current			0.17	0.35	mA
ANALOG						
V_{OL}	Output Swing Low	Sinking 5mA ($V_{REFH} = 15\text{V}$, $V_{REFL} = 0$)		50	150	mV
V_{OH}	Output Swing High	Sourcing 5mA ($V_{REFH} = 15\text{V}$, $V_{REFL} = 0$)	14.85	14.95		V
I_{SC}	Short Circuit Current	$R_L = 10\Omega$	100	140		mA
PSRR	Power Supply Rejection Ratio	V_{S+} is moved from 14V to 16V	45	60		dB
t_D	Program to Out Delay			4		ms
V_{AC}	Accuracy Referred to the Ideal Value	Code = 512		20		mV
ΔV_{MIS}	Channel to Channel Mismatch	Code = 512		2		mV
V_{DROOP}	Droop Voltage			1	2	mV/ms
R_{INH}	Input Resistance @ V_{REFH} , V_{REFL}			34		k Ω
REG	Load Regulation	$I_{OUT} = 5\text{mA}$ step		0.5	1.5	mV/mA
BG	Band Gap		1.1	1.3	1.6	V
DIGITAL						
V_{IH}	Logic 1 Input Voltage		2			V
V_{IL}	Logic 0 Input Voltage				1	V
F_{CLK}	Clock Frequency				5	MHz
t_S	Setup Time			20		ns
t_H	Hold Time			20		ns
t_{LC}	Load to Clock Time			20		ns
t_{CE}	Clock to Load Line			20		ns
t_{DCO}	Clock to Out Delay Time	Negative edge of SCLK		10		ns
R_{SDIN}	S_{DIN} Input Resistance			1		G Ω
T_{PULSE}	Minimum Pulse Width for EXT_OSC Signal			5		μs
Duty Cycle	Duty Cycle for EXT_OSC Signal			50		%
F_{OSC}	Internal Refresh Oscillator Frequency	OSC_Select = 0		21		kHz
INL	Integral Nonlinearity Error			1.3		LSB
DNL	Differential Nonlinearity Error			0.5		LSB

Pin Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	ENA	Logic Input	Chip select, low enables data input to logic
2	SDI	Logic Input	Serial data input
3	SCLK	Logic Input	Serial data clock
4	SDO	Logic Output	Serial data output
5	EXT_OSC	Input/Output	Oscillator pin for synchronizing
6, 11, 16	VS	Power	Positive supply voltage for analog circuits (4.5V to 16.5V)
7	VSD	Power	Positive power supply for digital circuits (3.3V to 5V)
8, 9, 17	NC		Not connected
10	OSC_SELECT		Oscillator select, "0" = internal, "1" = external
12	REFH	Analog Input	High reference voltage
13	REFL	Analog Input	Low reference voltage
14, 24, 28, 35	GND	Power	Ground
15	CAP	Analog	Decoupling capacitor for internal reference
18	OUTR	Analog Output	Channel R output voltage
19	OUTQ	Analog Output	Channel Q output voltage
20	OUTP	Analog Output	Channel P output voltage
21	OUTO	Analog Output	Channel O output voltage
22	OUTN	Analog Output	Channel N output voltage
23	OUTM	Analog Output	Channel M output voltage
25	OUTL	Analog Output	Channel L output voltage
26	OUTK	Analog Output	Channel K output voltage
27	OUTJ	Analog Output	Channel J output voltage
29	OUTI	Analog Output	Channel I output voltage
30	OUTH	Analog Output	Channel H output voltage
31	OUTG	Analog Output	Channel G output voltage
32	OUTF	Analog Output	Channel F output voltage
33	OUTE	Analog Output	Channel E output voltage
34	OUTD	Analog Output	Channel D output voltage
36	OUTC	Analog Output	Channel C output voltage
37	OUTB	Analog Output	Channel B output voltage
38	OUTA	Analog Output	Channel A output voltage

Typical Performance Curves

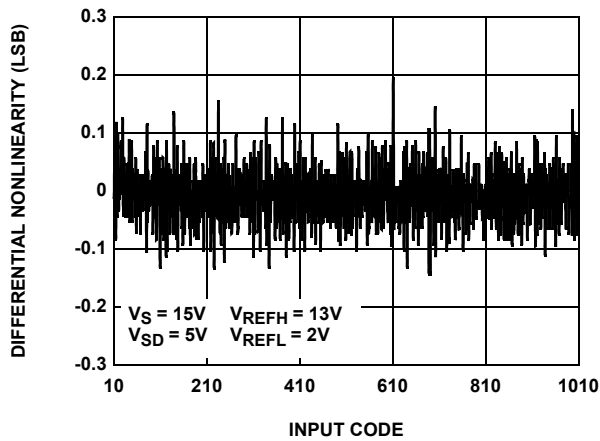


FIGURE 1. DIFFERENTIAL NONLINEARITY vs CODE

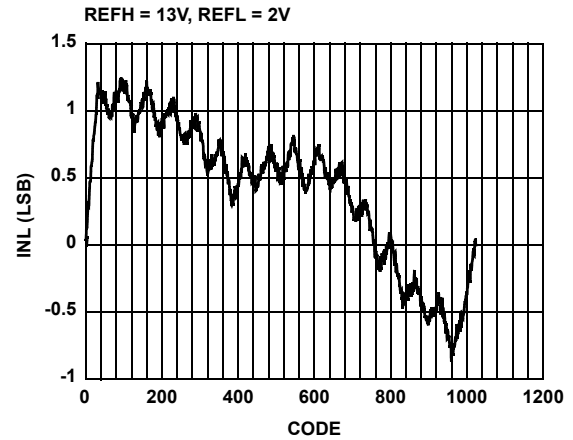


FIGURE 2. INTEGRAL NONLINEARITY ERROR

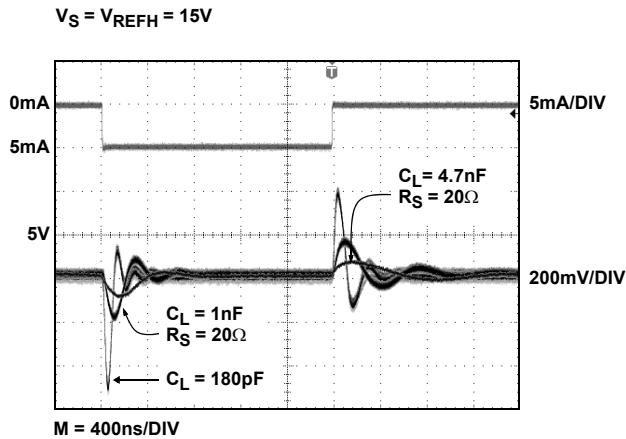


FIGURE 3. TRANSIENT LOAD REGULATION (SOURCING)

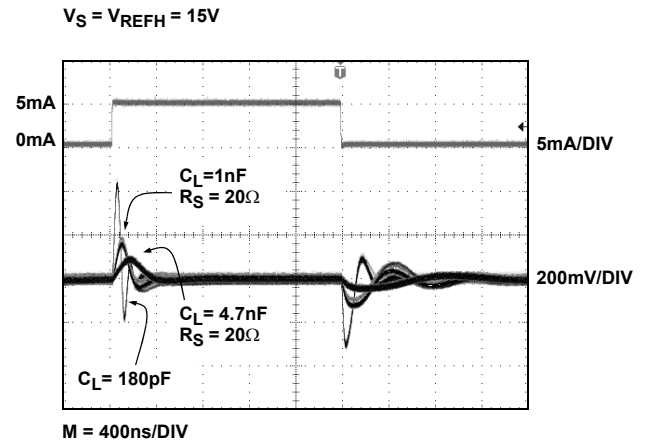


FIGURE 4. TRANSIENT LOAD REGULATION (SINKING)

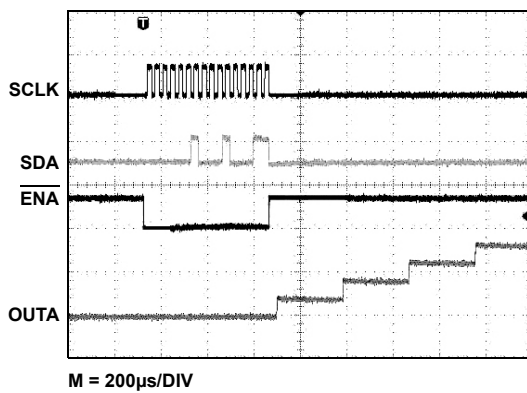


FIGURE 5. LARGE SIGNAL RESPONSE (RISING FROM 0V TO 8V)

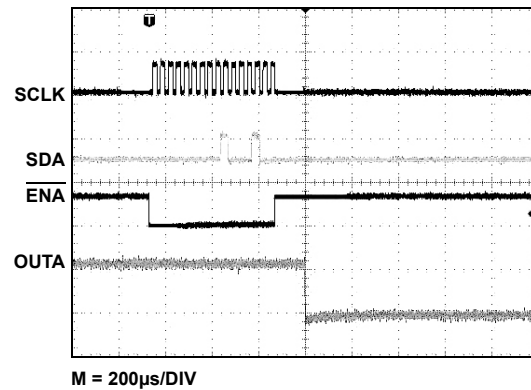


FIGURE 6. SMALL SIGNAL RESPONSE (FALLING FROM 200mV TO 100mV)

General Description

The EL5525 provides a versatile method of providing the reference voltages that are used in setting the transfer characteristics of LCD display panels. The V/T (Voltage/Transmission) curve of the LCD panel requires that a correction is applied to make it linear; however, if the panel is to be used in more than one application, the final curve may differ for different applications. By using the EL5525, the V/T curve can be changed to optimize its characteristics according to the required application of the display product. Each of the eight reference voltage outputs can be set with a 10-bit resolution. These outputs can be driven to within 50mV of the power rails of the EL5525. As all of the output buffers are identical, it is also possible to use the EL5525 for applications other than LCDs where multiple voltage references are required that can be set to 10 bit accuracy.

Digital Interface

The EL5525 uses a simple 3-wire SPI compliant digital interface to program the outputs. The EL5525 can support the clock rate up to 5MHz.

Serial Interface

The EL5525 is programmed through a three-wire serial interface. The start and stop conditions are defined by the $\overline{\text{ENA}}$ signal. While the $\overline{\text{ENA}}$ is low, the data on the SDI (serial data input) pin is shifted into the 16-bit shift register on the positive edge of the SCLK (serial clock) signal. The MSB (bit 15) is loaded first and the LSB (bit 0) is loaded last (see Table 1). After the full 16-bit data has been loaded, the $\overline{\text{ENA}}$ is pulled high and the addressed output channel is updated. The SCLK is disabled internally when the $\overline{\text{ENA}}$ is high. The SCLK must be low before the $\overline{\text{ENA}}$ is pulled low.

To facilitate the system designs that use multiple EL5525 chips, a buffered serial output of the shift register (SDO pin) is available. Data appears on the SDO pin at the 16th falling SCLK edge after being applied to the SDI pin.

To control the multiple EL5525 chips from a single three-wire serial port, just connect the $\overline{\text{ENA}}$ pins and the SCLK pins

together, connect the SDO pin to the SDI pin on the next chip. While the $\overline{\text{ENA}}$ is held low, the 16m-bit data is loaded to the SDI input of the first chip. The first 16-bit data will go to the last chip and the last 16-bit data will go to the first chip. While the $\overline{\text{ENA}}$ is held high, all addressed outputs will be updated simultaneously.

The Serial Timing Diagram and parameters table show the timing requirements for three-wire signals.

The serial data has a minimum length of 16 bits, the MSB (most significant bit) is the first bit in the signal. The bits are allocated to the following functions (also refer to Table 1).

- Bit 15 is always set to a zero
- Bits 14 through 10 select the channel to be written to, these are binary coded with channel A = 0, and channel R = 17
- The 10-bit data is on bits 9 through 0. Some examples of data words are shown in Table 3.

TABLE 1. CONTROL BITS LOGIC TABLE

BIT	NAME	DESCRIPTION
B15	Test	Always 0
B14	A4	Channel Address
B13	A3	Channel Address
B12	A2	Channel Address
B11	A1	Channel Address
B10	A0	Channel Address
B9	D9	Data
B8	D8	Data
B7	D7	Data
B6	D6	Data
B5	D5	Data
B4	D4	Data
B3	D3	Data
B2	D2	Data
B1	D1	Data
B0	D0	Data

Serial Timing Diagram

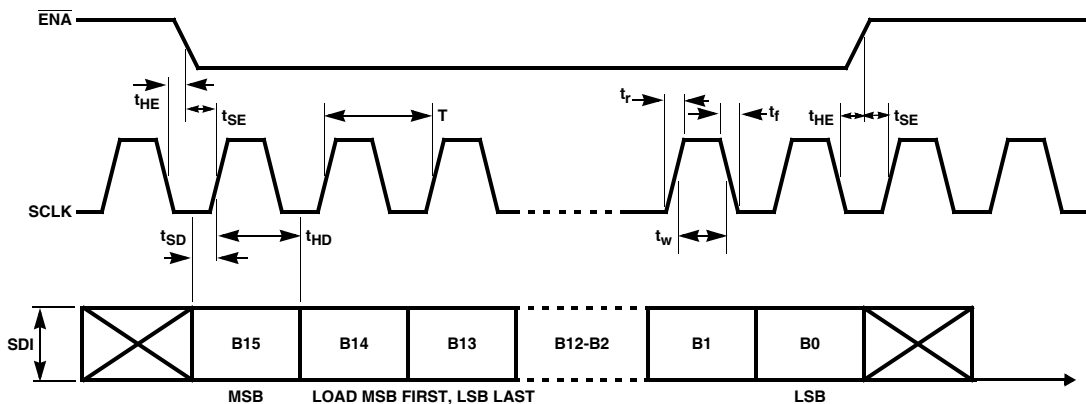


TABLE 2. SERIAL TIMING PARAMETERS

PARAMETER	RECOMMENDED OPERATING RANGE	DESCRIPTION
T	≥200ns	Clock Period
t _r /t _f	0.05 * T	Clock Rise/Fall Time
t _{HE}	≥10ns	$\overline{\text{EN}}\overline{\text{A}}$ Hold Time
t _{SE}	≥10ns	$\overline{\text{EN}}\overline{\text{A}}$ Setup Time
t _{HD}	≥10ns	Data Hold Time
t _{SD}	≥10ns	Data Setup Time
t _W	0.50 * T	Clock Pulse Width

TABLE 3. SERIAL PROGRAMMING EXAMPLES

Control	Channel Address					Data										Condition
C1	A4	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Channel A, Value = 0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	Channel A, Value = 1023
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	Channel A, Value = 512
0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	Channel C, Value = 513
0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	Channel H, Value = 31
0	1	0	0	0	1	0	0	0	0	0	1	1	1	1	1	Channel R, Value = 31

Analog Section

Transfer Function

The transfer function is: shown in Equation 1:

$$V_{\text{OUT(IDEAL)}} = V_{\text{REFL}} + \frac{\text{data}}{1024} \times (V_{\text{REFH}} - V_{\text{REFL}}) \quad (\text{EQ. 1})$$

where data is the decimal value of the 10-bit data binary input code.

The output voltages from the EL5525 will be derived from the reference voltages present at the V_{REFL} and V_{REFH} pins. The impedance between those two pins is about 32kΩ.

Care should be taken that the system design holds these two reference voltages within the limits of the power rails of the EL5525. $\text{GND} < V_{\text{REFH}} \leq V_{\text{S}}$ and $\text{GND} \leq V_{\text{REFL}} \leq V_{\text{REFH}}$.

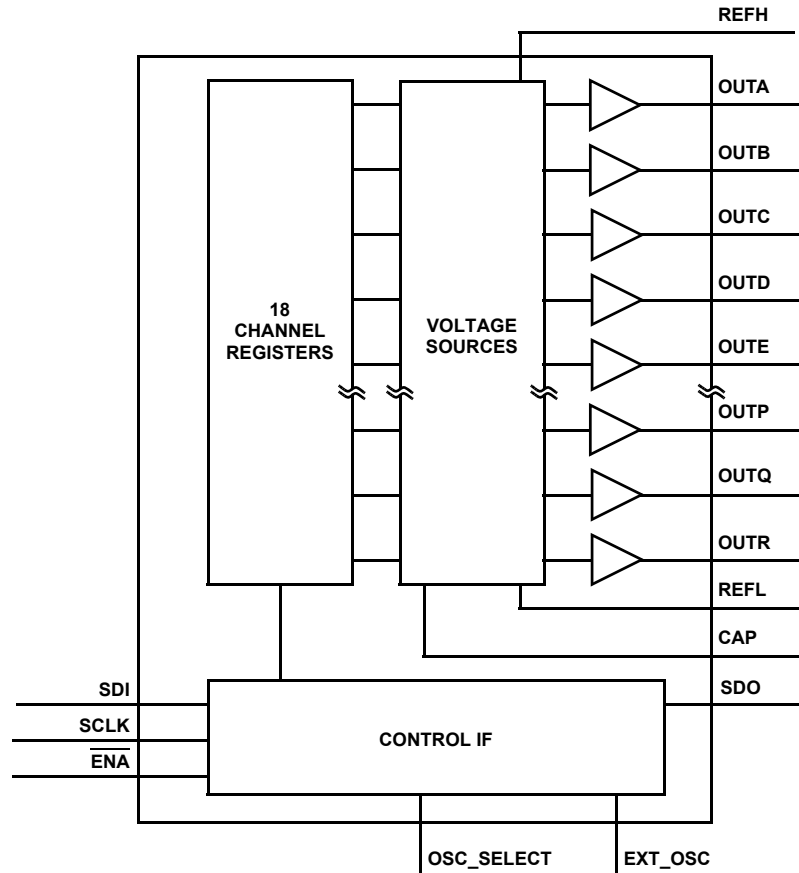
Clock Oscillator

The EL5525 requires an internal clock or external clock to refresh its outputs. The outputs are refreshed at the falling OSC clock edges. The output refreshed switches open at the rising edges of the OSC clock. The driving load shouldn't be changed at the rising edges of the OSC clock. Otherwise, it will generate a voltage error at the outputs. This clock may be input or output via the clock pin labeled EXT_OSC. The internal clock is provided by an internal oscillator running at approximately 21kHz and can be output to the EXT_OSC pin. In a 2 chip system, if the driving loads are stable, one chip may be programmed to use the internal oscillator; then the OSC pin will output the clock from the internal oscillator. The second chip may have the OSC pin connected to this clock source.

For transient load application, the external clock Mode should be used to ensure all functions are synchronized together. The positive edge of the external clock to the OSC pin should be timed to avoid the transient load effect. The Application Drawing shows the LCD H rate signal used, here the positive clock edge is timed to avoid the transient load of the column driver circuits.

After power on, the chip will start with the internal oscillator mode. At this time, the EXT_OSC pin will be in a high impedance condition to prevent contention. By setting pin 10 to high, the chip is on external clock mode. Setting pin 10 to low, the chip is on internal clock mode.

Block Diagram



Channel Outputs

Each of the channel outputs has a rail-to-rail buffer. This enables all channels to have the capability to drive to within 50mV of the power rails, (see Table Electrical Specifications on page 2 for details).

When driving large capacitive loads, a series resistor should be placed in series with the output. (Usually between 5Ω and 50Ω).

Each of the channels is updated on a continuous cycle, the time for the new data to appear at a specific output will depend on the exact timing relationship of the incoming data to this cycle.

The best-case scenario is when the data has just been captured and then passed on to the output stage immediately; this can be as short as 48μs. In the worst-case scenario, this will be 860μs for EL5525, when the data has just missed the cycle at $f_{OSC} = 21\text{kHz}$.

When a large change in output voltage is required, the change will occur in 2V steps, thus the requisite number of timing cycles will be added to the overall update time. This means that a large change of 16V can take between 6.8ms and 7.2ms depending on the absolute timing relative to the update cycle.

Output Stage and the Use of External Oscillator

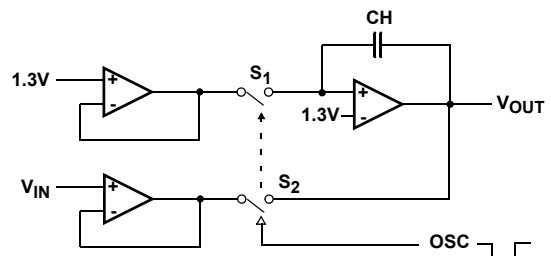


FIGURE 7. SIMPLIFIED OUTPUT SAMPLE AND HOLD AMP STAGE FOR ONE CHANNEL

The output voltage is generated from the DAC, which is V_{IN} in Figure 7. The refreshed switches are controlled by the internal or external oscillator signal. When the OSC clock signal is low, switches S_1 and S_2 are closed. The output $V_{OUT} = V_{IN}$ and at the same time the sample and hold cap CH is being charged. When the OSC clock signal is high, the refreshed switches S_1 and S_2 are opened and the output voltage is maintained by CH. This refreshed process will repeat every 18 clock cycles for each channel. The time

takes to update the output depends on the timing at the V_{IN} and the state of the switches. It can take 1 to 18 clock cycles to update each output.

For the sample and hold capacitor CH to maintain the correct output voltage, the driving load shouldn't be changed at the rising edge of the OSC signal. Since at the rising edge of the OSC clock, the refreshed switches are being opened, if the load changes at that time, it will generate an error output voltage. For a fixed load condition, the internal oscillator can be used.

For the transient load condition, the external OSC mode should be used to avoid the conflict between the rising edge of the OSC signal and the changing load. So a timing delay circuit will be needed to delay the OSC signal and avoid the rising edge of the OSC signal and changing the load at the same time.

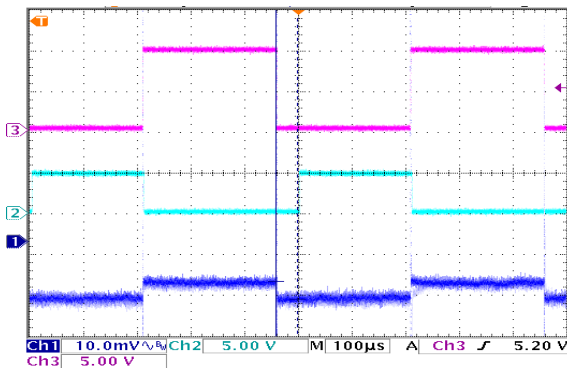


FIGURE 8. TRANSIENT LOAD RESPONSE

Channel 3 --- sinking and sourcing 5mA current

Channel 2 --- EXT_OSC signal

Channel 1 --- V_{OUT}

In Figure Table 8 on page 8, the OSC signal is synchronized to the load signal. The rising edge of the OSC signal is then delayed by some amount of time and gives enough time for CH to be charged to a new voltage before the switches are opened.

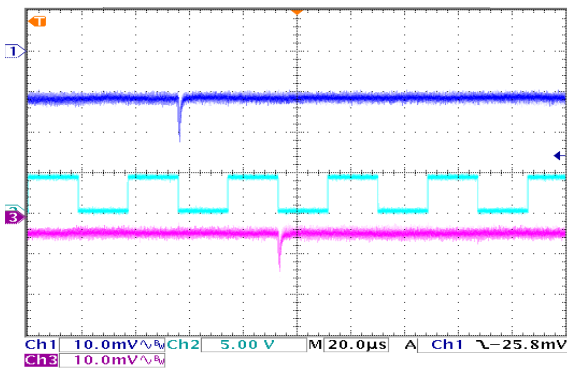


FIGURE 9. CHANNEL TO CHANNEL REFRESH

Ch1 --- Output1

Ch3 --- Output2

Ch2 --- EXT_OSC

At the falling edge of the OSC, output 1 is being refreshed, and one clock cycle later, output 2 is being refreshed. The spike you see here is the response of the output amplifier when the refreshed switches are closed. When driving a big capacitor load, there will be ringing at the spikes because the phase margin of the amplifier is decreased.

The speed of the external OSC signal shouldn't be greater than 70kHz because for the worst condition, it will take at least 4μs to charge the sample and hold capacitor CH. The pulse width has to be at least 4μs long. From our lab test, the duty cycle of the OSC signal must be greater than 30%.

POWER DISSIPATION

With the 30mA maximum continues output drive capability for each channel, it is possible to exceed the +125°C absolute maximum junction temperature. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the part to remain in the safe operation.

The maximum power dissipation allowed in a package is determined according to: Equation 2:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad (\text{EQ. 2})$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by the IC is the total quiescent supply current times the total power supply voltage and plus the power in the IC due to the loads.

$$P_{DMAX} = V_S \times I_S + \sum [(V_S - V_{OUTi}) \times I_{LOADi}] \quad (\text{EQ. 3})$$

when sourcing, and:

$$P_{DMAX} = V_S \times I_S + \sum (V_{OUTi} \times I_{LOADi}) \quad (\text{EQ. 4})$$

when sinking.

Where:

- $i = 18$
- V_S = Supply voltage
- I_S = Quiescent current
- V_{OUTi} = Output voltage of the i channel
- I_{LOADi} = Load current of the i channel

By setting the two $P_{D\text{MAX}}$ equations equal to each other, we can solve for the R_{LOADS} to avoid the device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat.

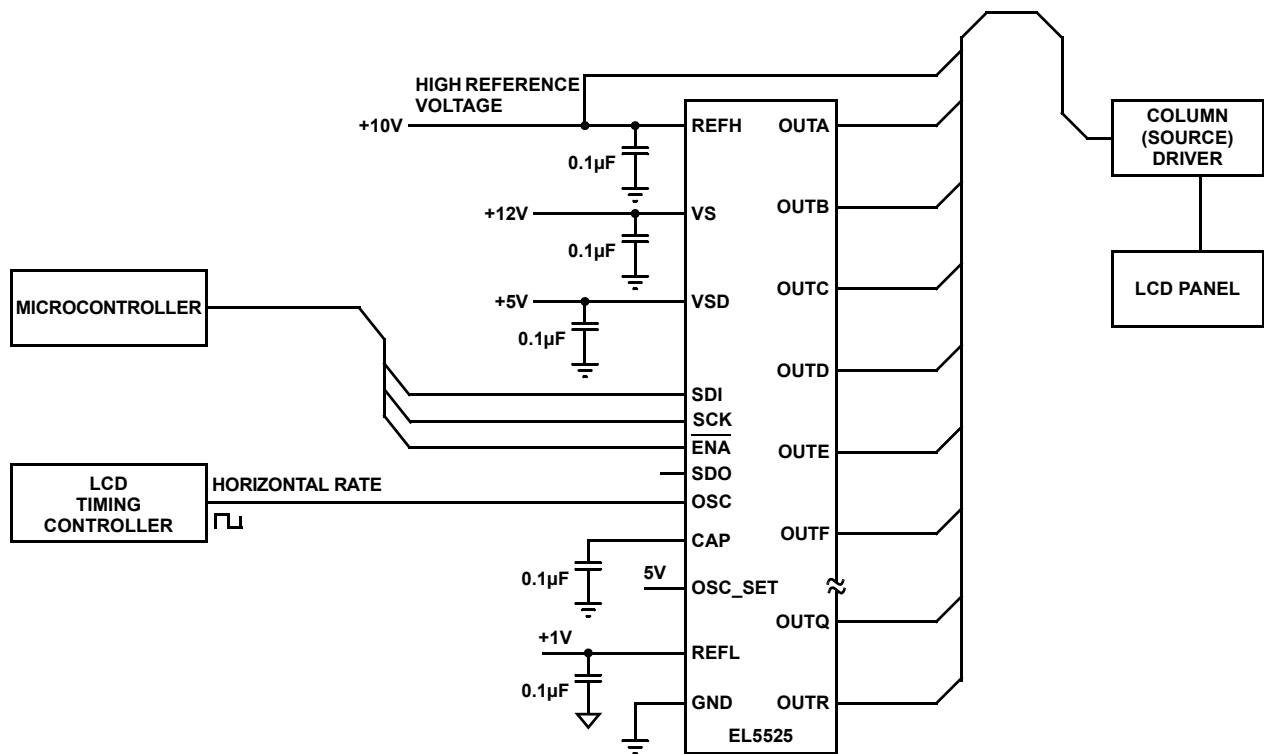
THERMAL SHUTDOWN

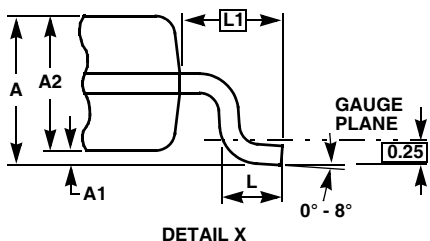
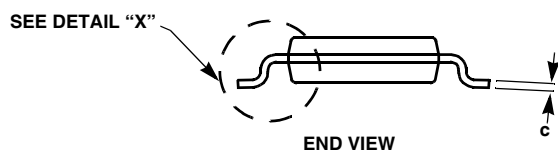
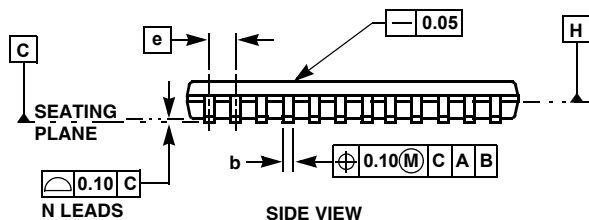
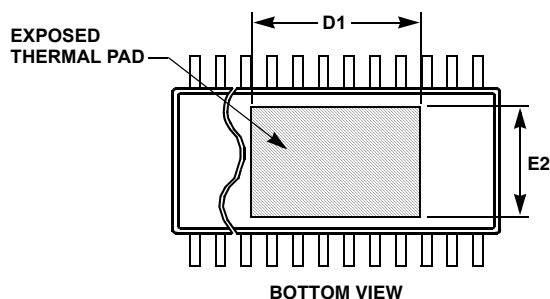
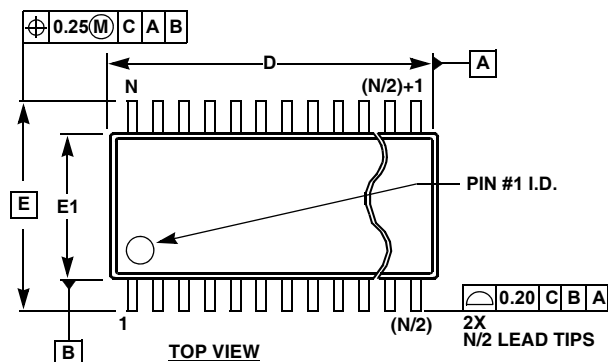
The EL5525 has an internal thermal shutdown circuitry that prevents overheating of the part. When the junction temperature goes up to about $+150^{\circ}\text{C}$, the part will be disabled. When the junction temperature drops down to about $+120^{\circ}\text{C}$, the part will be enabled. With this feature, any short circuit at the outputs will enable the thermal shutdown circuitry to disable the part.

POWER SUPPLY BYPASSING AND PRINTED CIRCUIT BOARD LAYOUT

Good printed circuit board layout is necessary for optimum performance. A low impedance and clean analog ground plane should be used for the EL5525. The traces from the two ground pins to the ground plane must be very short. The thermal pad of the EL5525 should be connected to the analog ground plane. Lead length should be as short as possible and all power supply pins must be well bypassed. A $0.1\mu\text{F}$ ceramic capacitor must be placed very close to the V_S , V_{REFH} , V_{REFL} , and CAP pins. A $4.7\mu\text{F}$ local bypass tantalum capacitor should be placed to the V_S , V_{REFH} , and V_{REFL} pins.

Application Drawing



HTSSOP (Heat-Sink TSSOP) Family**MDP0048****HTSSOP (HEAT-SINK TSSOP) FAMILY**

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	20 LD	24 LD	28 LD	38 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.075	0.075	0.075	0.075	0.075	±0.075
A2	0.90	0.90	0.90	0.90	0.90	+0.15/-0.10
b	0.25	0.25	0.25	0.25	0.22	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	6.50	7.80	9.70	9.70	±0.10
D1	3.2	4.2	4.3	5.0	7.25	Reference
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
E2	3.0	3.0	3.0	3.0	3.0	Reference
e	0.65	0.65	0.65	0.65	0.50	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
N	14	20	24	28	38	Reference

Rev. 3 2/07

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at Datum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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