

Single P-channel MOSFET

ELM14443AA-N

General description

ELM14443AA-N uses advanced trench technology to provide excellent $R_{ds(on)}$, low gate charge and low gate resistance.

Features

- $V_{ds} = -40V$
- $I_d = -6.5A$ ($V_{gs} = -10V$)
- $R_{ds(on)} < 42m\Omega$ ($V_{gs} = -10V$)
- $R_{ds(on)} < 63m\Omega$ ($V_{gs} = -4.5V$)

Maximum absolute ratings

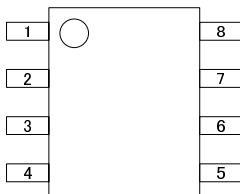
Parameter		Symbol	Limit	Unit	Note
Drain-source voltage		V_{ds}	-40	V	
Gate-source voltage		V_{gs}	± 20	V	
Continuous drain current	$T_a = 25^\circ C$	I_d	-6.5	A	1
	$T_a = 70^\circ C$		-5.0		
Pulsed drain current		I_{dm}	-20	A	2
Power dissipation	$T_a = 25^\circ C$	P_d	3.1	W	1
	$T_a = 70^\circ C$		2.0		
Junction and storage temperature range		T_j, T_{stg}	-55 to 150	$^\circ C$	

Thermal characteristics

Parameter		Symbol	Typ.	Max.	Unit	Note
Maximum junction-to-ambient	$t \leq 10s$	$R\theta_{ja}$	24	40	$^\circ C/W$	1
Maximum junction-to-ambient	Steady-state		54	75	$^\circ C/W$	
Maximum junction-to-lead	Steady-state	$R\theta_{jl}$	21	30	$^\circ C/W$	3

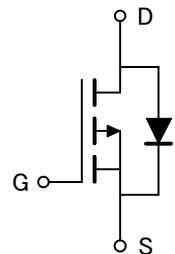
Pin configuration

SOP-8 (TOP VIEW)



Pin No.	Pin name
1	SOURCE
2	SOURCE
3	SOURCE
4	GATE
5	DRAIN
6	DRAIN
7	DRAIN
8	DRAIN

Circuit



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Electrical characteristics

Ta=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	BVdss	Id=-250 μ A, Vgs=0V	-40			V
Zero gate voltage drain current	Idss	Vds=-32V Vgs=0V			-1	μ A
		Tj=55°C			-5	
Gate-body leakage current	Igss	Vds=0V, Vgs= $\pm$ 20V			$\pm$ 100	nA
Gate threshold voltage	Vgs(th)	Vds=Vgs, Id=-250 μ A	-1.0	-1.9	-3.0	V
On state drain current	Id(on)	Vgs=-10V, Vds=-5V	-20			A
Static drain-source on-resistance	Rds(on)	Vgs=-10V Id=-6A		33.3	42.0	m Ω
		Tj=125°C		54.0	68.0	
		Vgs=-4.5V, Id=-5A		48.0	63.0	m Ω
Forward transconductance	Gfs	Vds=-5V, Id=-6A		14		S
Diode forward voltage	Vsd	Is=-1A, Vgs=0V		-0.75	-1.00	V
Max. body-diode continuous current	Is				-6	A
DYNAMIC PARAMETERS						
Input capacitance	Ciss	Vgs=0V, Vds=-20V, f=1MHz		657		pF
Output capacitance	Coss			143		pF
Reverse transfer capacitance	Crss			63		pF
Gate resistance	Rg	Vgs=0V, Vds=0V, f=1MHz		6.5		Ω
SWITCHING PARAMETERS						
Total gate charge (10V)	Qg	Vgs=-10V, Vds=-20V, Id=-6A		14.2		nC
Total gate charge (4.5V)	Qg			7.1		nC
Gate-source charge	Qgs			2.2		nC
Gate-drain charge	Qgd			4.1		nC
Turn-on delay time	td(on)	Vgs=-10V, Vds=-20V RI=3.7 Ω , Rgen=3 Ω		7.7		ns
Turn-on rise time	tr			8.0		ns
Turn-off delay time	td(off)			26.5		ns
Turn-off fall time	tf			11.5		ns
Body diode reverse recovery time	trr	If=-6A, dI/dt=100A/ μ s		21.9		ns
Body diode reverse recovery charge	Qrr	If=-6A, dI/dt=100A/ μ s		14.9		nC

NOTE :

1. The value of R θ ja is measured with the device mounted on 1in² FR-4 board of 2oz. Copper, in still air environment with Ta=25°C. The value in any given applications depends on the user's specific board design, The current rating is based on the t $\leq$ 10s thermal resistance rating.
2. Repetitive rating, pulse width limited by junction temperature.
3. The R θ ja is the sum of the thermal impedance from junction to lead R θ jl and lead to ambient.
4. The static characteristics in Figures 1 to 6 are obtained using 80 μ s pulses, duty cycle 0.5%max.
5. These tests are performed with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with Ta=25°C. The SOA curve provides a single pulse rating.

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Typical electrical and thermal characteristics

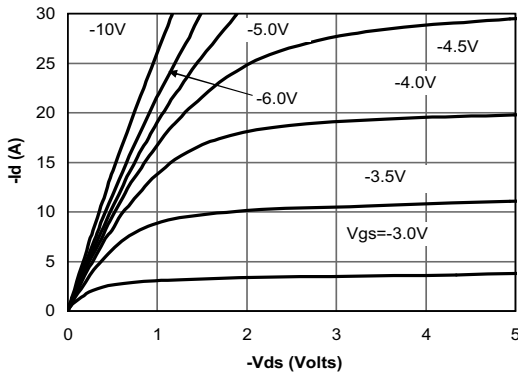


Fig 1: On-Region Characteristics

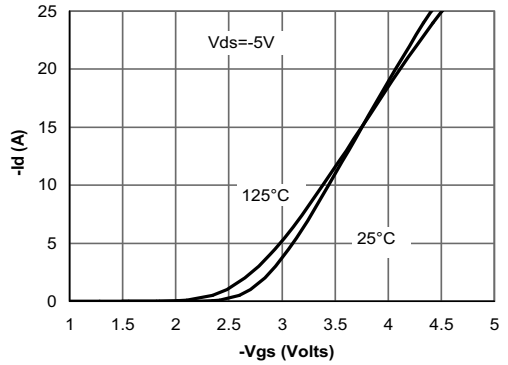


Figure 2: Transfer Characteristics

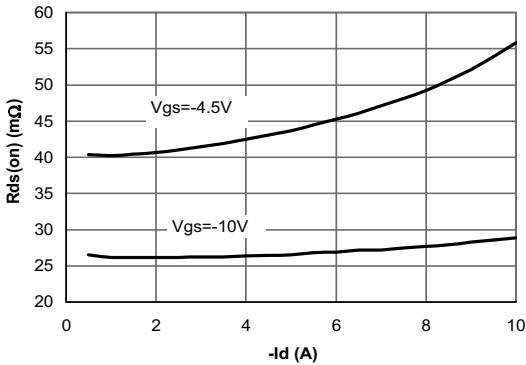


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

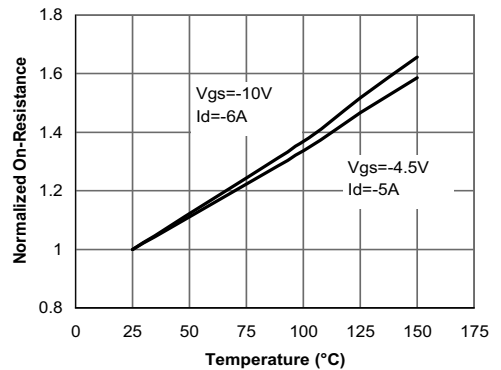


Figure 4: On-Resistance vs. Junction Temperature

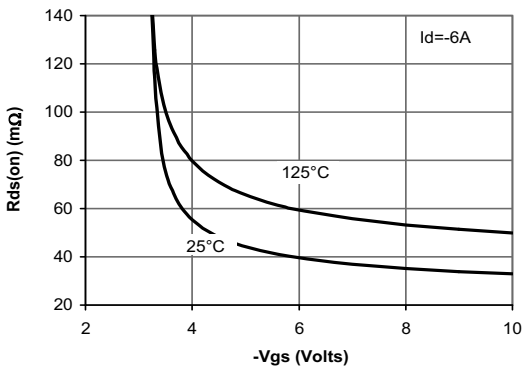


Figure 5: On-Resistance vs. Gate-Source Voltage

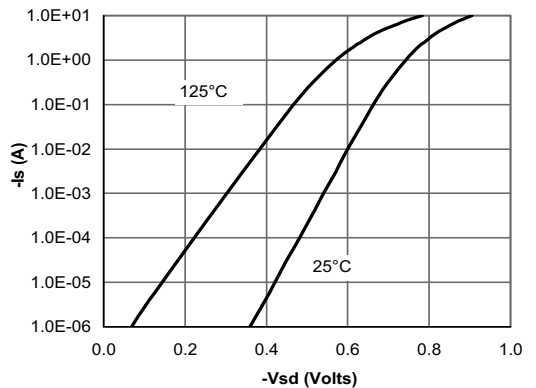


Figure 6: Body-Diode Characteristics

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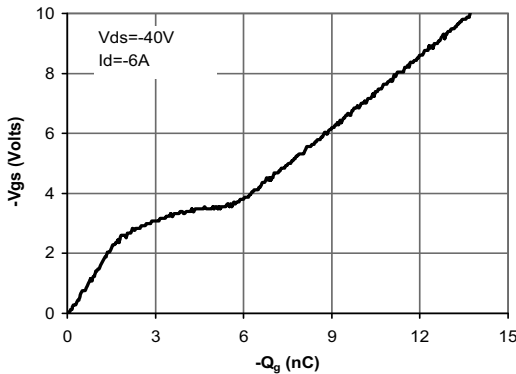


Figure 7: Gate-Charge Characteristics

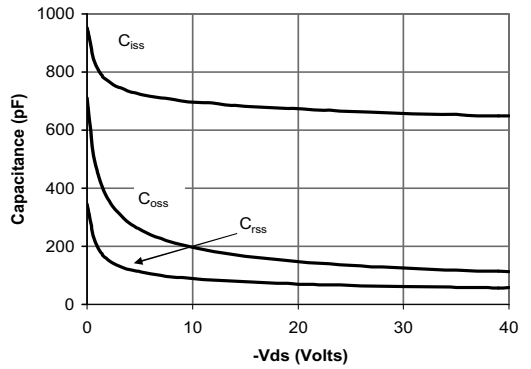


Figure 8: Capacitance Characteristics

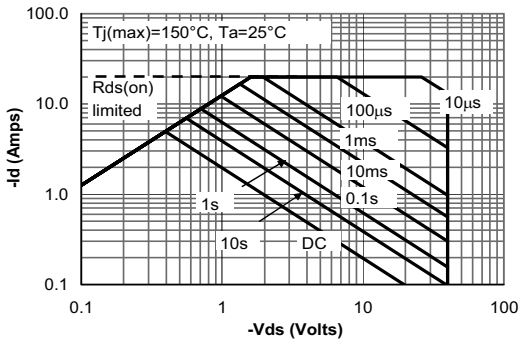


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

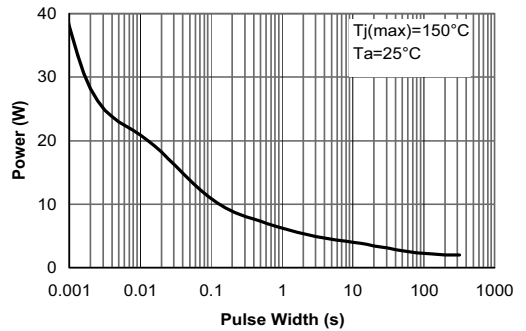


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

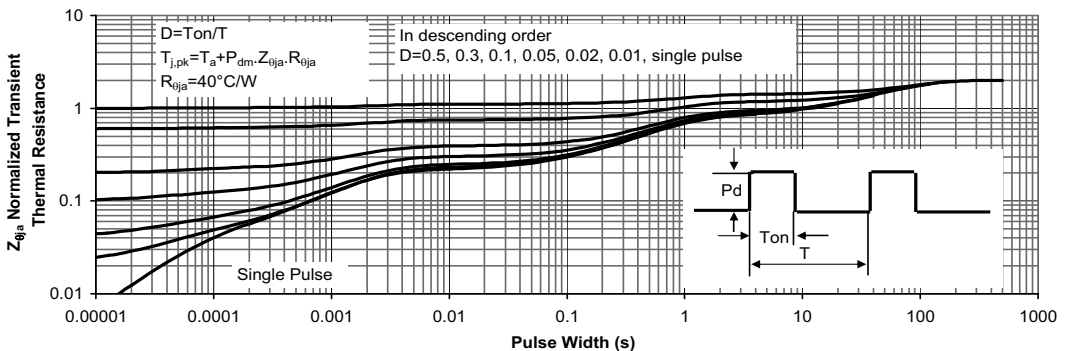


Figure 11: Normalized Maximum Transient Thermal Impedance