

Dual N-channel MOSFET

ELM14826AA-N

General description

ELM14826AA-N uses advanced trench technology to provide excellent $R_{ds(on)}$ and low gate charge.

Features

- $V_{ds}=60V$
- $I_d=6.3A$ ($V_{gs}=10V$)
- $R_{ds(on)} < 25m\Omega$ ($V_{gs}=10V$)
- $R_{ds(on)} < 30m\Omega$ ($V_{gs}=4.5V$)

Maximum absolute ratings

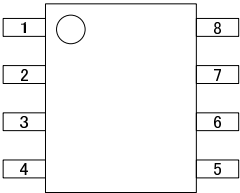
Parameter		Symbol	Limit	Unit	Note
Drain-source voltage		V_{ds}	60	V	
Gate-source voltage		V_{gs}	± 20	V	
Continuous drain current	$T_a=25^{\circ}C$	I_d	6.3	A	1
	$T_a=70^{\circ}C$		5.0		
Pulsed drain current		I_{dm}	40	A	2
Power dissipation	$T_a=25^{\circ}C$	P_d	2.00	W	
	$T_a=70^{\circ}C$		1.28		
Junction and storage temperature range		T_j, T_{stg}	-55 to 150	$^{\circ}C$	

Thermal characteristics

Parameter		Symbol	Typ.	Max.	Unit	Note
Maximum junction-to-ambient	$t \leq 10s$	$R\theta_{ja}$	50.0	62.5	$^{\circ}C/W$	1
Maximum junction-to-ambient	Steady-state		73.0	110.0	$^{\circ}C/W$	
Maximum junction-to-lead	Steady-state	$R\theta_{jl}$	31.0	40.0	$^{\circ}C/W$	3

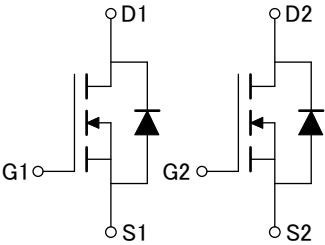
Pin configuration

SOP-8 (TOP VIEW)



Pin No.	Pin name
1	SOURCE2
2	GATE2
3	SOURCE1
4	GATE1
5	DRAIN1
6	DRAIN1
7	DRAIN2
8	DRAIN2

Circuit



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Electrical characteristics

Ta=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	BV _{dss}	I _d =250 μ A, V _{gs} =0V	60			V
Zero gate voltage drain current	I _{dss}	V _{ds} =48V V _{gs} =0V			1	μ A
		T _j =55°C			5	
Gate-body leakage current	I _{gss}	V _{ds} =0V, V _{gs} = $\pm$ 20V			100	nA
Gate threshold voltage	V _{gs(th)}	V _{ds} =V _{gs} , I _d =250 μ A	1.0	2.1	3.0	V
On state drain current	I _{d(on)}	V _{gs} =10V, V _{ds} =5V	40			A
Static drain-source on-resistance	R _{ds(on)}	V _{gs} =10V I _d =6.3A		20	25	m Ω
		T _j =125°C		34	42	
		V _{gs} =4.5V, I _d =5.7A		22	30	m Ω
Forward transconductance	G _{fs}	V _{ds} =5V, I _d =6.3A		27		S
Diode forward voltage	V _{sd}	I _s =1A, V _{gs} =0V		0.74	1.00	V
Max. body-diode continuous current	I _s				3	A
DYNAMIC PARAMETERS						
Input capacitance	C _{iss}	V _{gs} =0V, V _{ds} =30V, f=1MHz		1920	2300	pF
Output capacitance	C _{oss}			155		pF
Reverse transfer capacitance	C _{rss}			116		pF
Gate resistance	R _g	V _{gs} =0V, V _{ds} =0V, f=1MHz		0.65	0.80	Ω
SWITCHING PARAMETERS						
Total gate charge (10V)	Q _g	V _{gs} =10V, V _{ds} =30V, I _d =6.3A		47.6	58.0	nC
Total gate charge (4.5V)	Q _g			24.2	30.0	nC
Gate-source charge	Q _{gs}			6.0		nC
Gate-drain charge	Q _{gd}			14.4		nC
Turn-on delay time	t _{d(on)}			7.6		ns
Turn-on rise time	t _r	V _{gs} =10V, V _{ds} =30V		5.0		ns
Turn-off delay time	t _{d(off)}	R _l =4.7 Ω , R _{gen} =3 Ω		28.9		ns
Turn-off fall time	t _f			5.5		ns
Body diode reverse recovery time	t _{rr}	I _f =6.3A, dI/dt=100A/ μ s		33.2	40.0	ns
Body diode reverse recovery charge	Q _{rr}	I _f =6.3A, dI/dt=100A/ μ s		43.0		nC

NOTE :

1. The value of R θ _{ja} is measured with the device mounted on 1in² FR-4 board of 2oz. Copper, in still air environment with Ta=25°C. The value in any given applications depends on the user's specific board design. The current rating is based on the t $\leq$ 10s thermal resistance rating.
2. Repetitive rating, pulse width limited by junction temperature.
3. The R θ _{ja} is the sum of the thermal impedance from junction to lead R θ _{jl} and lead to ambient.
4. The static characteristics in Figures 1 to 6 are obtained using 80 μ s pulses, duty cycle 0.5%max.
5. These tests are performed with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with Ta=25°C. The SOA curve provides a single pulse rating.

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■ Typical electrical and thermal characteristics

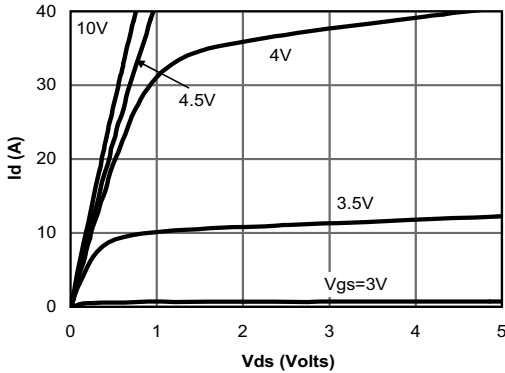


Fig 1: On-Region Characteristics

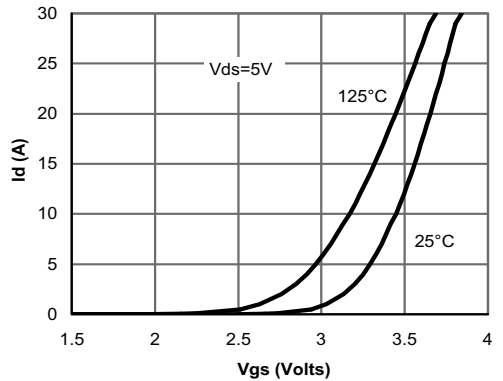


Figure 2: Transfer Characteristics

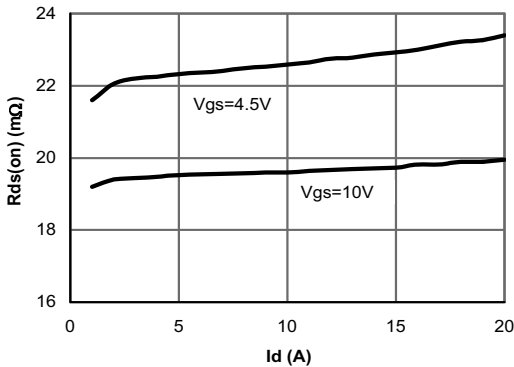


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

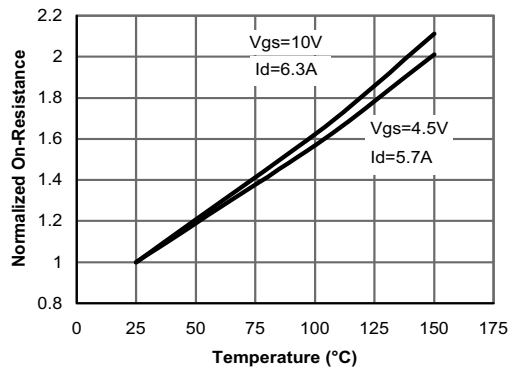


Figure 4: On-Resistance vs. Junction Temperature

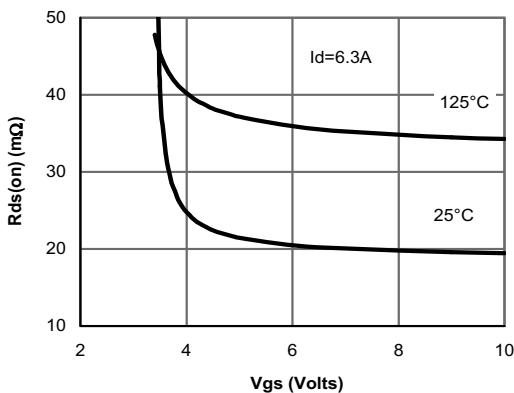


Figure 5: On-Resistance vs. Gate-Source Voltage

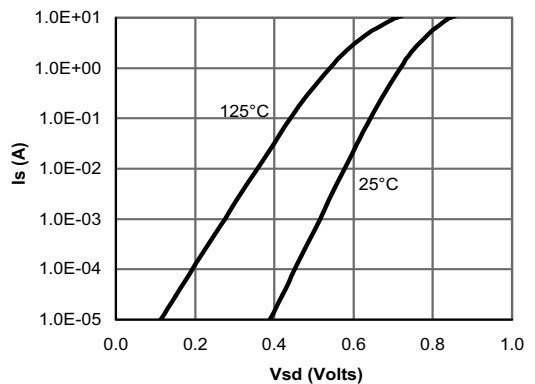


Figure 6: Body-Diode Characteristics

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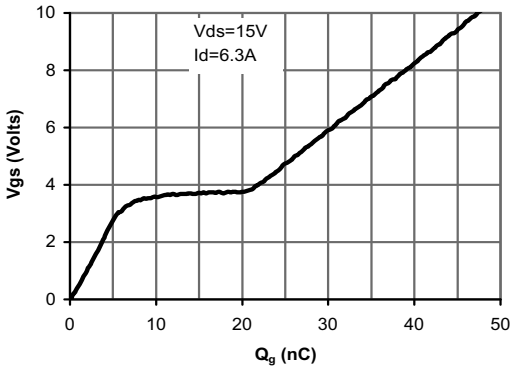


Figure 7: Gate-Charge Characteristics

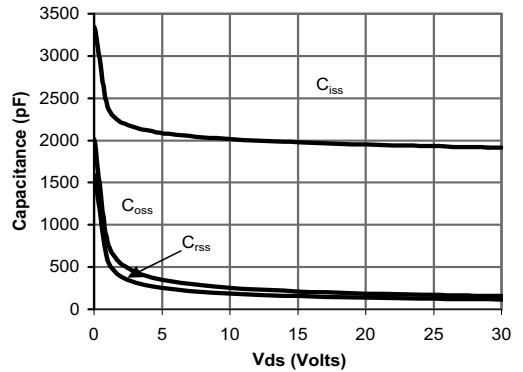


Figure 8: Capacitance Characteristics

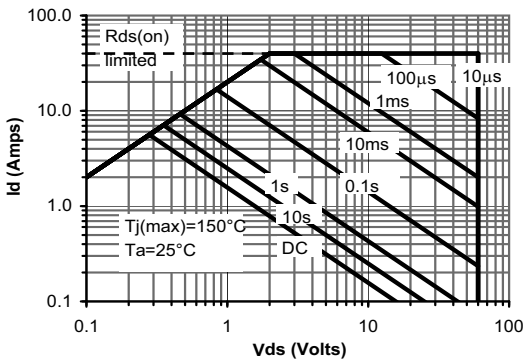


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

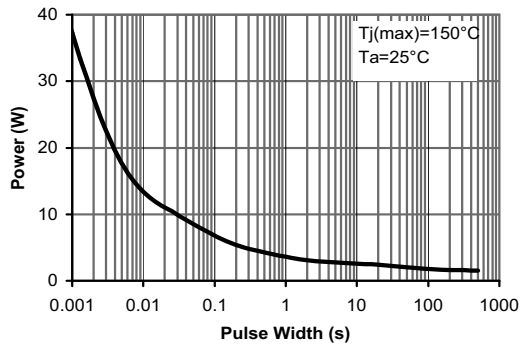


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

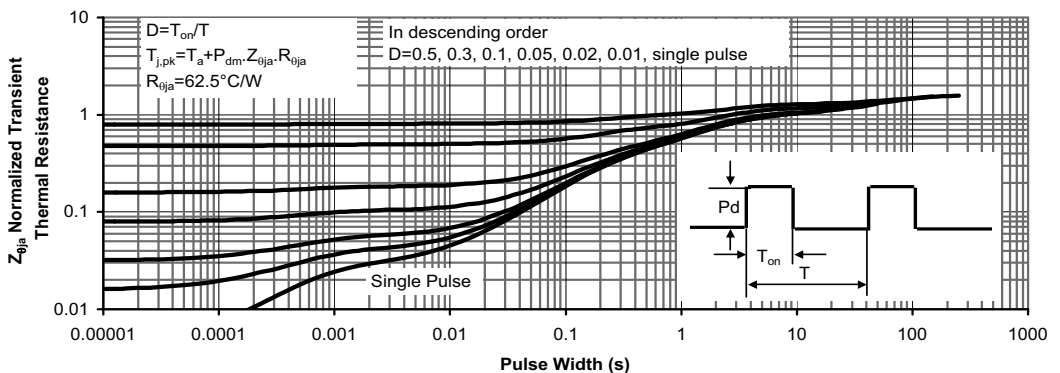


Figure 11: Normalized Maximum Transient Thermal Impedance